JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST -2 EXAMINATION- 2023
B.Tech-III Semester (ECE)

COURSE CODE (CREDITS): 18B11EC312(4) MAX. MARKS: 35
COURSE NAME: Digital Electronics and Logic design
COURSE INSTRUCTORS: Munish Sood MAX. TIME: 2 Hours

Note: (a)*All questions are compulsory.*
(b)Marks are indicated against each question in square brackets.
(c) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Q1) Design a 3 bit binary GRAY code synchronous counter using state diagram, state table and J-K flip flops. **CO-3[7]**

Q2) Design a 4 bit asynchronous binary Decade counter with each flip flop negatively edge triggered. Develop a timing diagram showing the Q output of each flip flop. **CO-6[5]**

Q3) Design a 4 bit bidirectional shift register using D flip flop. Develop a timing diagram showing the Q output of each fli flop. **CO-4[5]**

Q4) Design a 4 bit Digital to Analog Converter (DAC) using binary weighted resistor. A certain binary-weighted-input DAC has a binary input of 1101. If a HIGH = +3.0 V and a LOW = 0 V, what is V_{out}? **CO-5[5]**

Q5) Implement the following logic expression using only NOR or NAND gates **C0-1[5]**

a) $X = (A + B)(\bar{C} + D)(E + F)$
b) $(AB + \bar{C})D + EF$

Q6) Using Boolean Algebra and De-Morgan's theorem simplify the following expressions

a) $AB + A(B + C) + B(B + C)$ **CO-2[3]**
b) $\overline{ABC + DEF}$

Q7) Use a Karnaugh map to minimize the following standard SOP 5 variable expression:

$X=\bar{A}\bar{B}\bar{C}\bar{D}\bar{E} + \bar{A}\bar{B}C\bar{D}\bar{E} + \bar{A}BC\bar{D}\bar{E} + \bar{A}B\bar{C}\bar{D}\bar{E} + \bar{A}\bar{B}\bar{C}\bar{D}E + \bar{A}BC\bar{D}E + \bar{A}BCDE + A\bar{B}\bar{C}\bar{D}\bar{E} + A\bar{B}\bar{C}\bar{D}E + ABC\bar{D}E + ABCDE + A\bar{B}CDE$ **CO-2[5]**