JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATION- 2024

B. Tech-VI Semester (ECM)

COURSE CODE(CREDITS): 21B11EM611(3) MAX. MARKS: 15

COURSE NAME: Computer Organization and Architecture

COURSE INSTRUCTOR: Dr. Naveen Jaglan MAX. TIME: 1 Hour

Note: *(a) All questions are compulsory.*

(b)Marks are indicated against each question in square brackets.

(c) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

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1. Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied:

(+15) × (-13)

Assume 5-bit registers that hold the signed numbers. [CO-2; 4 marks]

2. Explain the characteristics of RISC and CISC processors. In order to implement complex instructions why the CISC architecture uses microprogramming?

[CO-2; 2 marks]

3. What do you understand by Von Neumann type computation? Explain the organization of a Von Neumann computer using a schematic diagram. Point out the shortcomings of Von-Neumann architecture. [CO-1; 3 marks]

4. Reduce the following Boolean expression using Boolean algebra:

$$F(A, B, C) = AB+BC+\bar{A}C$$ [CO-1; 2 marks]

5. Show the step-by-step non restoring division process for unsigned numbers when the following binary numbers are divided:

(+19) ÷ (+4) [CO-2; 4 marks]