JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATION- 2024

M. Tech.-2nd Semester (CSE/IT/**ECE**/CE)

COURSE CODE (CREDITS): 21M11EC211 MAX. MARKS: 15

COURSE NAME: Digital System Design Using Verilog HDL

COURSE INSTRUCTORS: Dr. Harsh Sohal MAX. TIME: 1 Hour

Note: (a)*All questions are compulsory.*

(b)Marks are indicated against each question in square brackets.

(c) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

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Q1. [CO1] Choose the most appropriate option for the following questions: 0.5x4 = 2

(i) What is the biggest drawback of microprocessor/DSP systems when compared to FPGAs?

a. Speed—they are too fast
b. Not enough flexibility
c. Speed—they are too slow
d. Too much flexibility

(ii) The statement " byte = data1[31-:8];" will assign _____ to 'byte' and the statement "byte = data1[24+:8];" will assign_____ to 'byte'.

a. data[31:24], data[31:24]
b. data[24:31], data[31:24]
c. data[31:24], data[24:31]
d. data[24:31], data[24:31]

(iii) Which of the following is not correct about the instance of a module in Verilog HDL?

a. An instance of a module has a unique identity and is different from other instances of the same module.
b. Each instance has an independent copy of the internals of the module.
c. When using the instance of a module, Name of that instance is not mandatory.
d. When using the instance of a module, Name of that instance is mandatory.

(iv) You are working in a company to develop a product set to be produced in large scale of the order of millions of units. Time to market and cost are not of concern. Only requirement is the highest possible performance. Which of the following solutions should be used?

a. reconfigurable FPGA
b. programmable DSP
c. ASIC
d. general purpose microprocessor like Arduino Uno

Q2. [CO2] Give the architectural comparison of PROM, PAL and PLAs. [3]

Q3. [CO2]

Discuss the advantages and disadvantages of ASIC over FPGA and vice versa. How do non-recurring costs and manufacturing costs help us to make a choice between the two? (Graphs can be plotted). Also mention the applications where FPGAs are preferred over ASICs. [4]

Q4. [CO1] What are the two styles to apply stimulus to a design modeled in verilog HDL? Explain. Which style is more efficient? Can we use verilog HDL to write test benches? [3]

Q5. [CO1] What is instantiation in Verilog HDL? Explain with a simple design example. [3]