JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- APRIL-2023

COURSE CODE (CREDITS): 19B1WEC831 (3) MAX. MARKS: 25

COURSE NAME: Digital CMOS ICs

COURSE INSTRUCTORS: Dr. Harsh Sohal MAX. TIME: 1 Hour 30 Minutes

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Note: *All questions are compulsory. Marks are indicated against each question in square brackets.*

Q1. [CO1] [4]

Describe the following terms with respect to CMOS circuits (use suitable diagrams when required):

(a) Moore's Law (b) Inversion layer (c) Feature size

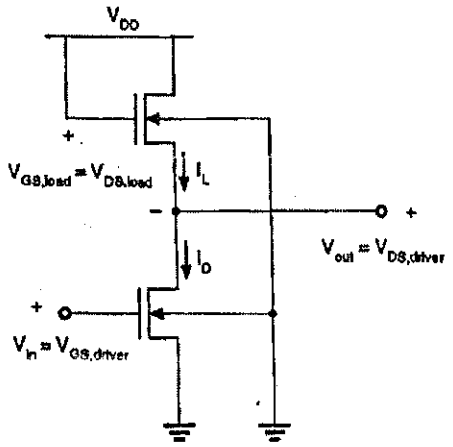
(d) Cross talk

Q2. [CO1+CO2] [4]

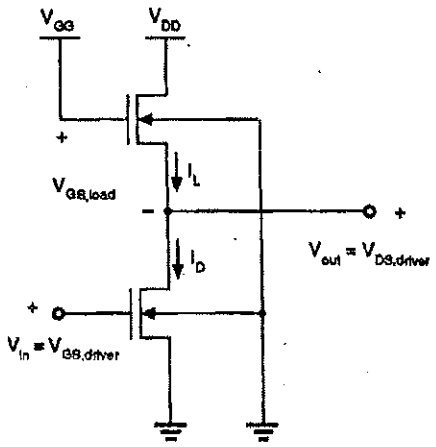
Differentiate between an n channel Enhancement MOSFET and an n channel Depletion MOSFET. (Draw the required diagrams and plot the characteristics). [4]

Q3. [CO2+CO3][4]

For the inverter circuits given below derive the expression for V_{OH} for both (a) and (b). Which of the two shall give better output voltage swing? Explain. [4]



(a)



(b)

Q4. [CO2+CO3][5]

Given V_{DD} = 2.5 V, k' = 40μA/V^2, andV_{T0}= 0.5 V, design a resistive-load inverter circuit with V_{OL}= 0.1 V.

(a) Determine the (W/L) ratio of the driver transistor and the value of the load resistor R_L that achieves the required V_{OL}. [3]

(b) Calculate the DC power dissipation of the inverter above (assuming that the input voltage is "low" during 50% of the operation time, and "high" during the remaining 50%) when W/L=1. [2]

Q5. [CO1+CO3] [8]

(a) Discuss the advantages and disadvantages of CMOS inverter with respect to D-MOSFET Load inverter. [2]

(b) Consider a CMOS inverter circuit with the following parameters: [3+3]

V_{DD} =5V

$V_{T0,n}$ = 1 V

$V_{T0,P}$= -1 V

k_n= 200 μA/V^2

k_p = 80 μA/V^2

Calculate (i) Noise Margin Low (NM_L) (ii) Threshold voltage (VTH) of the CMOS inverter