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# **Evaluation of jitter and its control using jitter attenuated circuits**

Project Report submitted in partial fulfillment of the requirement for the degree of

Bachelor of Technology.

In

Electronics and Communication Engineering

Under the Supervision of

***Mr S.V.R.K .Rao***

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### Certificate

This is to certify that project report entitled **“Evaluation of jitter and its control using jitter attenuated circuits”**, submitted by Samarth Nagpal (091046), Sarthak Gupta (091056), Archit Garg (091113) in partial fulfillment for the award of degree of Bachelor of Technology in Electronics and Communication Engineering to Jaypee University of Information Technology, Waknaghat, Solan has been carried out under my supervision.

This work has not been submitted partially or fully to any other University or Institute for the award of this or any other degree or diploma.

**Date: 29<sup>th</sup> May 2013**

  
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## Table of Content

S. No.	Topic	Page No.
	XI Abstract.....	9
1.	Introduction.....	10
1.1	Jitter.....	10
1.2	Sampling jitter.....	11
1.3	Sources of Jitter.....	11
1.3.1	Electromagnetic Interference.....	11
1.3.2	Cross Talk.....	11
1.3.3	Reflection.....	12
1.3.4	Shot Noise.....	12
1.3.5	Flicker Noise.....	12
1.3.6	Thermal Noise.....	12, 13
1.4	Jitter components and classification.....	14
1.5	Jitter components.....	15
1.5.1	Random jitter.....	15
1.5.2	Deterministic jitter.....	15
1.5.3	Total jitter.....	15
1.6	Types of jitter.....	16
1.6.1	Periodic jitter.....	16
1.6.2	Data dependent jitter(DDJ).....	16
1.6.2.1	Duty cycle distortion (DCD).....	16
1.6.2.2	Inter symbol interference(ISI).....	16
1.7	Metrics of jitter.....	17
1.7.1	Bit error rate.....	17
1.7.2	RMS to peak to peak jitter conversion.....	18
1.8	Mitigation.....	19
1.8.1	Anti jitter circuits.....	19
1.8.2	Jitter buffers.....	19
1.8.3	Dejitterizer.....	19
2.	Measurement of jitter.....	20
2.1	Jitter measurement techniques.....	20
2.1.1	Bathtub plot.....	20
2.1.2	Histogram.....	20
2.1.3	Eye diagram.....	21
2.2	Eye diagram.....	21
2.2.1	Introduction.....	21
2.2.2	Measurements from an eye diagram.....	22
2.3	Measurements from an eye diagram.....	23
2.3.1	Eye crossing time.....	23
2.3.2	Eye crossing amplitude.....	23
2.3.3	Eye delay.....	24
2.3.4	Eye level.....	24

2.3.5	Eye amplitude.....	25
2.3.6	Eye height.....	25
2.3.7	Eye width.....	26
2.3.8	Vertical eye opening.....	26
2.3.9	Eye crossing percentage.....	26
2.3.10	Eye SNR.....	26
2.3.11	Horizontal eye opening.....	27
2.3.12	Eye rise time.....	27
2.3.13	Eye Fall time.....	27
3.	Jitter Attenuation Circuits.....	28
3.1	Phase Locked Loop.....	28
3.1.1	Introduction.....	28
3.1.2	Tradeoffs.....	29
3.1.3	Block Diagram for PLL.....	30
3.1.4	Basic VCO circuits.....	30
3.2	Delay Locked Loop.....	31
3.2.1	Introduction.....	31
3.2.2	Basic structure of a DLL.....	31
3.3	Table comparison of DLL and PLL.....	32
4	Basic JAC theory.....	33
4.1	Introduction to the concept.....	33
4.2	The differential JAC system.....	34
4.3	The JAC system.....	35
5	Implementation of real time system.....	36
5.1	Flow chart.....	36
5.2	Path Loss.....	36
5.2.1	Introduction.....	36
5.2.2	Pathloss Friis equation.....	37
5.2.3	Pathloss diagram.....	37
5.3	Fading.....	38
5.3.1	Introduction.....	38
5.3.2	Fading diagram.....	38
6	Eye diagrams implementation on MATLAB.....	39
6.1	Eye diagram basic.....	39
6.2	Eye diagram with AWGN(10SNR).....	40
6.3	Eye diagram with AWGN(20SNR).....	41
6.4	Eye diagram with AWGN(40SNR).....	42
6.5	Signal with AWGN and Path loss and Fading.....	43
6.5.1	Signal with AWGN and Pathloss.....	43
6.5.2	Signal with AWGN and Path loss and Fading.....	44
6.6	Mitigation.....	45
6.6.1	Mitigation using MIMO.....	45, 46



XII	Conclusion.....	47
XIII	Future Work.....	48
XIV	Bibliography.....	49

## TABLE OF FIGURES

Figure no. : Title	Page No.
Figure 1.1.....	10
Figure 1.2.....	14
Figure 1.3.....	16
Figure 1.4.....	18
Figure 2.1.....	20
Figure 2.2.....	21
Figure 2.3.....	22
Figure 2.4.....	23
Figure 2.5.....	23
Figure 2.6.....	24
Figure 2.7.....	24
Figure 2.8.....	25
Figure 2.9.....	25
Figure 2.10.....	26
Figure 3.1.....	29
Figure 3.2.....	30
Figure 3.3.....	30
Figure 3.4.....	31
Figure 4.1.....	33
Figure 4.2.....	33
Figure 4.3.....	34
Figure 4.4.....	35
Figure 4.5.....	35



Figure 5.1.....	36
Figure 5.2.....	37
Figure 5.3.....	38
Figure 6.1.....	39
Figure 6.2.....	39
Figure 6.3.....	40
Figure 6.4.....	40
Figure 6.5.....	41
Figure 6.6.....	41
Figure 6.7.....	42
Figure 6.8.....	42
Figure 6.9.....	43
Figure 6.10.....	43
Figure 6.11.....	44
Figure 6.12.....	44
Figure 6.13.....	46

## **XI. ABSTRACT**

This report talks about performance evaluation of jitter and jitter attenuation circuits. One of the biggest problems we face in communication is the presence of jitter which leads to many problems and corruption of data and one may even lose the entire data. In the project we have first studied the techniques to measure jitter. Next study of various jitter attenuation circuits available in market was done. These circuits though having certain advantages, have certain drawbacks also. A basic model of JAC has also been proposed. This basic model decides on the level of signal we want to keep as threshold and then proceed, so that jitter is reduced. Simulations on MATLAB have been done. These simulations were done to study the eye diagrams under various circumstances. The eye diagrams are the best available tool to study the presence of jitter due to various parameters and evaluation of ISI and jitter etc.



## CHAPTER 1: INTRODUCTION

### 1.1 Jitter

Jitter is the random arrival time variation of a signal around what would be the ideally timed version of that signal. It is the enemy of any system whose accuracy depends on a signal arriving regularly at a specific time. For example, most sequential digital systems expect the clock signal, or, more correctly, the rising or falling edge of the signal used for clocking, to arrive at relatively even spaced intervals. If there is jitter on the clock signal it randomly makes the expected signals arrive early at times and arrive late at others. Jitter may be observed in characteristics such as the frequency of successive pulses, the signal amplitude, or phase of periodic signals.

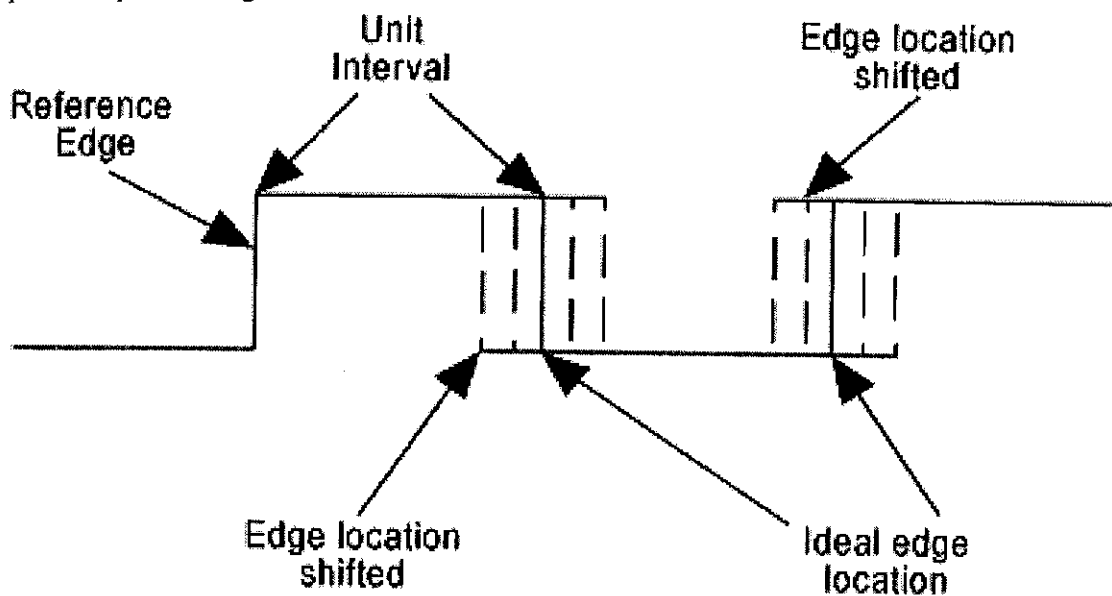


Fig 1.1

## 1.2 SAMPLING JITTER

In analog to digital and digital to analog conversion of signals, the sampling is normally assumed to be periodic with a fixed period - the time between every two samples is the same. If there is jitter present on the clock signal to the analog-to-digital converter or a digital-to-analog converter, the time between samples varies and instantaneous signal error arises. The error is proportional to the slew rate of the desired signal and the absolute value of the clock error. Various effects such as noise (random jitter), or spectral components (periodic jitter) can come about depending on the pattern of the jitter in relation to the signal. In some conditions, less than a nanosecond of jitter can reduce the effective bit resolution of a converter with a Nyquist frequency of 22 kHz to 14 bits.

This is a consideration in high-frequency signal conversion, or where the clock signal is especially prone to interference.

## 1.3 SOURCES OF JITTER

Understanding the underlying cause of jitter is crucial to signal integrity analysis. Determining the sources of jitter allows you to characterize and eliminate the potential problem. Here, we examine the most frequent causes of deterministic jitter(DJ) and random jitter(RJ).

Some common sources of DJ include EMI, Crosstalk and Reflection.

### 1.3.1 ELECTRO Magnetic Interference

EMI is the result of unwanted radiated or conducted emission from a local device or system switching type power supplies are common sources of EMI. These devices radiate strong high-frequency electric and magnetic fields, and they can conduct a large amount of electrical noise in a system if they lack adequate shielding and output filtering. EMI can couple or induce noise currents in a signal conductor and corrupt the signal by altering its bias. Because the interfering signal is deterministic, the resulting jitter is also deterministic. EMI may also corrupt a ground reference plane or a supply voltage plane by introducing transient noise currents. Noise currents can sporadically alter the effective input threshold of signal receiver. Given that logic signals require a finite time to change states, a sporadic change in receiver threshold results in signal jitter.

### 1.3.2 Crosstalk

Crosstalk occurs when the magnetic or electric fields of a signal on a conductor are inadvertently coupled to an adjacent signal-carrying conductor. The coupled signal components algebraically add to the desired signal, and can slightly alter its bias depending on the amount of coupling and



the frequency content of the interfering signal. The altered bias translates into jitter as the signal transitions the receiver's threshold. Reflection in a data signal channel creates DJ due to the signal interfering with itself. Signal reflection occurs when impedance mismatches are present in the channel. With copper technology, optimum signal power transfer occurs when the transmitter and receiver have the same characteristics impedance as the medium. If an impedance mismatch is present at the receiver, a portion of the energy is reflected back through the medium to be transmitter.

### **1.3.3 Reflection**

Reflection typically comes from uncontrolled stubbing and incorrect termination. Reflected energy, or energy not available to the receiver, reduces the signal-to-noise ratio at the receiver and increase jitter. If the transmitter is also mismatched, the transmitter absorbs a portion of the reflected signal energy while the remainder is reflected towards the receiver (again). Eventually the delayed signal energy arrives at the receiver, out of phase with the original signal. The portion that is absorbed is algebraically summed with first time arriving signal energy, resulting in DJ(specially, ISI) from the receiver's perspective.

Common sources of RJ include shot noise, flicker noise and thermal noise

### **1.3.4 Shot Noise**

Shot noise broadband "white" noise generated when electrons and holes move in a semiconductor. Shot noise amplitude is a function of average current flow. The current fluctuations about the average value give the rise in noise. This will depend on the process. For example, in a semiconductor it is the randomness of the density of electrons and holes. In a signal channel, shot noise contributes to the RJ.

### **1.3.5 Flicker Noise**

Flicker noise has a spectral distribution that is proportional to  $1/f$  where  $a$  is generally close to unity. Because flicker noise is proportional to  $1/f$ , its contribution is most dominant at lower frequencies. The origin of flicker noise is a surface effect due to fluctuations in the carrier density as electrons are randomly captured and emitted from oxide interface traps.

### **1.3.6 Thermal Noise**

Thermal noise can be represented by broadband "white" noise, and has flat spectral density. It is generated by the transfer of energy between "free" electrons and ions in a conductor. The amount of energy transfer and, therefore, the amount of noise, are related to temperature. Thermal noise is unrelated to signal current flow, but it is a contributor to RJ in signal with low signal-to-noise

ratios. Electron scattering due to non perfect lattice structure causes RJ. The deviations of the lattice structure are due to crystal vibration or phonons. Ions do not remain at their ideal crystal location because of thermal energy. The deviation of the lattice structure from its ideal position can induce electron scattering. The amplitude of ionic perturbation decrease with temperature and at sufficiently low temperature will not completely eliminate RJ because of intrinsic defects, such as impurities, missing atoms, or discontinuities in the lattice structure caused by an interface. In these cases, the defect or impurities causes a localized scattering centre, giving rise to RJ.



## 1.4 JITTER COMPONENTS AND CLASSIFICATION

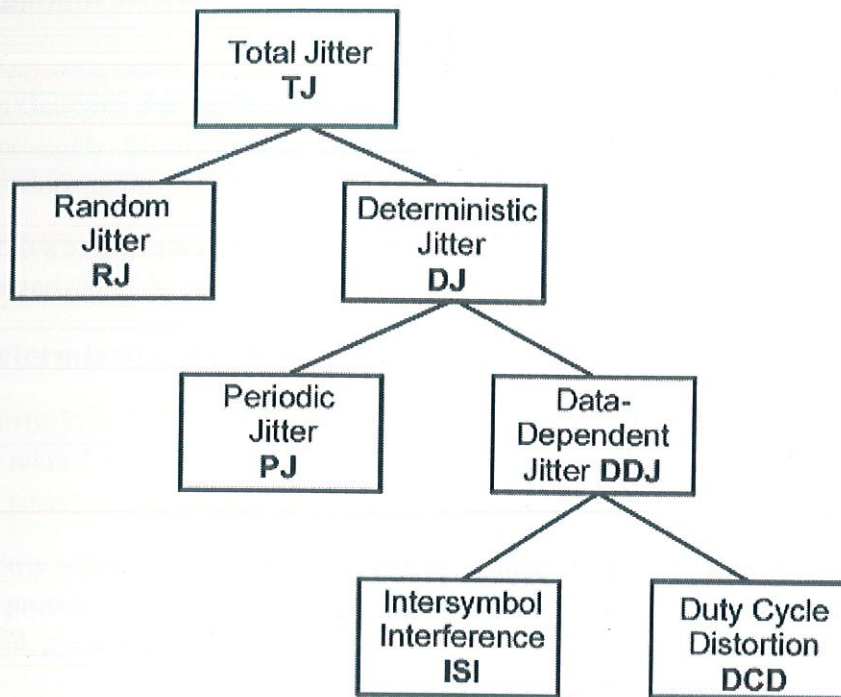


Fig 1.2

## 1.5 Jitter Components

The two major components of jitter are random jitter, and deterministic jitter.

### 1.5.1 Random Jitter

The random component in jitter is due to the noise inherent in electrical circuits and typically exhibits a Gaussian distribution. Random jitter (RJ) is due to stochastic sources, such as substrate and power supply. Electrical noise interacts with the slew rate of signals to produce timing errors at the switching points.

RJ is additive as the sum of squares, and follows a bell curve. Since random jitter is not bounded, it is characterized by its standard deviation (rms) value.

### 1.5.2 Deterministic Jitter

Deterministic jitter (DJ) is data pattern dependant jitter, attributed to a unique source. Sources are generally related to imperfections in the behavior of a device or transmission media but may also be due to power supply noise, cross-talk, or signal modulation.

DJ is linearly additive and always has a specific source. This jitter component has a non-Gaussian probability density function and is always bounded in amplitude. DJ is characterized by its bounded, peak-to-peak, value.

### 1.5.3 Total jitter

Total jitter ( $T$ ) is the combination of random jitter ( $R$ ) and deterministic jitter ( $D$ ):

$$T = D_{\text{peak-to-peak}} + 2 \times n \times R_{\text{rms}}$$

in which the value of  $n$  is based on the bit error rate (BER) required of the link.



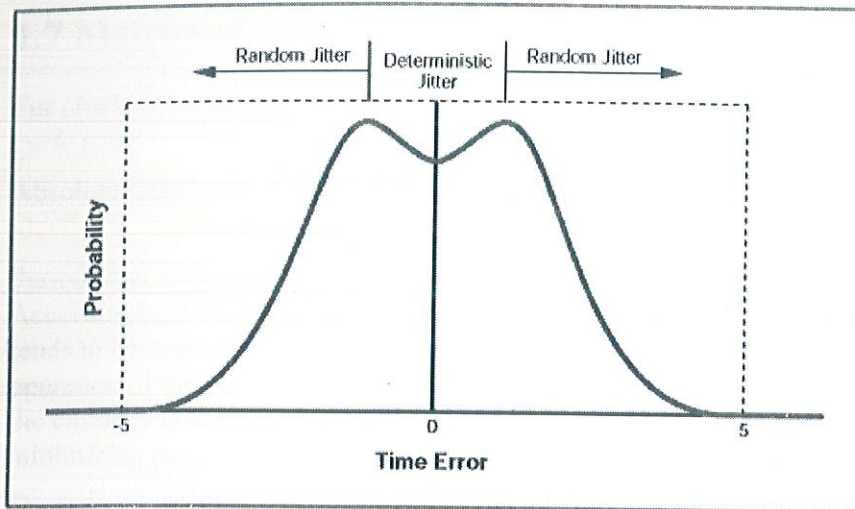


Fig 1.3

## 1.6 TYPES OF JITTER

Deterministic Jitter can be further classified as

### 1.6.1 Periodic Jitter

Period jitter is the change in a clock's output transition (typically the rising edge) from its ideal position over consecutive clock edges. Period jitter is measured and expressed in time or frequency. Period jitter measurements are used to calculate timing margins in systems, such as tSU and tCO.

### 1.6.2 Data Dependent Jitter(DDj)

**1.6.2.1 Duty cycle distortion (DCD)** is the deviation in propagation delay between high to low and low to high times. In other words, it is the deviation in the mean pulse width of the positive pulse compared to the negative pulse in a clock-like bit sequence. Amplitude offset error; turn on delays and saturation may be some of the causes of DCD.

**1.6.2.2 Inter-symbol interference (ISI)** is sometimes referred to as data dependent jitter. It is usually the result of bandwidth limitation in the transmitter or physical media; therefore, creating various amplitudes of data bits due to limited rise and fall times of signal. It occurs when the frequency components of the data (symbol) is propagated at different rates by the transmission medium.

## 1.7 Metrics of jitter

For clock jitter, there are three commonly used metrics: *absolute jitter*, *period jitter*, and *cycle to cycle jitter*.

Absolute jitter is the absolute difference in the position of a clock's edge from where it would ideally be.

Period jitter is the difference between any one clock period and the ideal/average clock period. Accordingly, it can be thought of as the discrete-time derivative of absolute jitter. Period jitter tends to be important in synchronous circuitry like digital state machines where the error-free operation of the circuitry is limited by the shortest possible clock period, and the performance of the circuitry is limited by the average clock period. Hence, synchronous circuitry benefits from minimizing period jitter, so that the shortest clock period approaches the average clock period.

Cycle-to-cycle jitter is the difference in length/duration of any two adjacent clock periods. Accordingly, it can be thought of as the discrete-time derivative of period jitter. It can be important for some types of clock generation circuitry used in microprocessors and RAM interfaces.

Since they have different generation mechanisms, different circuit effects, and different measurement methodology, it is useful to quantify them separately.

In telecommunications, the unit used for the above types of jitter is usually the *Unit Interval* (abbreviated *UI*) which quantifies the jitter in terms of a fraction of the ideal period of a bit. This unit is useful because it scales with clock frequency and thus allows relatively slow interconnects such as T1 to be compared to higher-speed internet backbone links such as OC-192. Absolute units such as *picoseconds* are more common in microprocessor applications. Units of *degrees* and *radians* are also used.

If jitter has a Gaussian distribution, it is usually quantified using the standard deviation of this distribution (RMS). Often, jitter distribution is significantly non-Gaussian. This can occur if the jitter is caused by external sources such as power supply noise. In these cases, *peak-to-peak* measurements are more useful. Many efforts have been made to meaningfully quantify distributions that are neither Gaussian nor have meaningful peaks (which are the case in all real jitter). All have shortcomings but most tend to be good enough for the purposes of engineering work. Note that typically, the reference point for jitter is defined such that the *mean* jitter is 0.

In networking, in particular IP networks such as the Internet, jitter can refer to the variation (statistical dispersion) in the delay of the packets.

### 1.7.1 Bit Error Rate

There are several ways to quantitatively state the amount of random jitter within a system. The first method is to give a standard deviation of the jitter distribution (or equivalently the RMS



value), and the second method is to select a bit error rate (BER) threshold and define the random jitter as a peak-to-peak value.

Jitter is essentially variation in the zero crossing times of the data eye. There are two ways that noise can cause bit errors in a system. One way occurs when the noise causes the data waveform to dip below the decision threshold voltage at the sampling instance (voltage noise). Also noise can cause errors by inducing jitter (timing noise). Jitter causes errors in a system by moving the data eye across the vertical sampling instance.

### 1.7.2 RMS to Peak-to-Peak Jitter Conversion

To convert between RMS and peak-to-peak random jitter, the BER must be specified. The following equations can be used to convert between the two:

$$\text{Jitter}_{p-p} = \alpha * \text{Jitter}_{rms}$$

$$\text{Jitter}_{rms} = \frac{\text{Jitter}_{P-P}}{\alpha}$$

$$\text{Where } \alpha = \frac{t(\text{sample}) - \text{jitter}_{P-P}}{\sigma \cdot \text{jitter}(rms)}$$

A Gaussian distribution describes random jitter. Qualitative analysis shows that the tails of a Gaussian distribution extend indefinitely on either side of the mean. Therefore, it is impossible to specify a peak-to-peak jitter range that bounds the jitter 100% of the time. Instead we want to identify a range that contains the jitter, for example, 99.99999% of the time. This means that 0.00001% of the time the jitter will be outside of our peak-to peak range.

Bit Error Rate (BER)	Ratio of peak deviation to standard deviation
$1 \times 10^{-4}$	3.891
$1 \times 10^{-5}$	4.417
$1 \times 10^{-6}$	4.892
$1 \times 10^{-7}$	5.327
$1 \times 10^{-8}$	5.731
$1 \times 10^{-9}$	6.109
$1 \times 10^{-10}$	6.467
$1 \times 10^{-11}$	6.807
$1 \times 10^{-12}$	7.131

Fig 1.4

## **1.8 Mitigation**

### **1.8.1 Anti-jitter circuits**

Anti-jitter circuits (AJCs) are a class of electronic circuits designed to reduce the level of jitter in a regular pulse signal. AJCs operate by re-timing the output pulses so they align more closely to an idealized pulse signal. They are widely used in clock and data recovery circuits in digital communications, as well as for data sampling systems such as the analog-to-digital converter and digital-to-analog converter. Examples of anti-jitter circuits include phase-locked loop and delay-locked loop. Inside digital to analog converters jitter causes unwanted high-frequency distortions. In this case it can be suppressed with high fidelity clock signal usage.

### **1.8.2 Jitter buffers**

Jitter buffers or de-jitter buffers are used to counter jitter introduced by queuing in packet switched networks so that a continuous payout of audio (or video) transmitted over the network can be ensured. The maximum jitter that can be countered by a de-jitter buffer is equal to the buffering delay introduced before starting the play-out of the media stream. In the context of packet-switched networks, the term *packet delay variation* is often preferred over *jitter*.

Some systems use sophisticated delay-optimal de-jitter buffers that are capable of adapting the buffering delay to changing network jitter characteristics. These are known as adaptive de-jitter buffers and the adaptation logic is based on the jitter estimates computed from the arrival characteristics of the media packets. Adaptive de-jittering involves introducing discontinuities in the media play-out, which may appear offensive to the listener or viewer. Adaptive de-jittering is usually carried out for audio play-outs that feature a VAD/DTX encoded audio, that allows the lengths of the silence periods to be adjusted, thus minimizing the perceptual impact of the adaptation.

### **1.8.3 Dejitterizer**

A dejitterizer is a device that reduces jitter in a digital signal. A dejitterizer usually consists of an elastic buffer in which the signal is temporarily stored and then retransmitted at a rate based on the average rate of the incoming signal. A dejitterizer is usually ineffective in dealing with low-frequency jitter, such as waiting-time jitter



## Chapter 2: Measurement of Jitter

### 2.1 Jitter Measurement Techniques

#### 2.1.1 Bathtub Plot

A viewpoint of jitter is provided by the bathtub plot, so named because of its characteristic curve looks like a cross-section of a bathtub it is a graph of bit error rate versus sampling point throughout the unit interval. It is typically shown with a log scale, which illustrates the functional relationship of sampling time to bit error ratio.

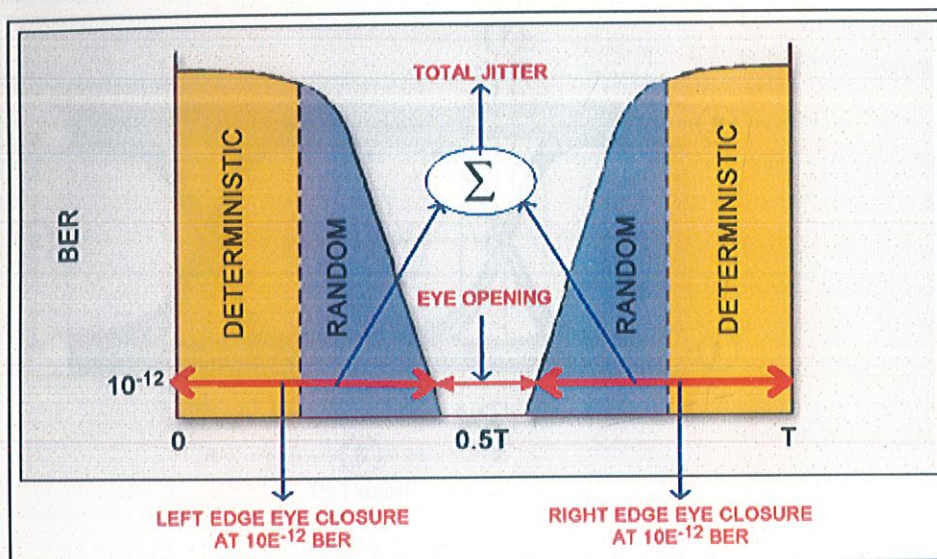


Fig 2.1

#### 2.1.2 Histogram

Histogram is another jitter measurement viewpoint. At their most basic, histograms plot the range of values exhibited by the analyzed parameter (often time or magnitude) on the x-axis versus the frequency of occurrence on the y-axis. Histogram provides a level of insight that the eye diagram cannot show, and so are very useful for understanding a circuit and for diagnosing problem. In addition, histograms, particularly the time interval error histogram, are key data sets for jitter separation routines required by various digital bus standards. For troubleshooting, waveform parameters such as rise time, fall time, period, and duty cycle can be histogrammed. These histograms clearly illustrate conditions such as multimodal performance distribution, which can then be correlated to circuit conditions such as transmitted patterns.



### 2.1.3 Eye Diagram

An eye diagram intuitively provides much information about the jitter on a signal as well as many of its other characteristics. For example, when intersymbol interference is present, those sections of the waveform with many transitions have a different characteristic from those where continuous identical digits are transmitted, which could be caused by having a low pass structure before the detector or a high pass structure that cause droop. Multiple distinct rising and falling edges probably indicate data-dependent jitter.

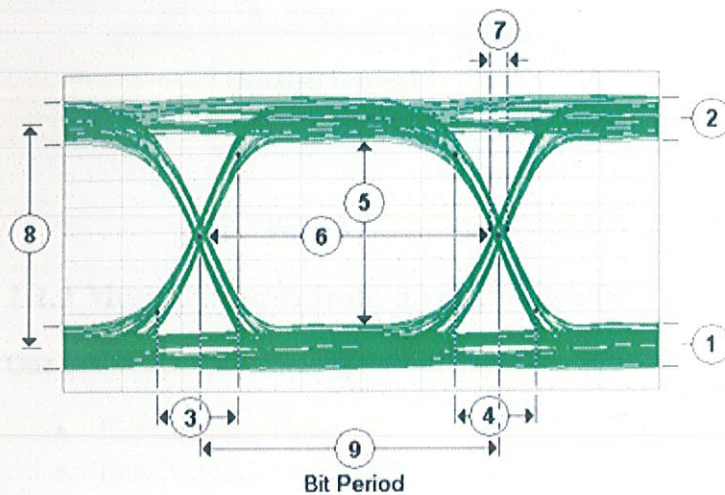


Fig 2.2

## 2.2 Eye Diagram

### 2.2.1 Introduction

In telecommunication, an eye pattern, also known as an eye diagram, is an oscilloscope display in which a digital data from a receiver is repetitively sampled and applied to the vertical input, while the data rate is used to trigger the horizontal sweep. It is so called because, for several types of coding, the pattern looks like a series of eyes between a pair of rails.

Several system performance measures can be derived by analyzing the display. If the signals are too long, too short, poorly synchronized with the system clock, too high, too low, too noisy, or too slow to change, or have too much undershoot or overshoot, this can be observed from eye diagram. Distortion of the signal waveform due to inter-symbol interference and noise appears as closure of the eye pattern. An open eye pattern corresponds to minimal signal distortion.



Slope of the eye determines how sensitive the signal is to timing error. A small slope allows eye to be opened more and hence less sensitivity to timing error. The width of the crossover represents the amount of jitter present in the signal. Small is better.

The wide superimposed transitions in the eye pattern are the result of high jitter associated with the signals, implying that the signals are not consistently transitioning at the required time. Smaller eye width implies a larger variance in the signal transition time.

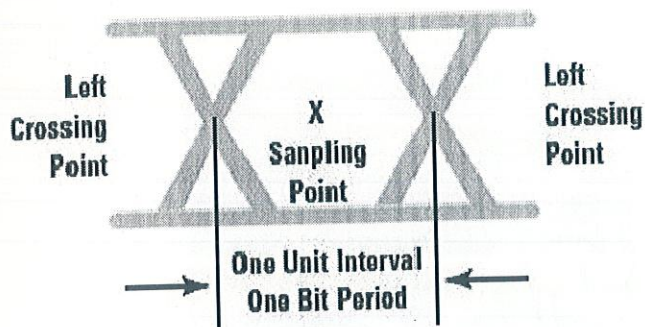


Fig 2.3

### 2.2.2 Measurements from an eye diagram

One can obtain the following measurements on an eye diagram:

- Eye Crossing Times
- Eye Crossing Amplitude
- Eye Delay
- Eye Level
- Eye Amplitude
- Eye Height
- Eye Width
- Vertical Eye Opening
- Eye Crossing Percentage
- Eye SNR
- Horizontal Eye Opening
- Eye Rise Time
- Eye Fall Time

## 2.3 Measurements from eye diagram

### 2.3.1 Eye crossing time

Eye crossing times are calculated as the means of the horizontal histogram for each crossing point, around the reference amplitude level. The value is measured in seconds. The mean value of all the horizontal PDF's is calculated in a region defined by the crossing band with property of the eye measurement setup object.

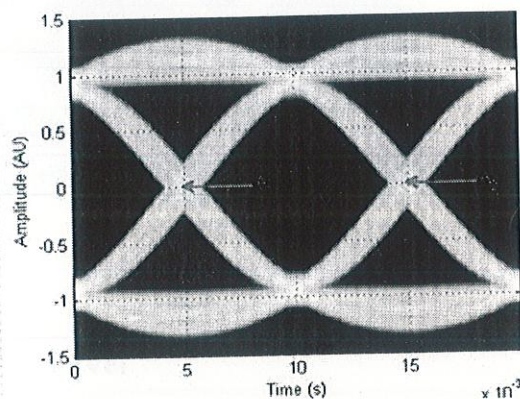


Fig 2.4

### 2.3.2 Eye Crossing Amplitude

Eye crossing amplitudes are the amplitude levels at which the eye crossings occur, measured in amplitude units (AU). The analyze method calculates this value using the mean value of the vertical histogram at the crossing times.

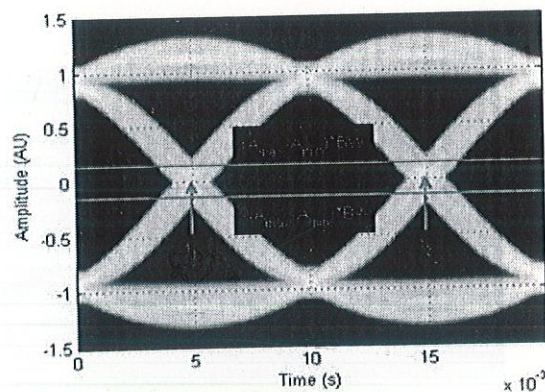


Fig 2.5



### 2.3.3 Eye Delay

Eye delay is the distance from the midpoint of the eye to the time origin, measured in seconds. The analyze method calculates this distance using the crossing time. Eye delay is also the best sampling point.

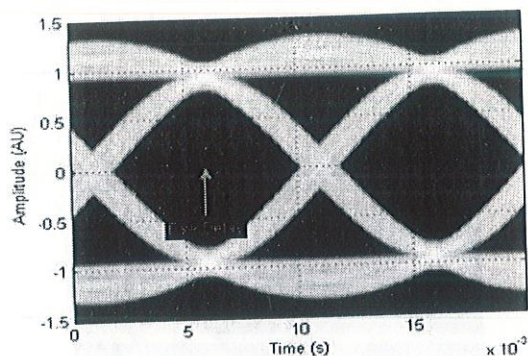


Fig 2.6

### 2.3.4 Eye Level

Eye level is the amplitude level used to represent data bits, measured in amplitude units (AU).

For an ideal NRZ signal, there are two eye levels: A+ and A-. The analyze method calculates eye levels by estimating the mean value of the vertical histogram in a window around the eye delay, which is also the 50% point between eye crossing times.

Analyze method also calculate the mean value of all the vertical histograms within the eye level boundaries.

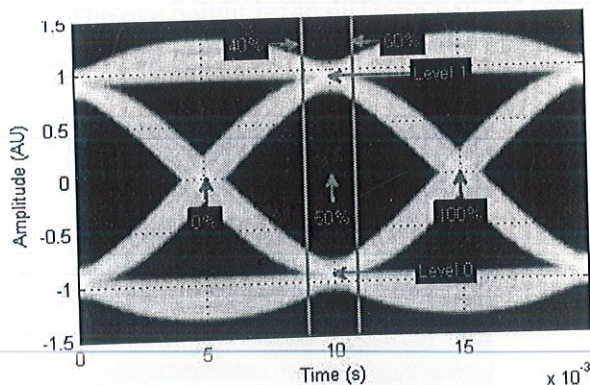


Fig 2.7

### 2.3.5 Eye Amplitude

Eye amplitude measured in amplitude units (AU), is defined as the distance between two neighboring eye levels. For an NRZ signal, there are only two levels: the high level and the low level.

The amplitude is the difference of these two values.

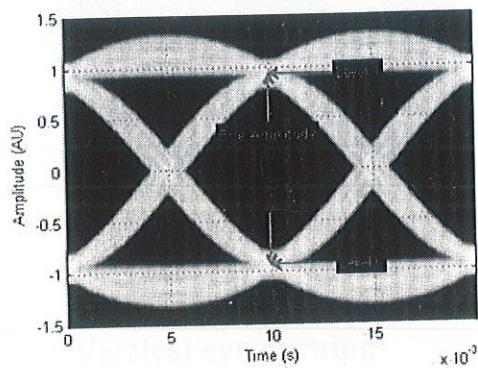


Fig 2.8

### 2.3.6 Eye Height

Eye height is measured in amplitude units (AU), is defined as the 3s distance between two neighboring eye levels. For an NRZ signal, there are only two levels: the high level and the low level. The eye height is the difference of the two 3s point. 3s point is defined as the point that is three standard deviations away from the mean value of a PDF.

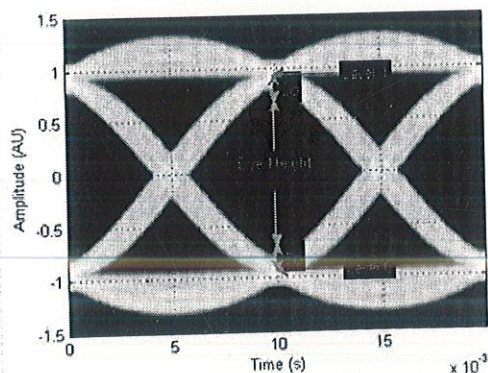


Fig 2.9



### 2.3.7 Eye Width

Eye width is measured in seconds, defined as the 3s distance between two eye crossing times. The 3s point is defined as the point that is three standard deviations away from the mean value of a PDF.

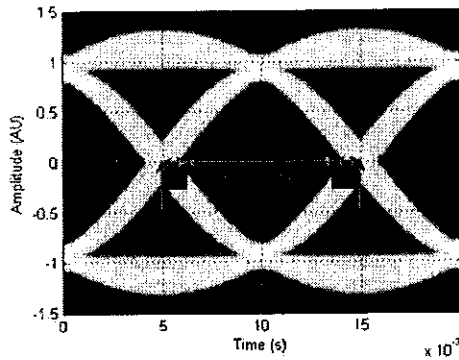


Fig 2.10

### 2.3.8 Vertical eye opening

Vertical eye opening is defined as the vertical distance between two points on the vertical histogram at eye delay that corresponds to the BER value defined by the BER threshold property of the eye measurement setup object. The analyze method calculates this measurement taking into account the random and deterministic components using a dual Dirac model.

### 2.3.9 Eye crossing percentage

Eye crossing percentage is the location of the eye crossing levels as a percentage of the eye amplitude.

### 2.3.10 Eye SNR

Eye signal-to-noise ratio is defined as the ratio of the eye amplitude to the sum of the standard deviations of the two eye levels.

### **2.3.11 Horizontal eye opening**

Horizontal eye opening is the horizontal distance between two points on the horizontal histogram that corresponds to the BER value defined by the BER Threshold property of the eye measurement setup object. The measurement is taken at the amplitude value defined by the reference amplitude property of the eye measurement setup object.

### **2.3.12 Eye rise time**

Eye rise time is the mean time between the low and high threshold values defined by the amplitude threshold property of the eye measurement setup object.

### **2.3.13 Eye fall time**

Eye fall time is the mean time between the high and low threshold values defined by the amplitude threshold property of the eye measurement setup object.



## Chapter 3: Jitter Attenuation Circuits

In order to reduce jitter there are certain techniques available in the market. All of these techniques have certain benefits but there are also certain shortcomings. In this section we are going to study the basic circuits available, their advantages and disadvantages and then study a basic jitter attenuation circuit.

### 3.1 Phase-locked loop (PLL)

#### 3.1.1 Introduction

Phase-locked loops (PLLs) are devices used to align the phase of a generated clock signal to an input reference clock signal. They often offer multiplication and division of the reference clock frequency, and, as a byproduct of their use of a low-pass filter, they also offer some level of jitter removal.

PLLs use feedback to adjust the phase of the output signal to match that of the input signal. The input clock is divided to match a divided version of the output signal and a phase detector compares these two signals. The phase detector outputs a value related to the difference in phase between the two signals.

Jitter also causes changes in the output of the phase detector because an edge moved by jitter can also be viewed as a disagreement in phase of the output clock and input reference clock.

Changes, when caused by jitter (or noise), are often of a high frequency and the low-pass filter, which the output of the phase detector passes through, reduces the effects of these random high-frequency additions to the proper output of the phase detector.

The low-pass filter, in effect, holds a proper value for the voltage controlled oscillator (VCO). The result that the filter removes jitter is a bonus. The low pass filter output is then transformed into a proper bias value for the voltage controlled oscillator which generates the output clock signal.

The VCO generates noise and that noise introduces variations in the output signal. These variations will accumulate as time offsets in the generated clock edges over time.

Increasing the bandwidth of the low-pass filter reduces the variation generated by the VCO, but as bandwidth is increased, less of the jitter on the input reference clock is removed.

PLLs filter out shorter-term jitter, such as variations in the reference clock period and the noise on the output of the phase detector, but may let longer-term jitter pass through.

The amount of long-term jitter that will result depends on the sensitivity of the VCO to noise. VCOs based on LC oscillators typically have high quality factor  $Q$ , that can substantially reduce their sensitivity to noise sources, but VCOs based on RC oscillators, such as relaxation or ring oscillators, have low- $Q$ , and thus are very sensitive to noise.

This suggests that LC oscillators should be the preferred implementation of the VCO when designing a PLL, but the limited frequency range and the larger chip area requirement of LC oscillators can make an LC VCO implementation impractical or unusable.

There is another trade off: A reduced bandwidth of the low pass filter. The lower the cutoff frequency of the filter, the longer it takes for the PLL to synchronize edges of the output clock to the input clock.

The acquisition time is the measure of how quickly the PLL can switch between frequencies. Acquisition time is important in systems where there may be quick switching between frequencies.

High-speed switching requires a wider passband, but the wider the passband, the more jitter effects get through from the reference clock.

Another parameter that is often used in PLL design is the acquisition range. This is the frequency range that the PLL can acquire a lock to and is directly proportional to the loop bandwidth. The trade offs in PLL design are shown.

The introduction of a phase-frequency detector before the charge pump block has improved performance. The phase-frequency detector effectively increases lock range and improves acquisition time while still allowing reduction of reference clock jitter. Though this improves acquisition time and range of the PLL, there is still self-generated VCO noise which appears up on the output of the PLL.

### 3.1.2 Trade offs

Increase loop bandwidth	Decrease loop bandwidth
Reduces acquisition time	Increases acquisition time
Increases acquisition range	Decreases acquisition range
Reduces VCO phase noise	Reduces reference clock jitter

Phase Locked Loop design bandwidth trade offs  
Fig 3.1



### 3.1.3 Block diagram for PLL

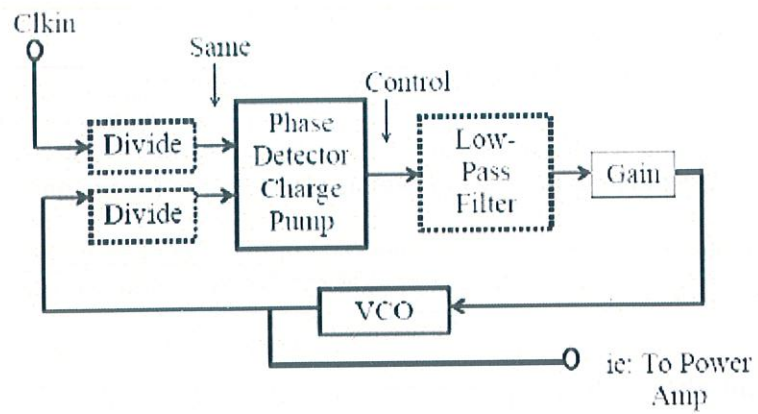
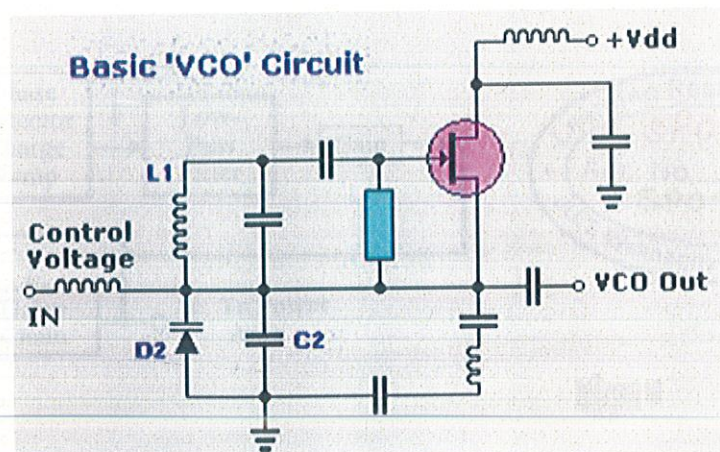


Fig 3.2

### 3.1.4 Basic VCO circuit



Phase Detector

Fig 3.3

## 3.2 Delay-locked loop (DLL)

### 3.2.1 Introduction

Delay-locked loops are another option that can be used to synchronize phase, and, compared to PLLs, they produce relatively little self-generated jitter.

Delay-locked loops differ from phase-locked loops in that they do not use a voltage controlled oscillator to generate their output.

The DLL uses a phase detector as does the PLL, but it uses the feedback information to speed up or slow down a delay line instead of control the frequency of a self-generated clock.

This delay line is composed of a chain of inverters each current starved such that their output can be adjusted to a slower transition by decreasing their current flow, or sped up by allowing more current to flow.

The input clock is fed directly into the delay chain and as such, any jitter on the input will be delayed but eventually show up at the output.

Because of this there is no reduction of the jitter on the input signal, but in the case where phase synchronization is required; a DLL may have less jitter on the output than a PLL simply due to the absence of a VCO.

### 3.2.2 Basic structure of a DLL

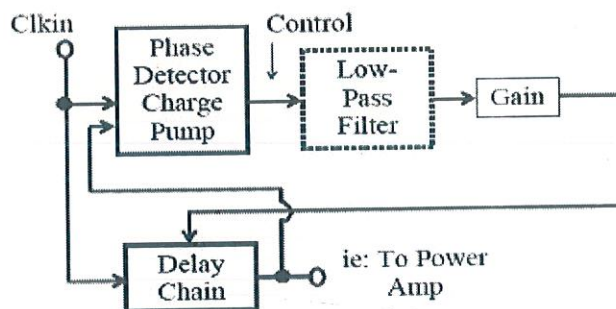


Fig 3.4



### 3.3 Table comparison DLLs and PLLs.

Phase-locked loops	Delay-locked loops
Second/Third order loops (Stability can be an issue)	First order loop (Always stable)
Frequency synthesis possible	Single output frequency
Input jitter is filtered	No VCO noise
Phase error accumulates (Lengthens acquisition time)	Phase error does not accumulate
Limited frequency capture range	Single output frequency
Unlimited phase capture range	Limited phase capture range

## Chapter 4: Basic JAC Theory

### 4.1 Introduction to the concept

The JAC is a multi-staged circuit. The first stage changes the input square wave into another square wave which fits a particular set of requirements. The next stage takes the adjusted square wave and turns it into a sawtooth wave by creating a rising (falling) slope when the square wave is high, and creating a falling (rising) slope when it is low.

The final stage is a level sensor which watches when the saw tooth crosses a certain level. The Combination of these three blocks can remove 100% of the jitter from a signal if the circuit behaves ideally (no intrinsic noise, switching non idealities, process variations, etc).

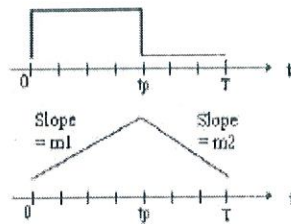


Fig 4.1

When the square pulse is high, the value on the graph below it rises with a slope of  $m1$ . When the square wave is low, the graph below the square wave falls at a slope of  $m2$ . if, for some time  $t_p$  the graph is rising at a slope of  $m1$  and the rest of the time the graph is falling at slope  $m2$ , after time  $T$ , the graph will be at the same height as it was at time zero

$$t_p \times m1 - (T - t_p) \times m2 = 0$$

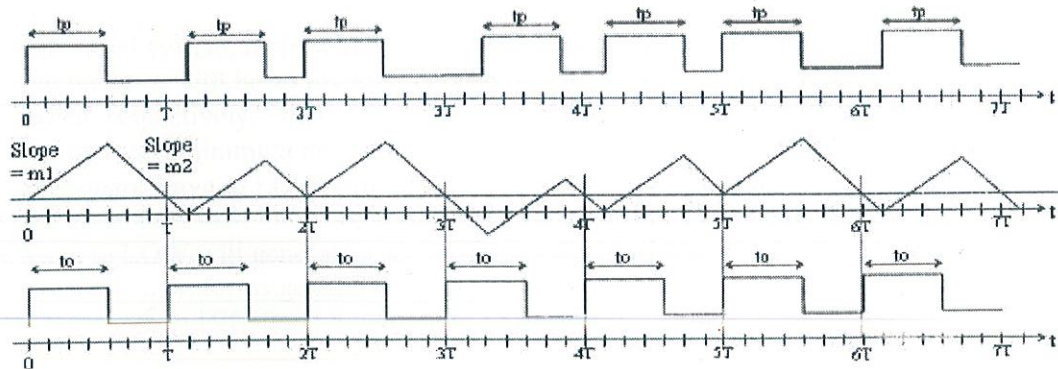


Fig 4.2



Raising or lowering of the threshold can cause the system to be more likely to fail. The fourth pulse is missed because there was too much jitter on the input and the saw tooth never was able to rise above the threshold value during the period  $3T$  to  $4T$ . If the threshold was lowered below the DC average, there would be the chance that the system would fail at time  $2T$  and at time  $5T$  where there might be a chance that the saw tooth never got above the threshold.

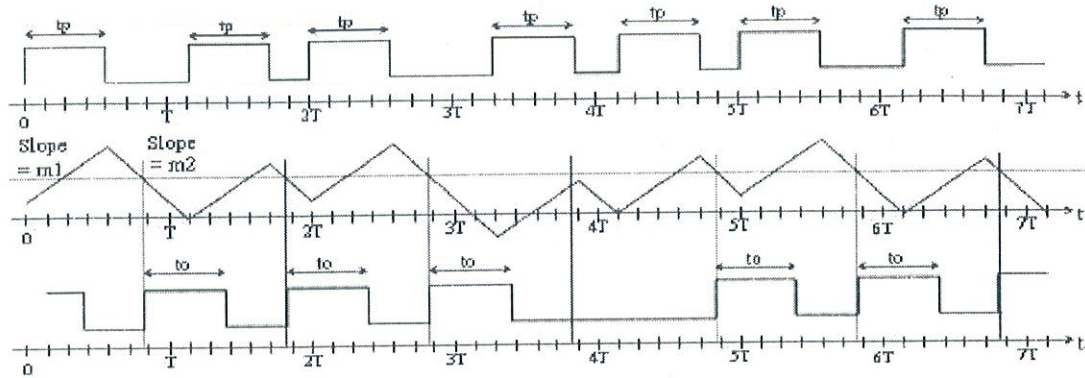


Fig 4.3

#### ON RAISING THE THRESHOLD

A change in threshold will move the beginning of the period by the value shown by

### 4.2 The Differential JAC System

In the differential system, there will be two square wave inputs; One will be high for  $t_p$ , and the other will be an inverted version that is low for  $t_p$ . These input waveforms will be called, respectively, SquareWave  $t_p$ HIGH and SquareWave  $t_p$ LOW and will have the same maximum and minimum amplitude values. The sawtooths generated by the SquareWave  $t_p$ HIGH and SquareWave  $t_p$ LOW will be inverted versions of each other also. SquareWave  $t_p$ HIGH will generate a sawtooth waveform which falls for time  $t_p$  and rises for  $T - t_p$ . SquareWave  $t_p$ LOW will generate a sawtooth waveform which rises for time  $t_p$  and falls for  $T - t_p$ . The sawtooth waveforms generated by SquareWave  $t_p$ HIGH and SquareWave  $t_p$ LOW will be called Sawtooth  $t_p$ HIGH and Sawtooth  $t_p$ LOW.

In the differential version, an output pulse is generated when the falling slope edge of the negative sawtooth crosses the rising slope edge of the positive sawtooth. Where these two signals cross becomes the differential system's threshold.

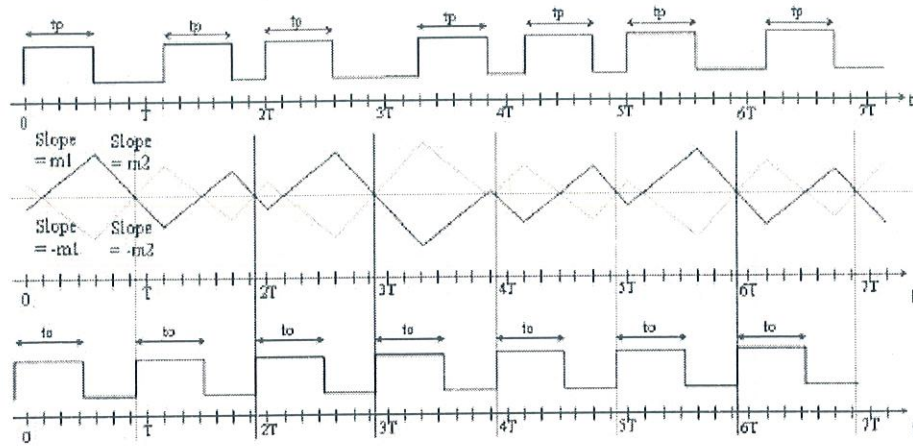


Fig 4.4

### 4.3 The JAC System

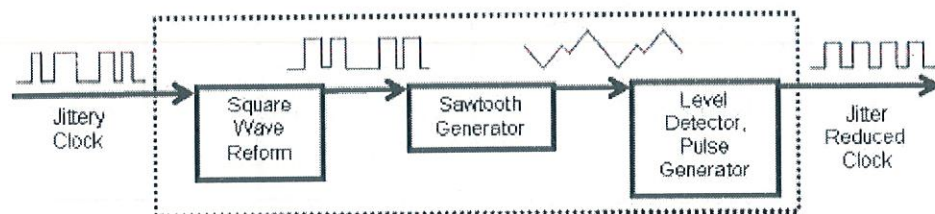


Fig 4.5



## Chapter 5: Implementation of Real time system

### 5.1 Flow Chart

The flow chart below shows the various steps in implementing the eye diagrams on mat lab.

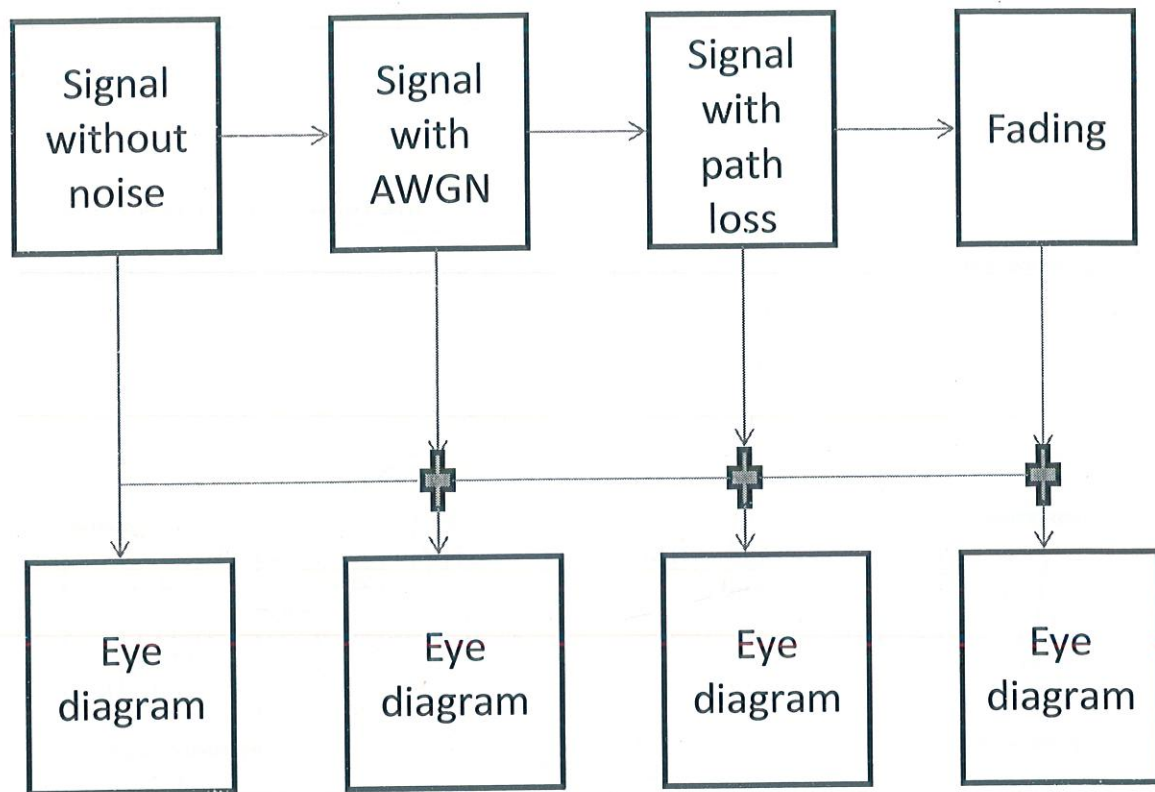


Fig 5.1

### 5.2 Path loss

#### 5.2.1 Introduction

- Path loss is the reduction in power density of an electromagnetic wave as it travels through space.
- Path loss may be due to free space loss, refraction, diffraction, reflection, aperture-medium coupling loss and absorption.

### 5.2.2 Path loss friis equation

$$L = 20 \log_{10} \left( \frac{4\pi d}{\lambda} \right)$$

- Where  $L$  is the path loss in decibels.
- $\lambda$  is the wavelength .
- $d$  is the transmitter-receiver distance in the same units as the wavelength.

### 5.2.3 Path Loss Diagram

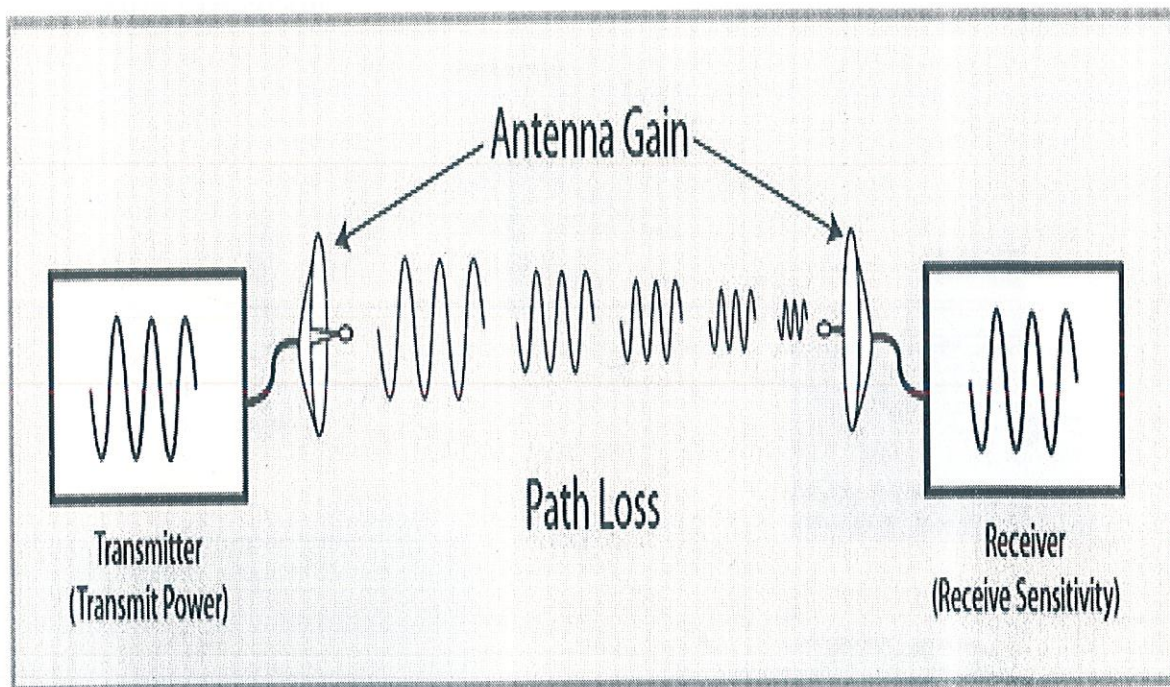


Fig 5.2



## 5.3 Fading

### 5.3.1 Introduction

- In wireless communications, **fading** is deviation of the attenuation affecting a signal over certain propagation media.
- **Fading** can be due to shadowing from obstacles affecting the wave propagation, sometimes referred to as **shadow fading**.
- Fading can cause poor performance in a communication system because it can result in a loss of signal power without reducing the power of the noise. This signal loss can be over some or all of the signal bandwidth.

### 5.3.2 Fading Diagram

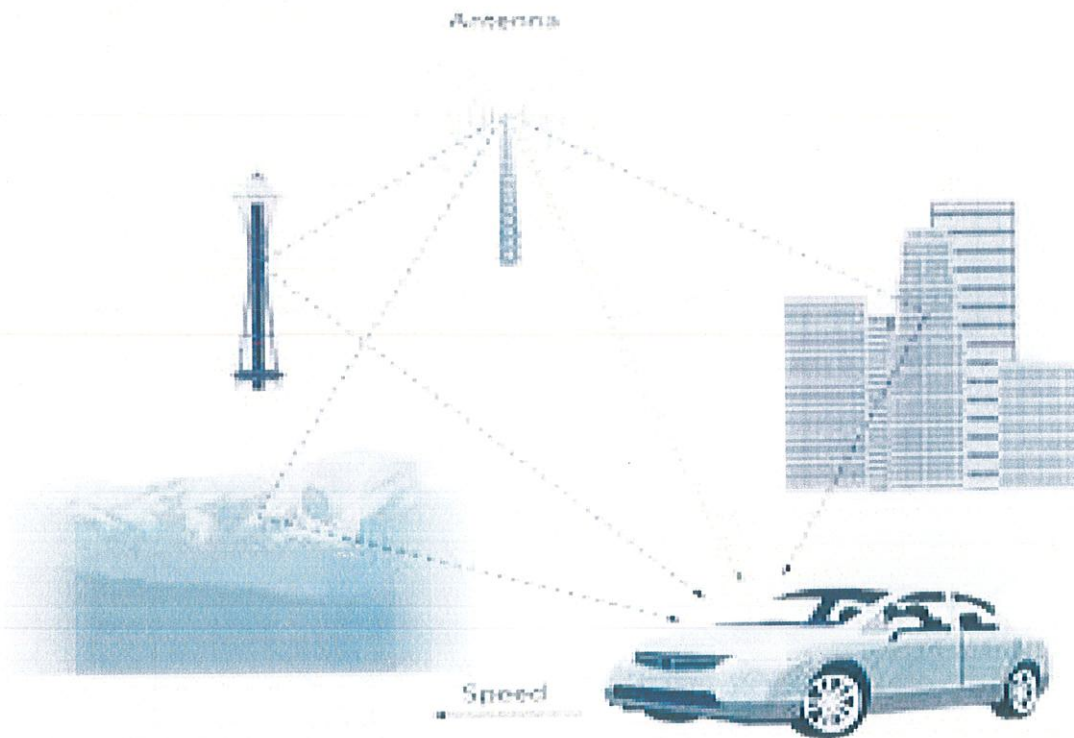


Fig 5.3

## Chapter 6: Eye diagrams implementation on matlab

### 6.1 EYE DIAGRAM BASIC

```
clc;  
clearall;  
t=0:.01:40;  
x=square(t,50);  
plot(x);  
Eyediagram(x,2);
```

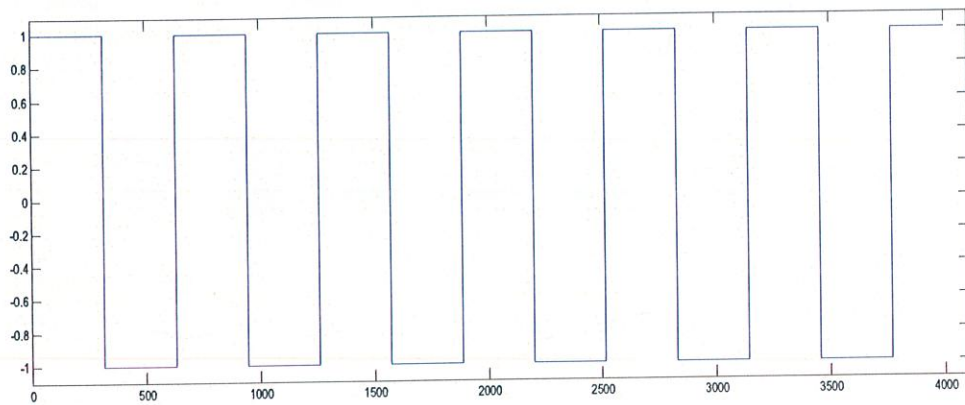


Fig 6.1

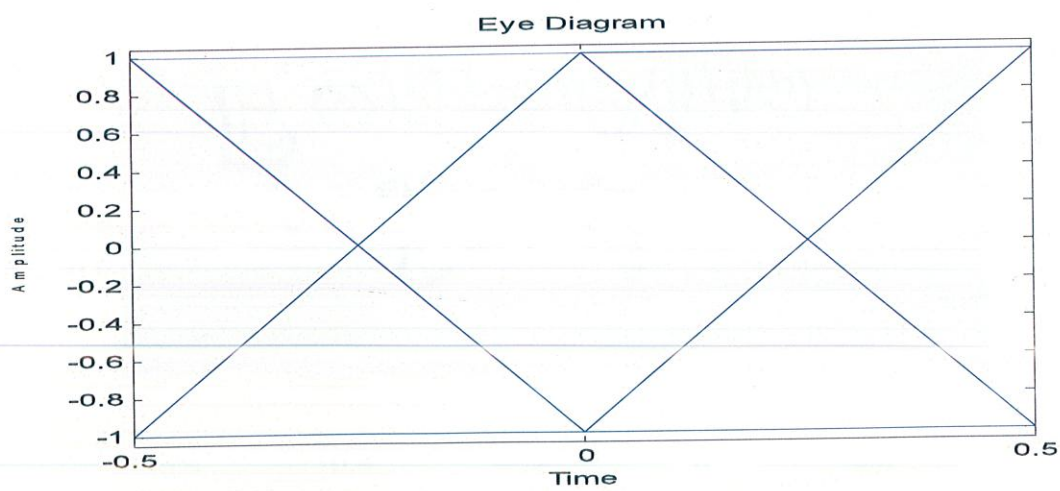


Fig 6.2



## 6.2 EYE DIAGRAM WITH AWGN (10 SNR)

```
clc;  
clearall;  
t=0:.01:40;  
x=square(t,50);  
y=awgn(x,10);  
plot(y);  
eyediagram(y,3);
```

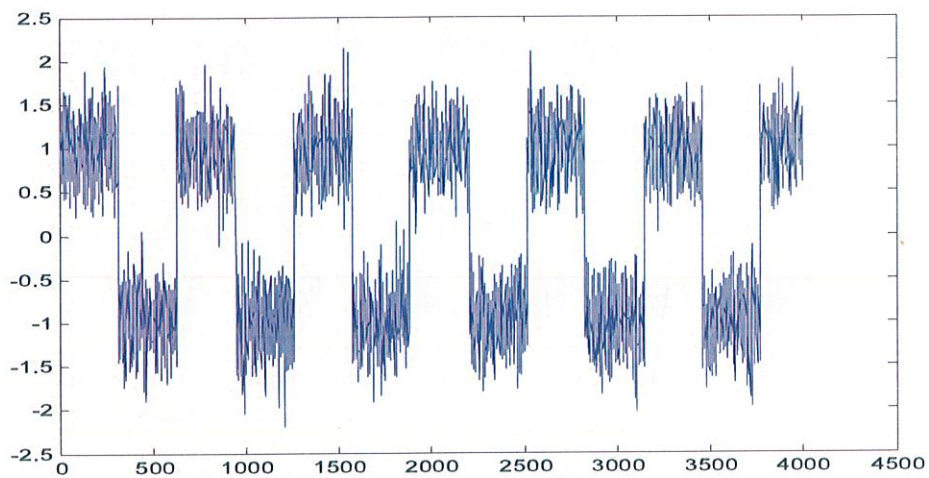


Fig 6.3

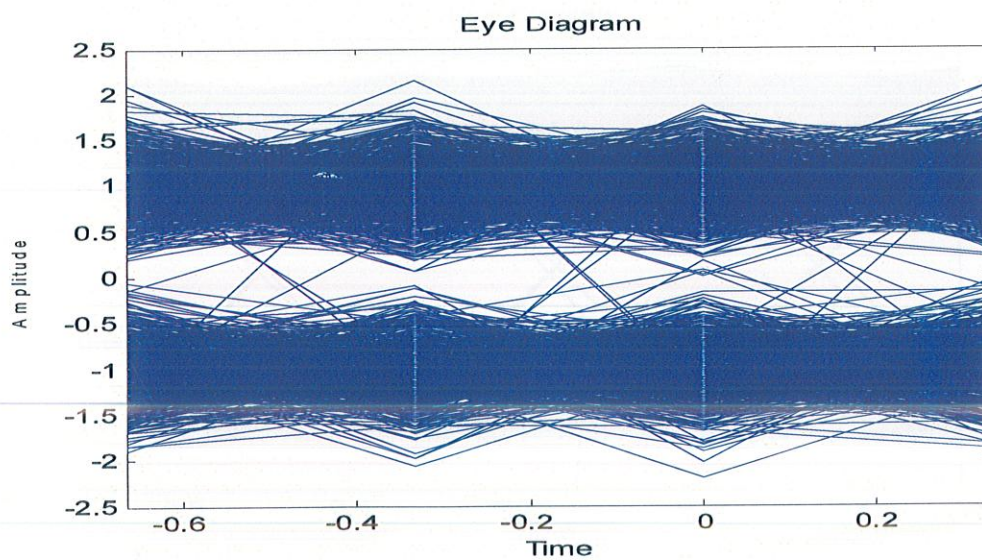


Fig 6.4

### 6.3 EYE DIAGRAM WITH AWGN(20 SNR)

```
clc;  
clearall;  
t=0:.01:40;  
x=square(t,50);  
y=awgn(x,20);  
plot(y);  
eyediagram(y,3);
```

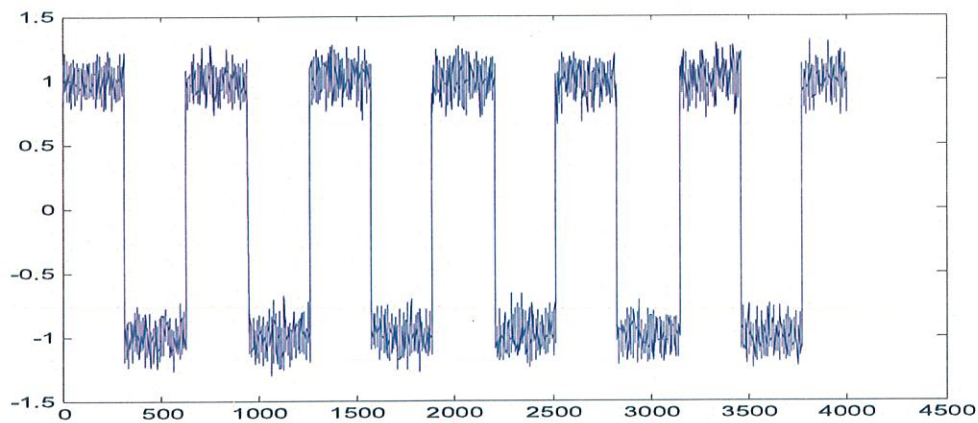


Fig 6.5

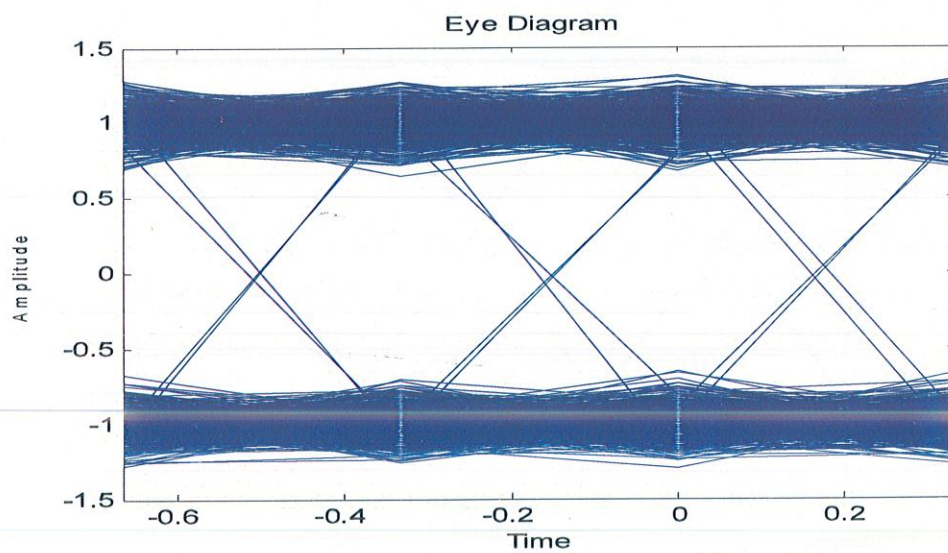


Fig 6.6



## 6.4 EYE DIAGRAM WITH AWGN (40 SNR)

```
clc;  
clearall  
t=0:.01:40;  
x=square(t,50);  
y=awgn(x,40);  
plot(y);  
eyediagram(y,3);
```

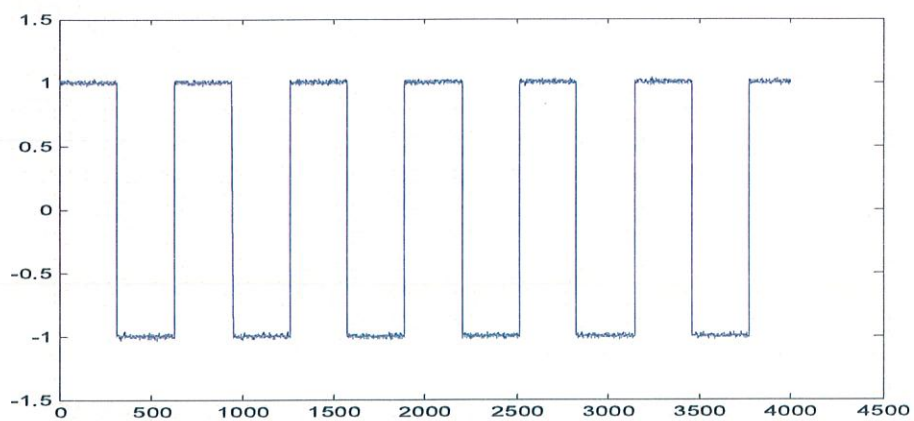


Fig 6.7

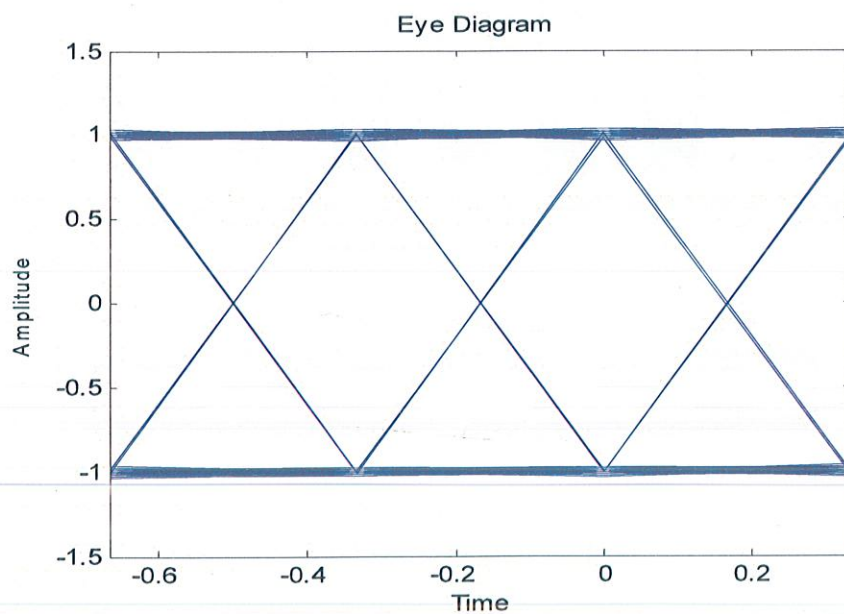


Fig 6.8

## 6.5 Signal with AWGN and pathloss and fading

```
clc;
clear all;
t=0:.01:40;lambda=33.3;tgtrng=100;
x=square(t,50);
y=awgn(x,20);
Loss = pow2db((4*pi*tgtrng/lambda)^2);
w=y+Loss;
c = rayleighchan(1/1000000,2);
v = filter(c,w);
eyediagram(x,2);
eyediagram(y,2);
eyediagram(w,2);
eyediagram(v,2)
```

### 6.5 .1 Signal with AWGN and pathloss

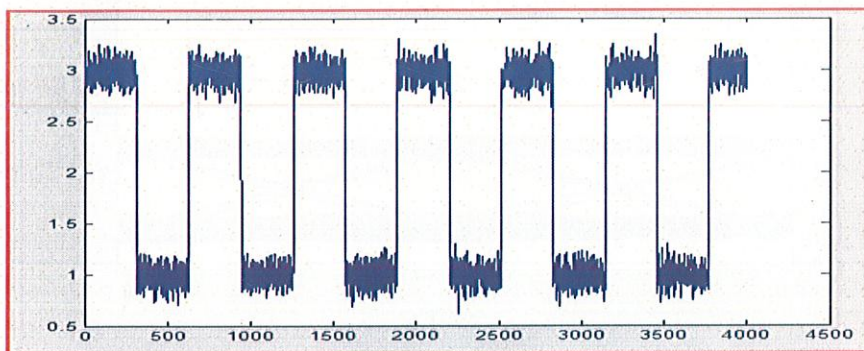


Fig 6.9

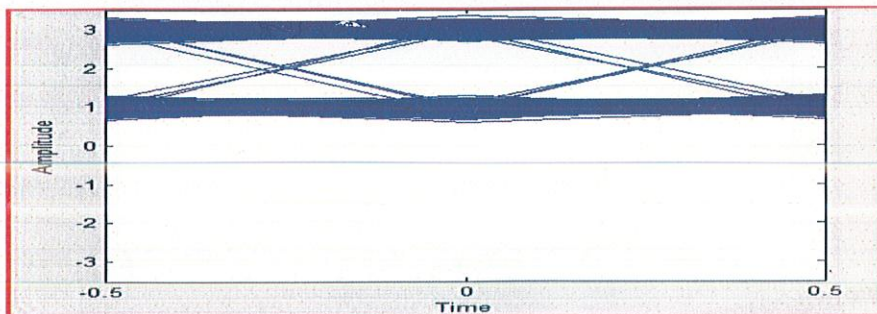


Fig 6.10



### 6.5.2 Signal with AWGN and pathloss and fading

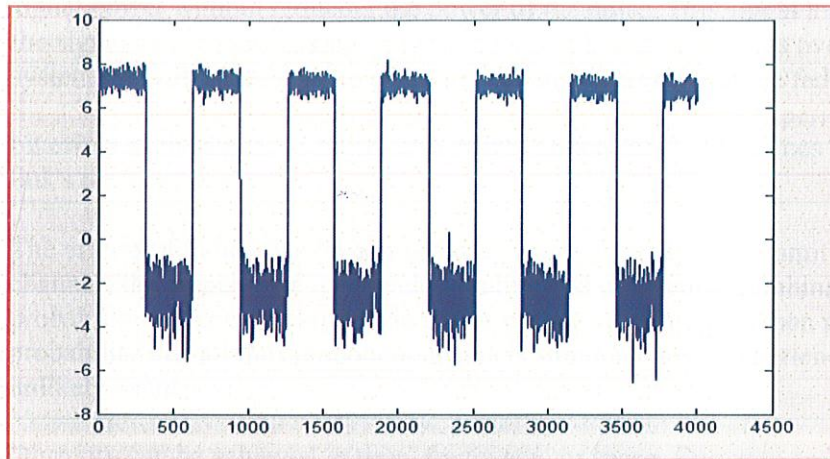


Fig 6.11

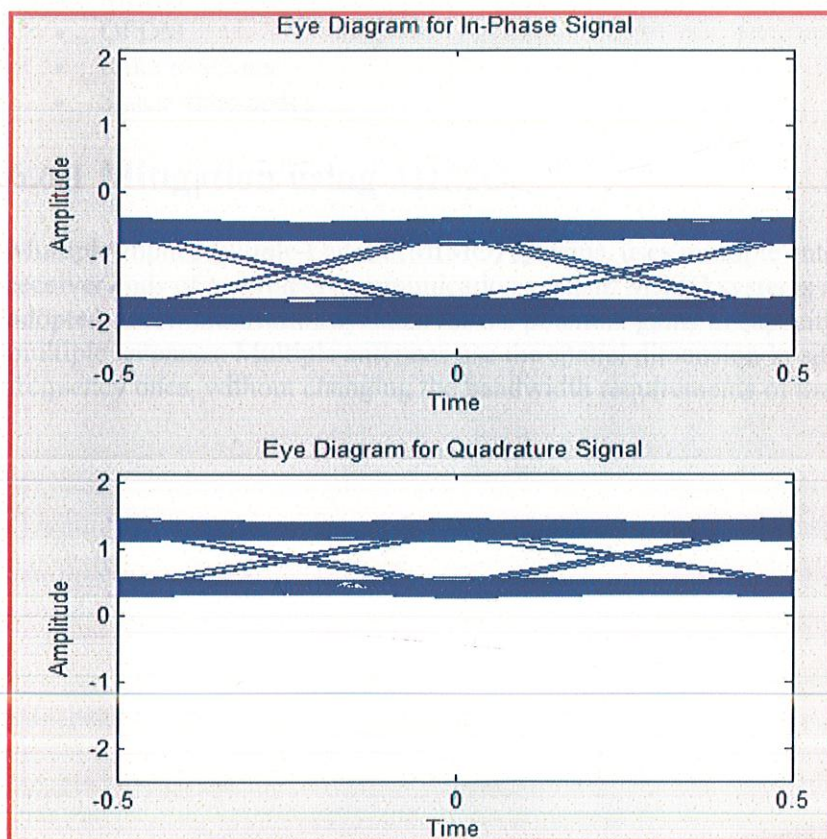


Fig 6.12

## 6.6. Mitigation

Fading can cause poor performance in a communication system because it can result in a loss of signal power without reducing the power of the noise. This signal loss can be over some or all of the signal bandwidth. Fading can also be a problem as it changes over time: communication systems are often designed to adapt to such impairments, but the fading can change faster than the adaptations can be made. In such cases, the probability of experiencing a fade (and associated bit errors as the signal-to-noise ratio drops) on the channel becomes the limiting factor in the link's performance.

The effects of fading can be combated by using diversity to transmit the signal over multiple channels that experience independent fading and coherently combining them at the receiver. The probability of experiencing a fade in this composite channel is then proportional to the probability that all the component channels simultaneously experience a fade, a much more unlikely event.

Diversity can be achieved in time, frequency, or space. Common techniques used to overcome signal fading include:

- Diversity reception and transmission
- MIMO
- OFDM
- Rake receivers
- Space-time codes

### 6.6.1 Mitigation using MIMO

Multiple-Input-Multiple-Output (MIMO) systems, uses multiple antennas at the transmitter and receiver ends of a wireless communication system. MIMO systems are increasingly being adopted in communication systems for the potential gains in capacity they realize when using multiple antennas. Multiple antennas use the spatial dimension in addition to the time and frequency ones, without changing the bandwidth requirements of the system.



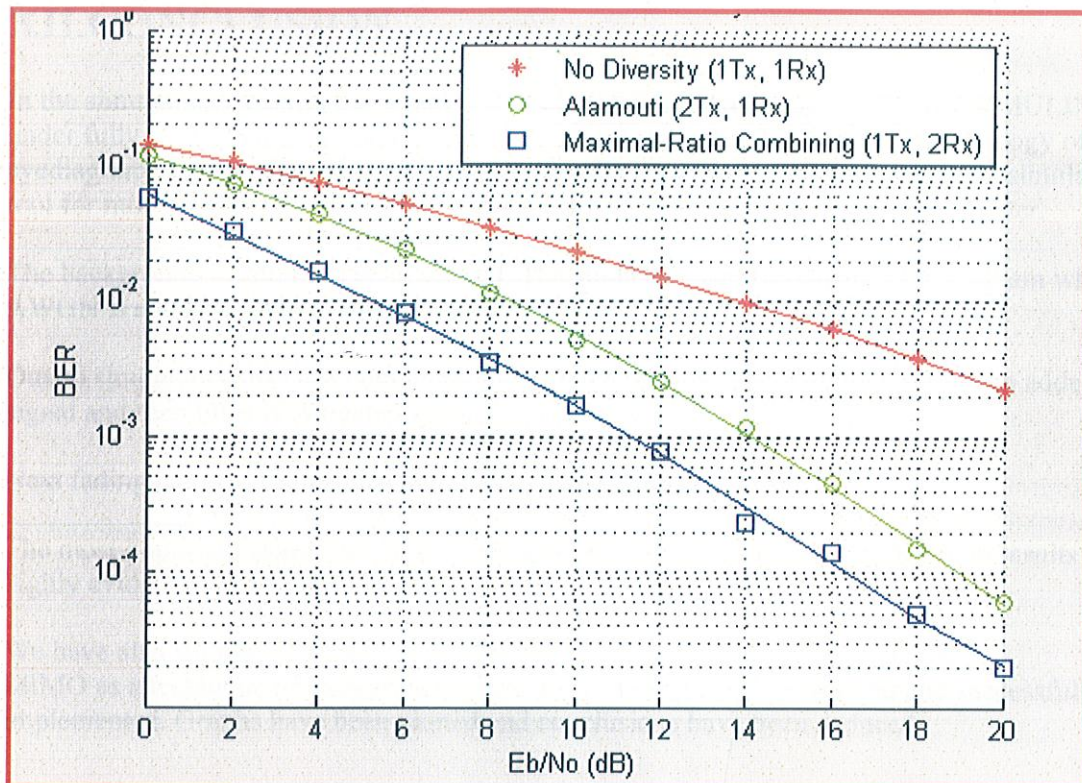


Fig 6.13

The resulting simulation results show that using two transmit antennas and one receive antenna provides the same diversity order as the maximal-ratio combined (MRC) system of one transmit antenna and two receive antennas.

Also observe that transmit diversity has a 3 dB disadvantage when compared to MRC receive diversity. This is because we modelled the total transmitted power to be the same in both cases. If we calibrate the transmitted power such that the received power for these two cases is the same, then the performance would be identical.

## **XII.CONCLUSION**

In the simulation scenario, the signal is first ideally simulated using MATLAB/ SIMULINK under fully controlled environments .We have studied basic definition and terminology of eyediagram with the help of MATLAB. The results show that MATLAB is a good simulation tool for modeling and analyzing eye diagrams which help in the measurement of jitter.

The background of jitter has been studied. The study of Characteristics of eye diagram when AWGN is added to signal is done.

Due to simple formulas and computational efficiency, noise and path loss have been added to the signal and then jitter is evaluated using eye diagrams.

Next fading has also been added and then eye diagram is evaluated.

The most important aspect has been to mitigate the fading on MATLAB, in which results are highly evident in MATLAB.

We have also studied various jitter attenuation circuits available and a basic JAC. MIMO as a technique of mitigation of jitter due to fading has been studied and successfully implemented. Graphs have been plotted and conclusions have been deduced.



### **XIII.FUTURE WORK**

- 1) Implementation of other mitigation techniques apart from MIMO.
- 2) Design of a basic jitter attenuation circuit.

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