IMPLEMENTATION OF CMOS CURRENT FEEDBACK MILLER COMPENSATED OPERATIONAL AMPLIFIER

Project report submitted in partial fulfillment of the requirement for the degree of

Bachelor of Technology

in

ELECTRONICS AND COMMUNICATION ENGINEERING

under the Supervision of

Dr. Shruti Jain

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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

WAKNAGHAT

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

WAKNAGHAT, SOLAN – 173234, HIMACHAL PRADESH

CERTIFICATE

This is to certify that project report entitled "**Implementation of CMOS current feedback Miller compensated operational amplifier**", submitted by Ankur Agrawal (091004), Abhimanyu Gupta (091006) and Arpit Kuthiala (091011) in partial fulfillment for the award of degree of Bachelor of Technology in Electronics and Communication Engineering to Jaypee University of Information Technology, Waknaghat, Solan has been carried out under my supervision.

This work has not been submitted partially or fully to any other University or Institute for the award of this or any other degree or diploma.

Date: 30/5/13

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ACKNOWLEDGEMENT

Knowledge, energy and time are the resources in the completion of this project but the most requisite is the proper guidance of our respected mentor, **Dr. Shruti Jain**, to whom we extend the sincere vote of thanks, for her invaluable co-operation and help, throughout the project. She acted as a constant source of motivation and support throughout the development stage of the project.

We would also like to thank all the panel members for their valuable suggestions and guidance in all the seminars and viva-voce during evaluation.

We also express our obligation to all people who helped us directly or indirectly in the completion of this project.

Our series of gratitude will certainly be incomplete if we do not thank our parents and friends who have always been on the supporting side in our entire thick and thins.

In spite of our best efforts, some mistakes must have crept in.

I shall be thankful to anyone who brings it to our concerned notice. Suggestion for improvement is welcomed.

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LIST OF ABBREVIATIONS

ACRONYM	STANDS FOR
Op-Amp	Operational Amplifier
ac	Alternating Current
dc	Direct Current
w.r.t	With Respect To
Vss	Source voltage
Vout	Output voltage
Vin	Input Voltage
Rf	Feedback Resistance
Rg	Ground Resistance
Ad	Differential Gain
Ac	Common Mode Gain
VFB	Voltage Feedback
CFB	Current Feedback
SR	Slew Rate
BJT	Bi-Polar Junction Transistor
P-SPICE	Personal Simulation Program with Integrated Circuit Emphasis
CMRR	Common Mode Rejection Ratio
dB	Decibels
T	Tera
VFOA	Voltage Feedback Operational Amplifier
CMOS	Complementary Metal Oxide Semiconductor
Meg	Mega
CFOA	Current Feedback Operational Amplifier

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ABSTRACT

An operational amplifier, or an op-amp, is a very high gain differential amplifier with high input impedance and low output impedance. Typical uses of the operational amplifier are to provide voltage amplitude changes (amplitude and polarity), oscillators, filter circuits and many types of instrumentation circuits. An op-amp contains a number of differential amplifier stages to achieve a very high voltage gain. In this project, we have investigated the internal architecture of an op-amp using BJT and CMOS and divided the operation of an op-amp into 4 stages. We have also revealed that change in the architecture of any of the stage has an impact on the basic parameters of the op-amp.

We have also tried to propose some new models with improved Gain, CMRR and Slew Rate and compared the proposed architectural design with the existing design of op-amp.

Also the effect of change of output resistance and feedback resistance on the gain, CMRR and slew rate has been measured and hence the most optimum value of resistances has been chosen for the design procedure. The designed op-amp circuits were operated for both voltage as well as current feedback. Finally, we did the AC analysis of the op-amp circuit and plotted the Bode plot and Nyquist plot for the op-amp circuits to figure out the band of frequencies where the gain is maximum and the break-off frequency of the op-amp. As op-amp are the building blocks of linear integrated electronics, therefore proposing newer design models for op-amp with improved parameters is an important landmark in electronics industry in hunt for a faster and efficient design.

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OPERATIONAL AMPLIFIERS

Linear integrated circuits are being used in a number of electronic applications such as in fields like audio and radio communication, medical electronics, instrumentation control etc.

An important linear integrated circuit is Op-Amp also called an Operational Amplifier. An OP-Amp is a direct-coupled high gain amplifier usually consisting of one or more differential amplifier and usually followed by a level translator and an output stage. The output stage is generally a push-pull pair. An OP-Amp is used to amplify both "ac" as well as "dc" signals.

1.1 BLOCK DIAGRAM OF A TYPICAL OP-AMP:

The block diagram of an Op-Amp essentially consists of 4 stages. The input to the Op-Amp passes through all these 4 stages before the output is finally received.

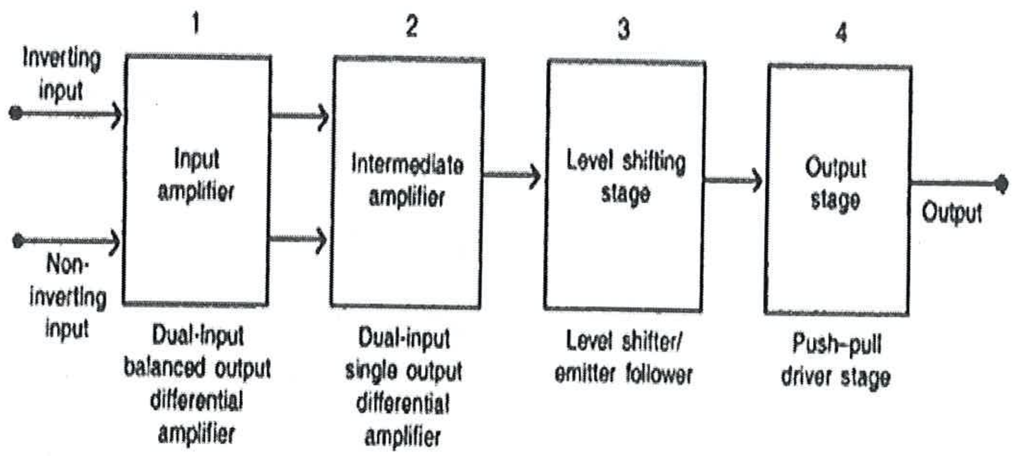

Figure 1 Block Diagram of a Typical Op-Amp

- ## INPUT STAGE :

  The input-stage is the dual-input, balanced-output differential amplifier. This stage generally provides most of the voltage gain of the amplifier and also establishes the input resistance of the Op-Amp.

- ## INTERMEDIATE STAGE :

  The intermediate stage is usually another differential amplifier, which is driven by the output of the first stage. In most amplifiers, the intermediate stage is dual input, unbalanced output.

- ## LEVEL SHIFTING STAGE :

  The level translator is used after the intermediate stage to shift the DC level at an output of the intermediate stage downward to zero volts w.r.t the ground.

- ## OUTPUT STAGE :

  The final stage is usually a complementary push-pull stage amplifier output stage. The output stage increases the output voltage swing and raises the current supplying capability of the Op-Amp.

1.2 SCHEMATIC SYMBOL OF AN OP-AMP :

The schematic diagram of an Op-Amp is given below. The input is provided at pin 2 and pin 3 and the output is obtained at pin 6. The source voltages are provided at pin 4 and 7.

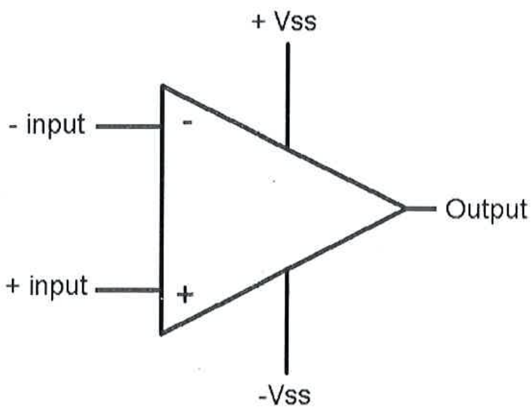

Figure 2 Schematic symbol of an Op-Amp

1.2.1 The Golden Rules

- The voltage difference between the inputs, V+, V- is zero.
- The inputs draw no current.

1.3 EQUIVALENT CIRCUIT OF AN OP-AMP :

The equivalent circuit of an Op-Amp is shown below

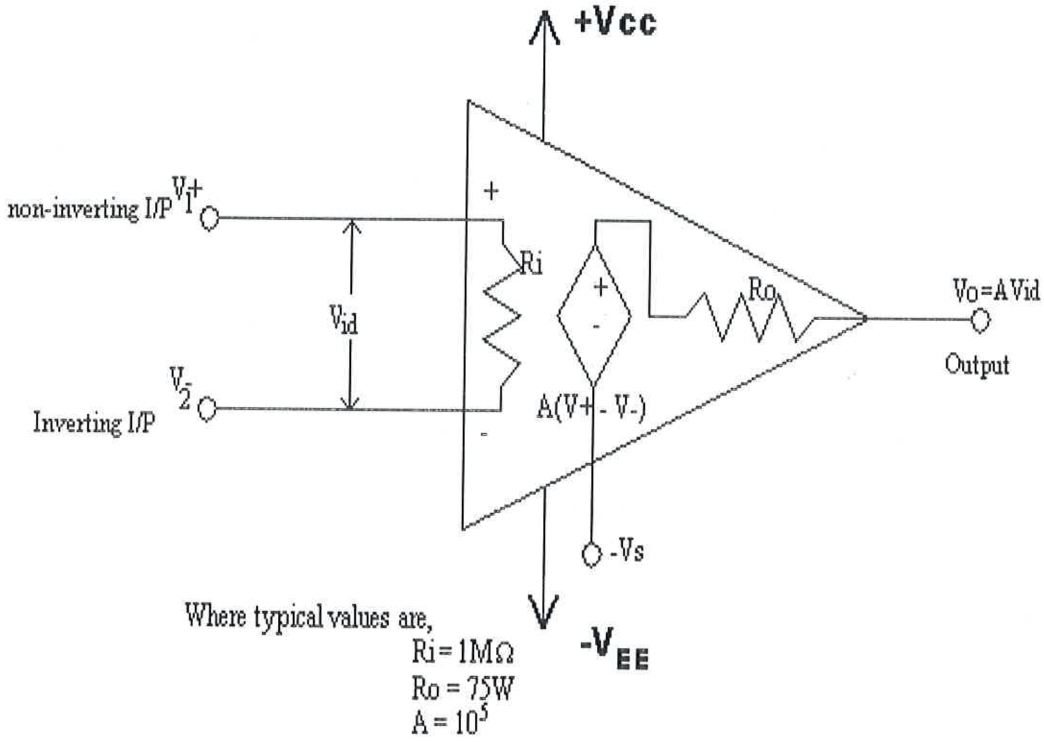

Figure 3 Equivalent circuit of an Op-Amp

The output voltage is given as :

$$V_o = A.V_{id} = A(V_1^+ + V_2^-)$$

Where

A= large scale voltage-gain.

V_{id} = difference input voltage.

From the above equation, it is clear that the Op-Amp amplifies only the difference between the two inputs, not the voltage itself. The polarity of the output depends on the polarity of the input voltage.

1.4 OP-AMP CONFIGURATIONS :

For a basic op-amp, the following three configurations are possible

- Non-Inverting amplifier.
- Inverting amplifier.
- Differential amplifier.

1.4.1 Non-Inverting Amplifier :

The circuit diagram for the non-inverting configuration is given below

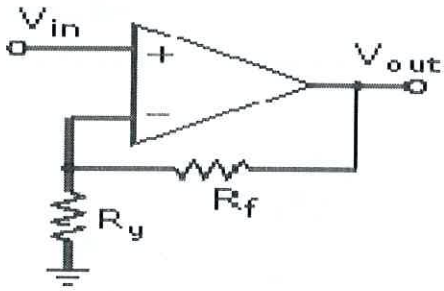

Figure 4 Non-Inverting Amplifier

The output voltage is given as

$$V_{OUT} = V_{IN}\left(1 + \frac{R_F}{R_G}\right)$$

where

R_F = Feedback resistance

R_G = Input resistance

V_{OUT} = Output voltage

V_{IN} = Input Voltage

1.4.2 Inverting Amplifier :

The circuit diagram for the non-inverting configuration is given below

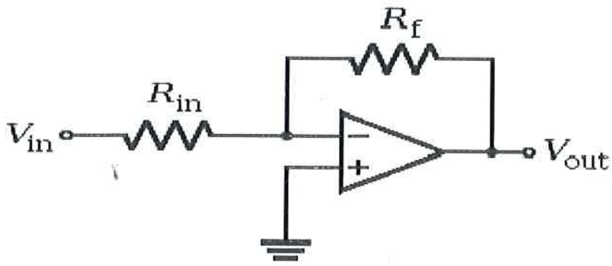

Figure 5 Inverting Amplifier

The output voltage is given as

$$V_{OUT} = V_{IN}\left(-\frac{R_F}{R_G}\right)$$

1.4.3 Differential Amplifier :

The circuit diagram for the non-inverting configuration is given below

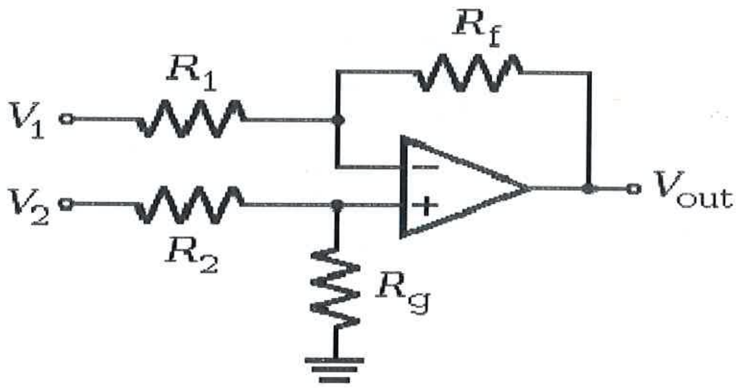

Figure 6 Differential Amplifier

The output voltage is given as

$$V_{OUT} = A_d\left(V_2 - V_1\right) + A_c\left(\frac{V_1 + V_2}{2}\right)$$

where

A_d = differential Voltage Gain

A_C = Common mode gain

2

FEEDBACK OPERATIONAL AMPLIFIERS

2.1 FEEDBACK

The block diagram of a basic voltage feedback circuit is as given below

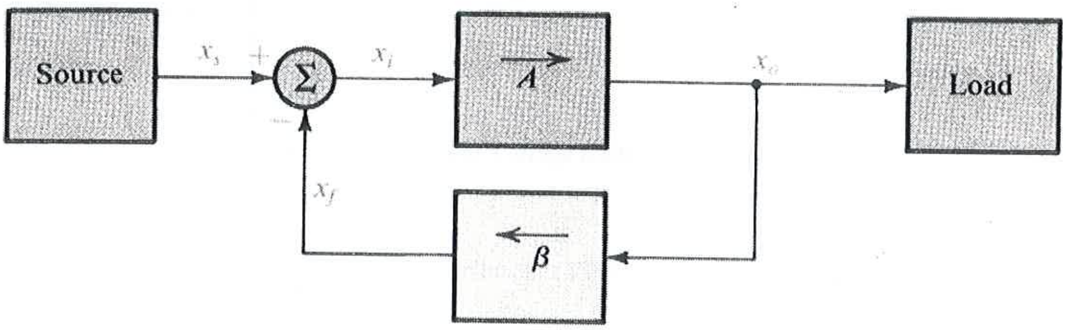

Figure 7 A Basic Voltage Feedback Network

2.2 INTRODUCTION :

Modern VFB use the same architecture as the CFB in order to reduce the power consumption while maintaining a large slew rate.

This architecture eliminates the dependency of the SR on the I_Q although at the cost of more circuitry.

This architecture will achieve almost as good a SR as an equivalent I_Q CFB. This approach will ensure a good matching between both inverting and non-inverting input of the amplifier restoring the typical VFB good.

2.3 VOLTAGE FEEDBACK OP-AMP BASICS

2.3.1 Voltage Feedback-Amp circuit symbol :

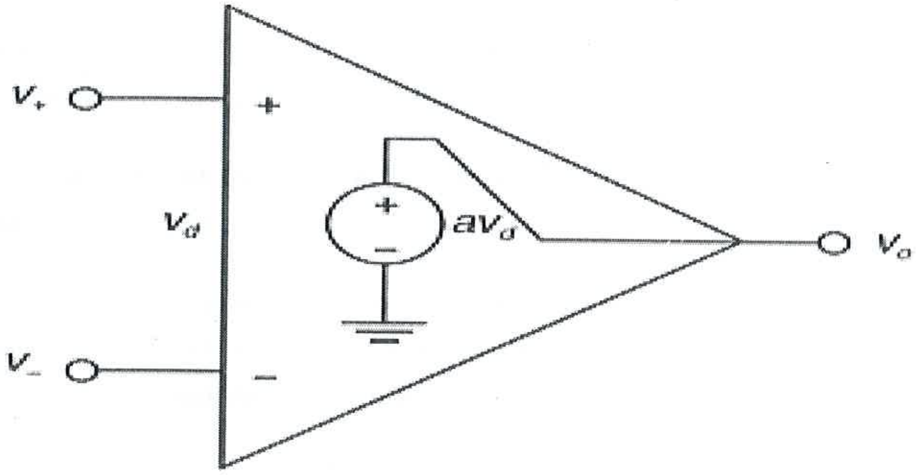

Figure 8 Circuit Symbol of Voltage feedback Op-Amp

The classic model of the **voltage feedback (VFB)** op amp has the following characteristics:

1. **Infinite input impedance**
2. **Infinite bandwidth**
3. **Infinite voltage gain**
4. **Zero output impedance**
5. **Zero power consumption**

None of these can be actually realized, of course. How close a real implementation comes to these ideals determines the quality of the op amp.

2.3.2 BASIC OPERATIONS :

First, we assume that there is a portion of the output that is fed back to the inverting terminal to establish the fixed gain for the amplifier. ***This is negative feedback.***

Any differential voltage across the input terminals of the op-amp is multiplied by the amplifier's open loop gain which is infinite for the ideal op-amp.

If the magnitude of this differential voltage is more positive on the inverting (–) terminal than on the non-inverting (+) terminal, ***the output will swing negative***.

If the magnitude of the differential voltage is more positive on the non-inverting (+) terminal than on the inverting (–) terminal, ***the output voltage will swing positive***.

The infinite open loop gain of the amplifier will attempt to force the differential input voltage to zero.

As long as the inputs and output stays in the operational range of the amplifier, it will keep the differential input voltage at zero, and the output will be the input voltage multiplied by the gain determined by the feedback network.

2.3.3 INVERTING AND NON-INVERTING CONFIGURATIONS

There are two basic ways configure the ideal voltage feedback op-amp as an amplifier.

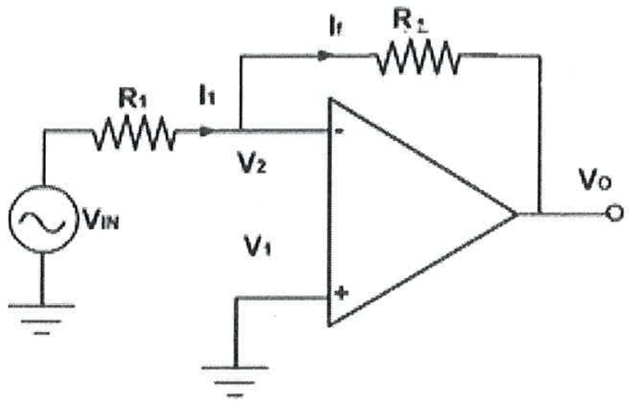

Figure 9 Inverting Op-Amp

Figure* 9** is known as the ***inverting configuration. With this circuit is out of phase with the input. The signal gain of this circuit is determined by the ratio of the resistors used and is given by:

$$G = - R_F/R$$

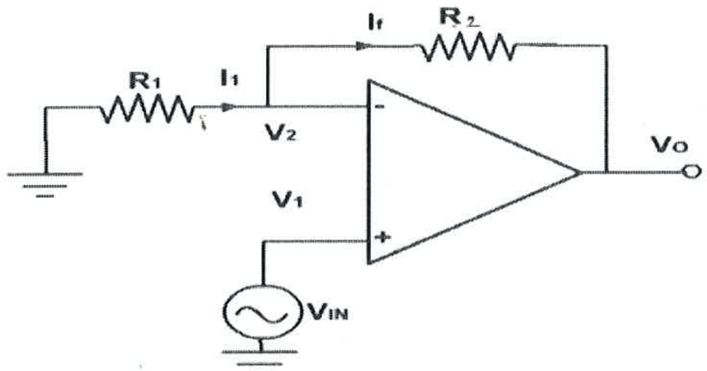

Figure 10 Non-Inverting Op-amp

Figure.*10** is known as the ***non-inverting configuration. With this circuit the output is in phase with the input. The signal gain of the circuit is also determined by the ratio of the resistors used and is given by:

$$\mathbf{G = 1 + R_F/R_G}$$

2.4 CURRENT FEEDBACK OPERATIONAL AMPLIFIER:

The block diagram of a basic current feedback circuit is as given below

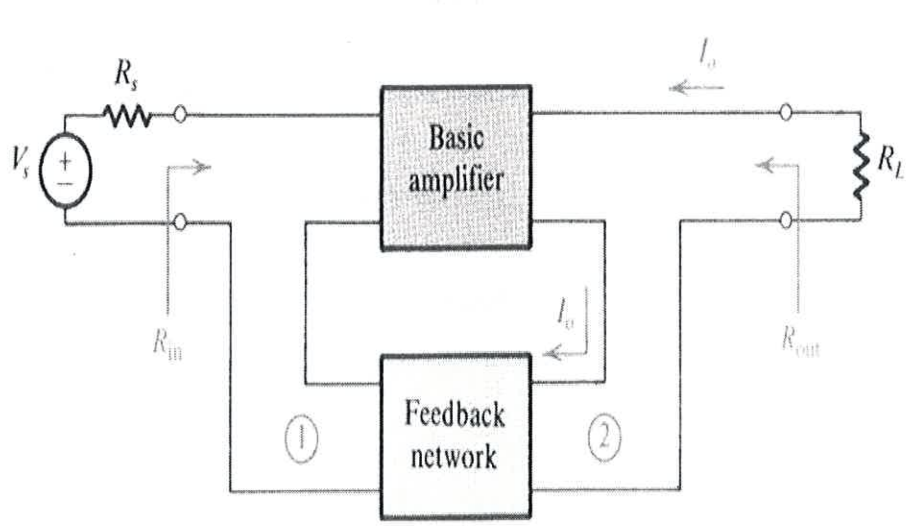

Figure 11 A basic Current Feedback Network

2.5 INTRODUCTION

Current-feedback amplifiers (CFA) do not have the traditional differential amplifier input structure, thus they sacrifice the parameter matching inherent to that structure. The CFA circuit configuration prevents them from obtaining the precision of voltage-feedback amplifiers (VFA), but the circuit configuration that sacrifices precision results in increased bandwidth and slew rate. The higher bandwidth is relatively independent of closed-loop gain, so the constant gain-bandwidth restriction applied to VFAs is removed for CFAs. The slew rate of CFAs is much improved from their counterpart VFAs because their structure enables the output stage to supply slewing current until the output reaches its final value.

In general, VFAs are used for precision and general purpose applications, while CFAs are restricted to high frequency applications above 100 MHz .

Although CFAs do not have the precision of their VFA counterparts, they are precise enough to be dc-coupled in video applications where dynamic range requirements are not severe. CFAs, unlike previous generation high-frequency amplifiers, have eliminated the ac coupling requirement; they are usually dc-coupled while they operate in the GHz range. CFAs have much faster slew rates than VFAs, so they have faster rise/fall times and less inter modulation distortion.

2.6 Current Feedback Amp Basics

2.6.1 Current Feedback Op-Amp Model:

The current feedback Op-Amp model is shown below

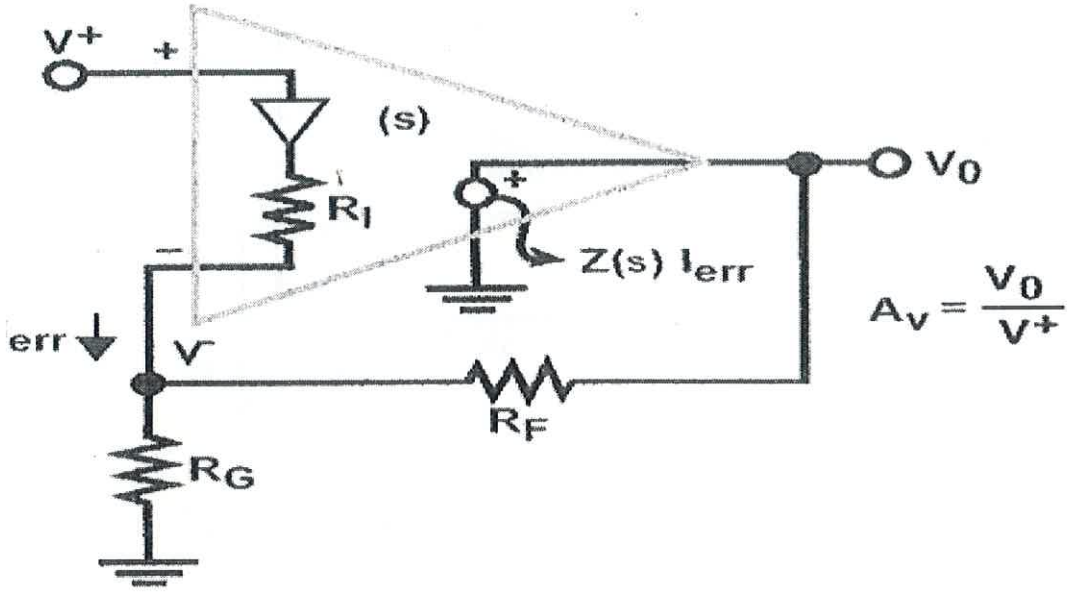

Figure 12 Current Feedback Op-Amp model

2.6.2 BASIC OPERATION

Current feedback op amps have an *input buffer* as opposed to a *differential pair*

1. The input buffer is most often an emitter follower or something very similar.
2. The non-inverting input is high impedance, while the buffer's output is low impedance.

The output of a current-feedback op amp is a voltage; it is related to the current that flows out of or into the inverting input of the op amp by a complex function called trans impedance, Z(s) which is a very high number at DC.

The current-feedback op amp's key flexibility is adjustable bandwidth and stability.

Because the feedback resistor value actually changes the AC loop dynamics of the amplifier, it can impact both the bandwidth and stability.

2.6.3 The Non-inverting Current Feedback Amp :

The non-inverting current feedback Amplifier circuit diagram is shown below

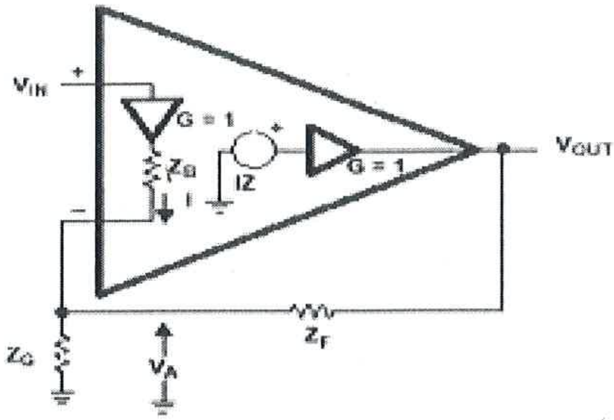

Figure 13 Non-Inverting CFA

$V_{out} = I\,Z$

$I = V_A / Z_G - [(V_{out} - V_A)/Z_F]$

$V_A = V_{in} - I\,Z_B$

$V_{out}/V_{in} = [1 + Z_F / Z_G] / [1 + Z_F / Z]$

$V_{out}/V_{in} = 1 + Z_F / Z_G$

The Inverting Current Feedback Amp :

The inverting current feedback Amplifier circuit diagram is shown below

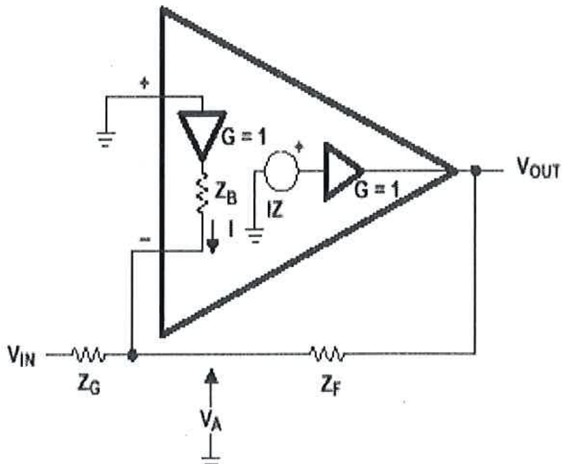

Figure 14 Inverting CFA

$I + [(V_{in} - V_A) / Z_G] = (V_A - V_{out}) / Z_F$

$I Z_B = -V_A$

$I Z = V_{out}$

$V_{out}/V_{in} = -[(1/Z_G) / (1/Z) + (1/Z_F)]$

$V_{out}/V_{in} = -Z_F / Z_G$

3

RESULTS AND DISCUSSIONS

3.1 VOLTAGE FEEDBACK OPERATIONAL AMPLIFIER USING BJT:

3.1.1 Circuit Design:-

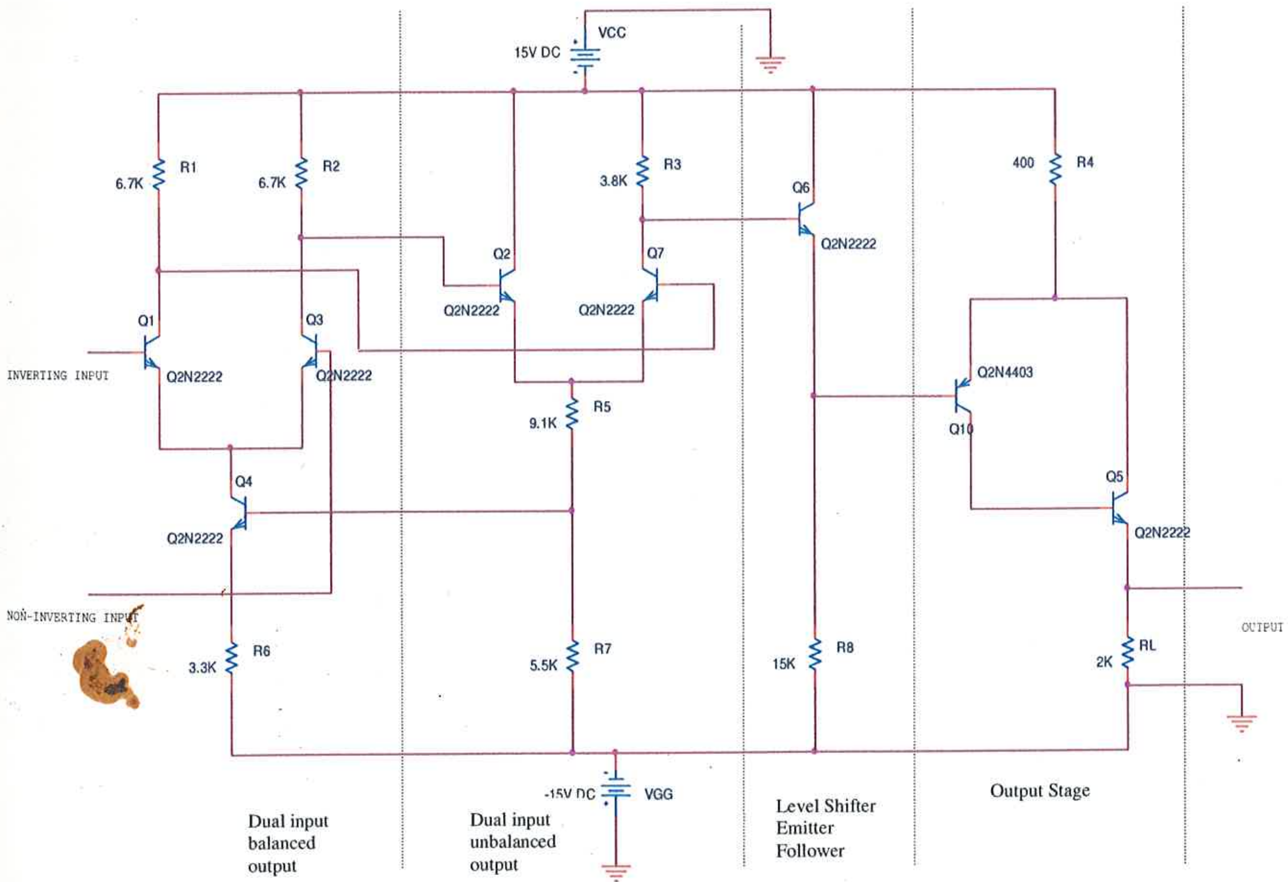

Figure 15 BJT Op-Amp circuit

The operation of a BJT op-amp has been divided into four stages. The input is provided at the base of two NPN transistors in Dual-Input Balanced Output stage and output id obtained using a push pull stage that uses a PNP and NPN transistor. The output in level shifter stage is taken across the emitter and hence the output is in phase with the input.

3.1.2 OUTPUT WAVEFORMS FOR VOLTAGE FEEDBACK BJT OP-AMP:

Using P-Spice software, the outputs for the BJT Voltage Feedback Op-Amp have been traced for the three basic Op-Amp configurations:-

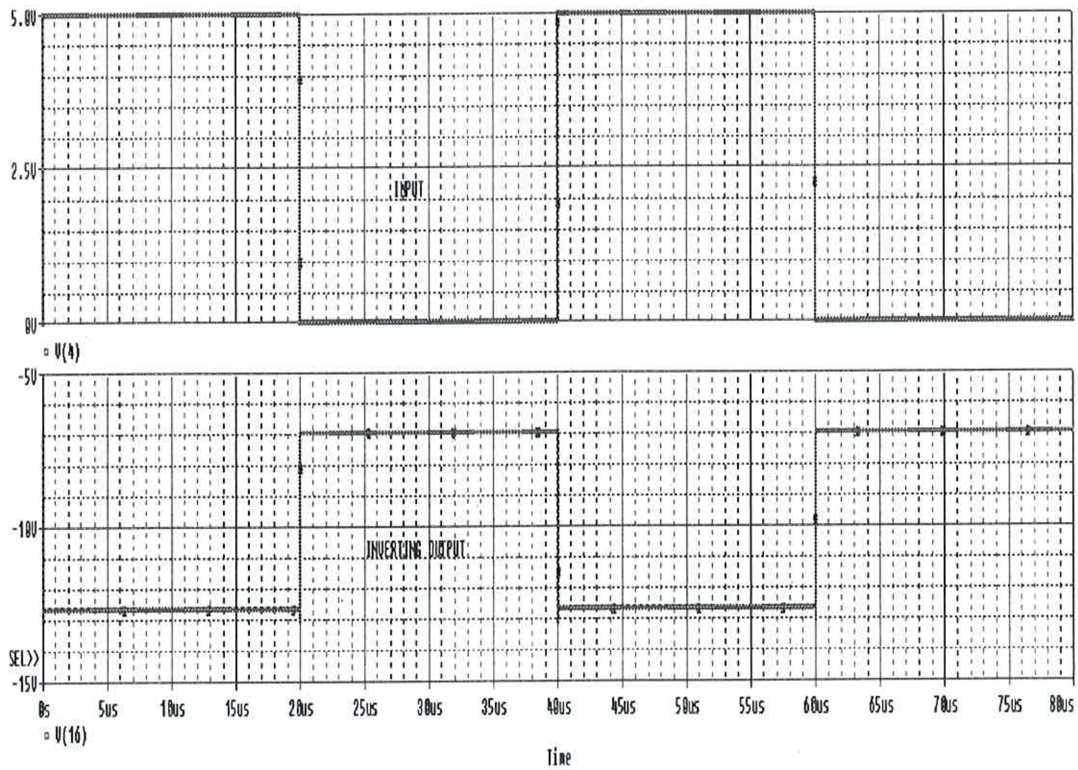

Figure 16 Inverted Output

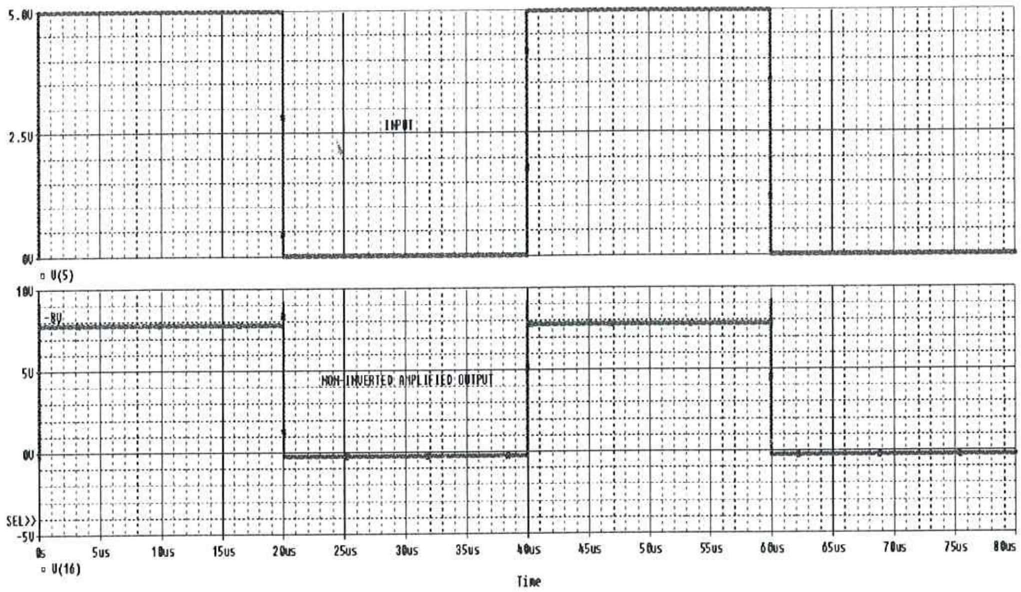

Figure 17 Non-Inverted Output

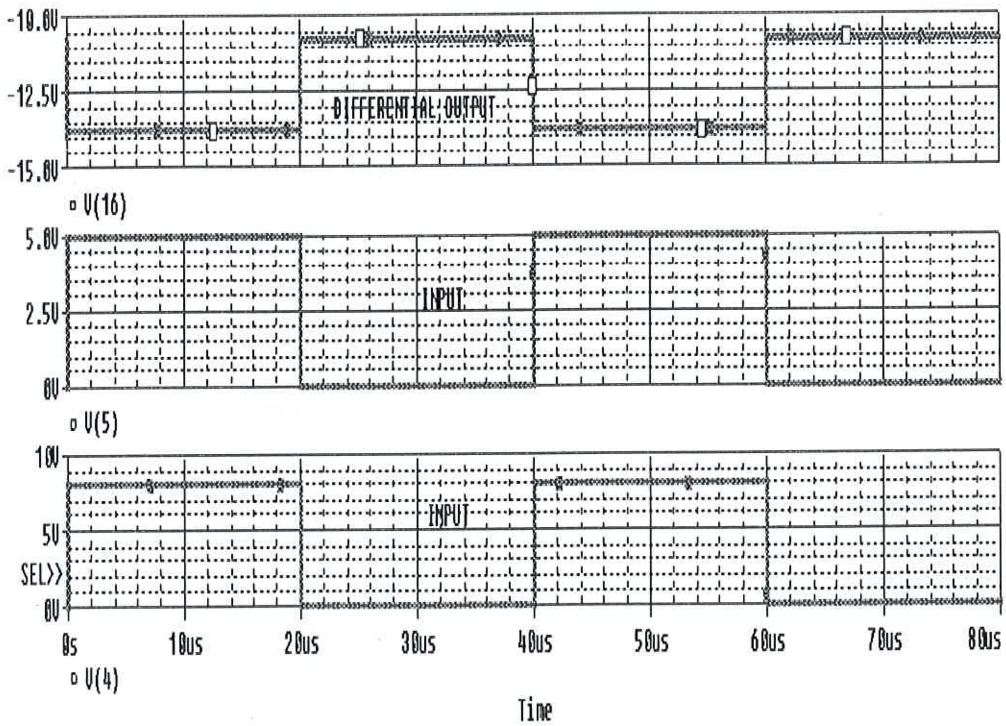

Figure 18 Differential Output

3.1.3 Circuit Design (Proposed):-

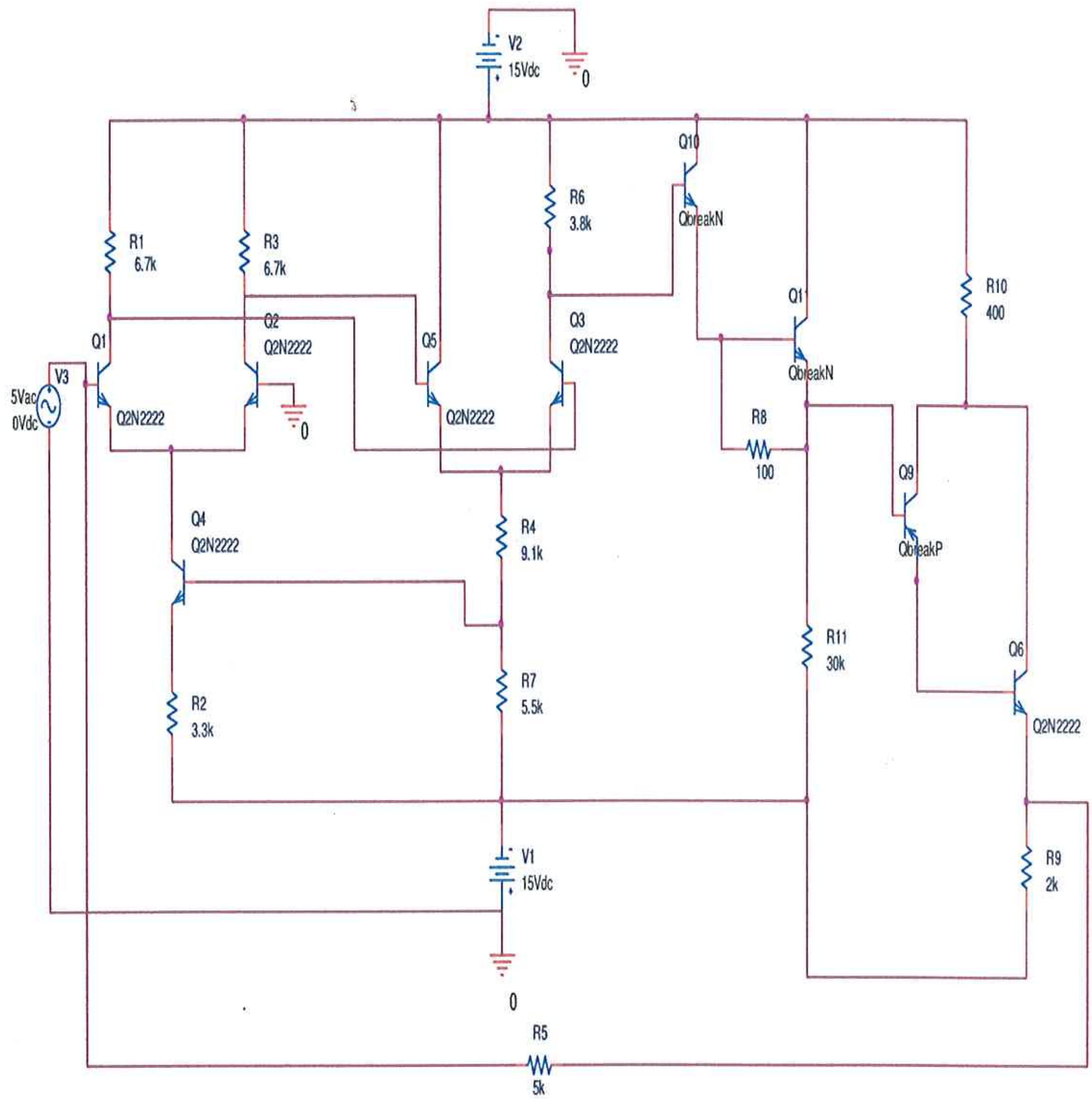

Figure 19 Proposed BJT Op-Amp Circuit

The circuit given above is the proposed model for high gain, improved CMRR and faster operation of BJT op-amp. The emitter follower stage is replaced by a cascaded network of BJT's so that the input to the stage passes through the cascaded setup of transistors and the output is more stable with higher gain value.

3.1.4 OUTPUT WAVEFORMS FOR PROPOSED VOLTAGE FEEDBACK BJT OP-AMP:

Using P-Spice software, the outputs for the proposed BJT Voltage Feedback Op-Amp have been traced for the three basic Op-Amp configurations:-

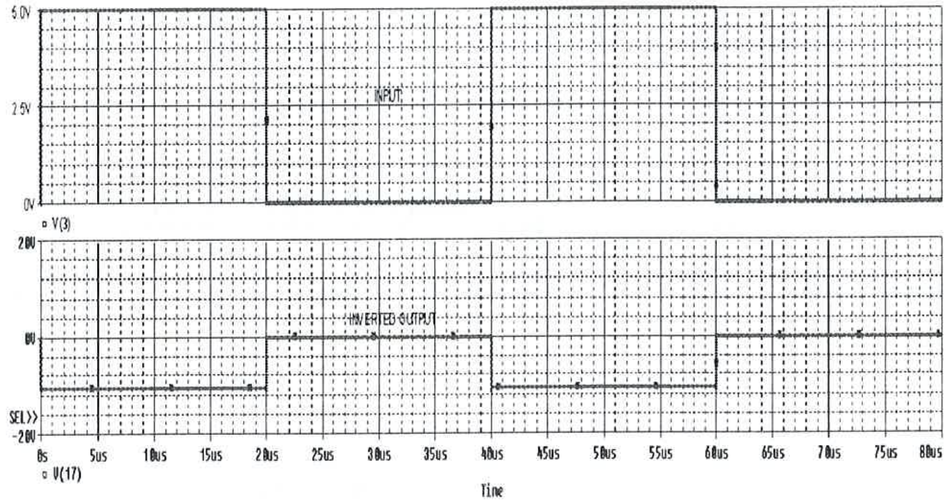

Figure 20 Inverted Output

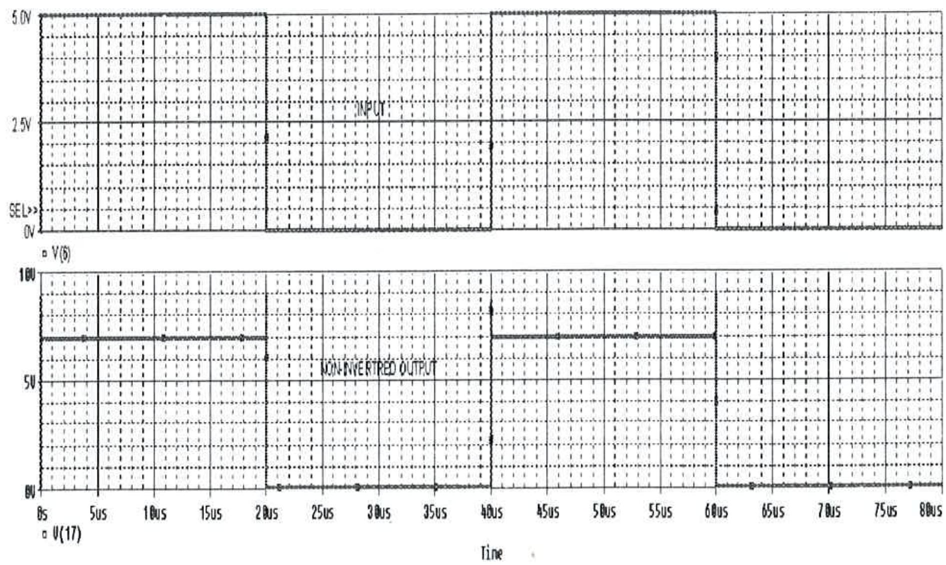

Figure 21 Non-Inverted Output

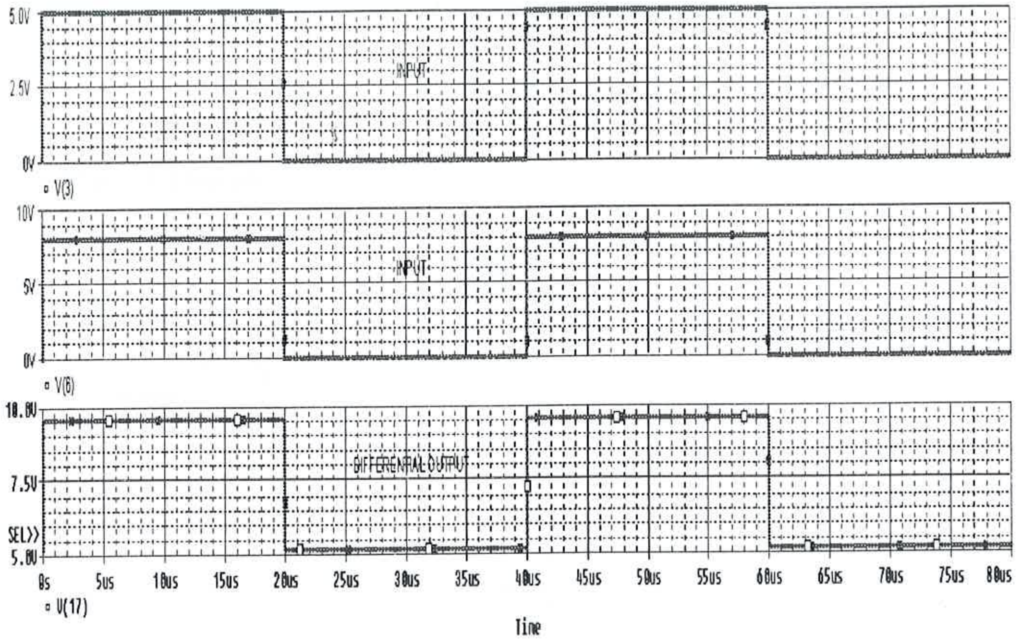

Figure 22 Differential Output

3.1.5 COMPARISON TABLE:

Given below is the comparison between the BJT voltage feedback circuit and proposed model. Various parameters such as CMRR, Slew Rate and power dissipation have been compared.

	NON-INVERTING CONFIGURATION		INVERTING CONFIGURATION		DIFFERENTIAL CONFIGURATION	
PARAMETERS	**Circuit**	**Proposed circuit**	**Circuit**	**Proposed circuit**	**Circuit**	**Proposed circuit**
SUPPLY POWER	15V DC	15V DC	15V DC	15V DC	15V DC	15V DC
CMRR RATIO	97.23 dB	105.05dB	102.97 dB	107.16dB	93.58 dB	103.34dB
SLEW RATE	107.156T	108.13T	-30.556 T	61.24T	-28.67 T	65.16T
POWER DISSIPATED	0.385W	0.363W	0.395 W	0.363W	0.401 W	0.363W

Table1 - Comparison between BJT VFOA and Proposed BJT VFOA Circuit

3.2 VOLTAGE FEEDBACK OPERATIONAL AMPLIFIER USING CMOS:

3.2.1 Circuit Design :-

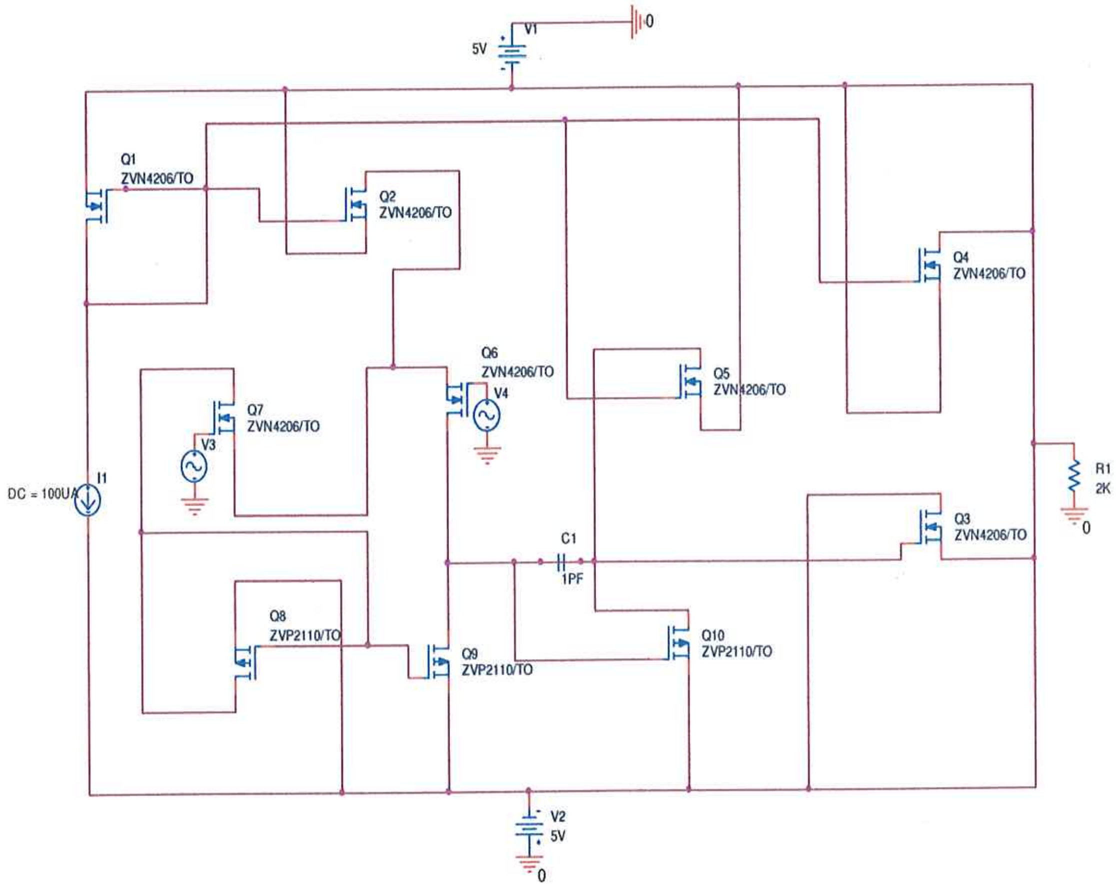

Figure 23 CMOS Op-Amp circuit

Given above is circuit for Voltage Feedback Op-Amp using CMOS. The supply voltage required to drive the above circuit is 5V which is one-third of voltage supply required for BJT Op-amp

3.2.2 OUTPUT WAVEFORMS FOR VOLTAGE FEEDBACK CMOS OP-AMP:

Using P-Spice software, the outputs for the CMOS Voltage Feedback Op-Amp have been traced for the three basic Op-Amp configurations:-

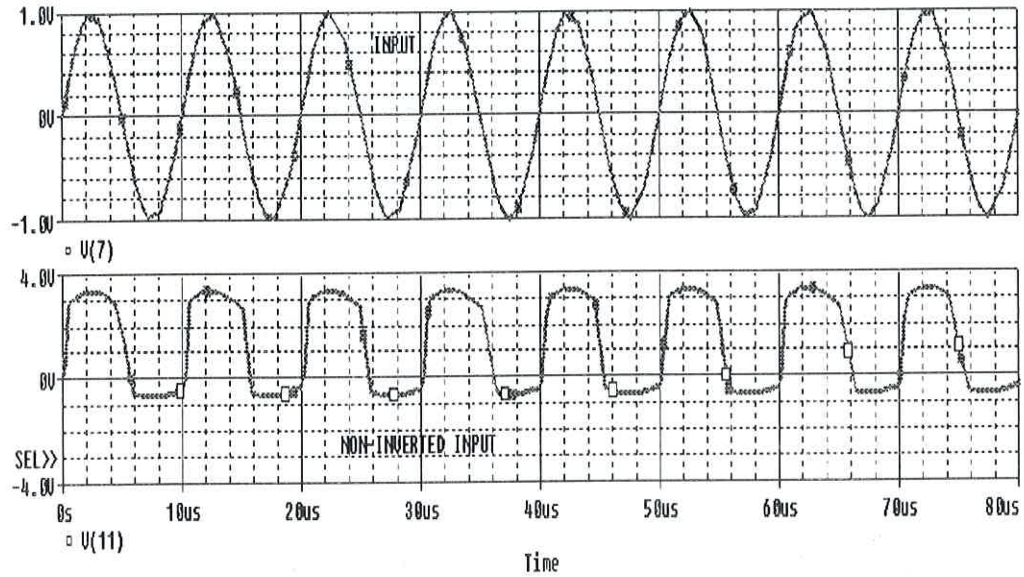

Figure 24: Non-Inverted Output

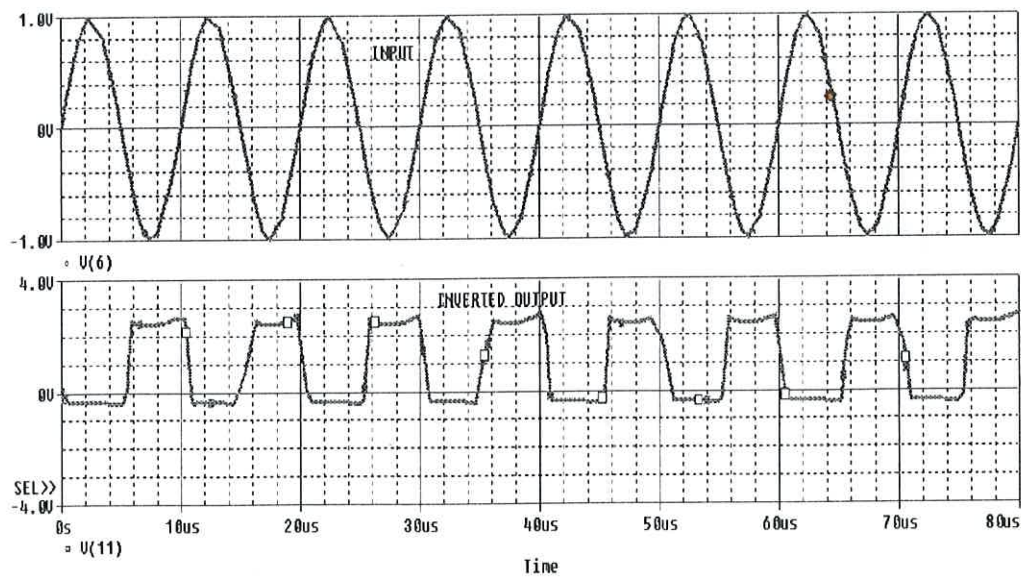

Figure 25: Inverted Output

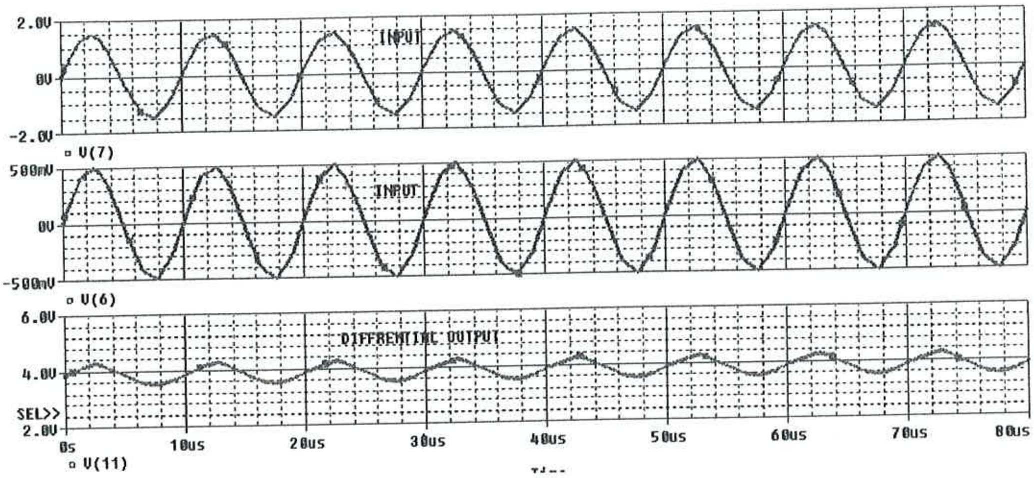

Figure 26: Differential Output

3.2.3 Circuit Design (Proposed):-

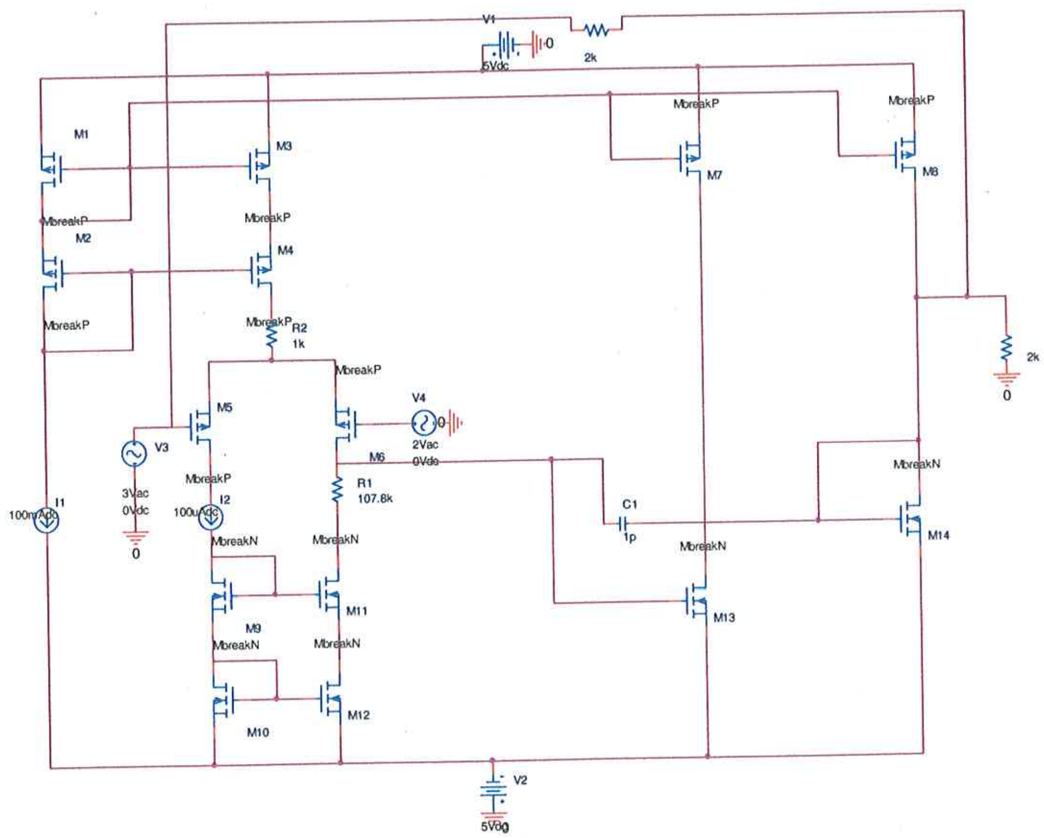

Figure 27 CMOS Op-Amp proposed design

The circuit shown above is the proposed model for CMOS Op-amp Voltage feedback. The input stage is further enhanced with addition of a PMOS-NMOS pair to the input CMOs rather than grounding the input via resistor.

3.2.4 OUTPUT WAVEFORMS FOR PROPOSED VOLTAGE FEEDBACK CMOS OP-AMP:

Using P-Spice software, the outputs for the proposed CMOS Voltage Feedback Op-Amp have been traced for the three basic Op-Amp configurations:-

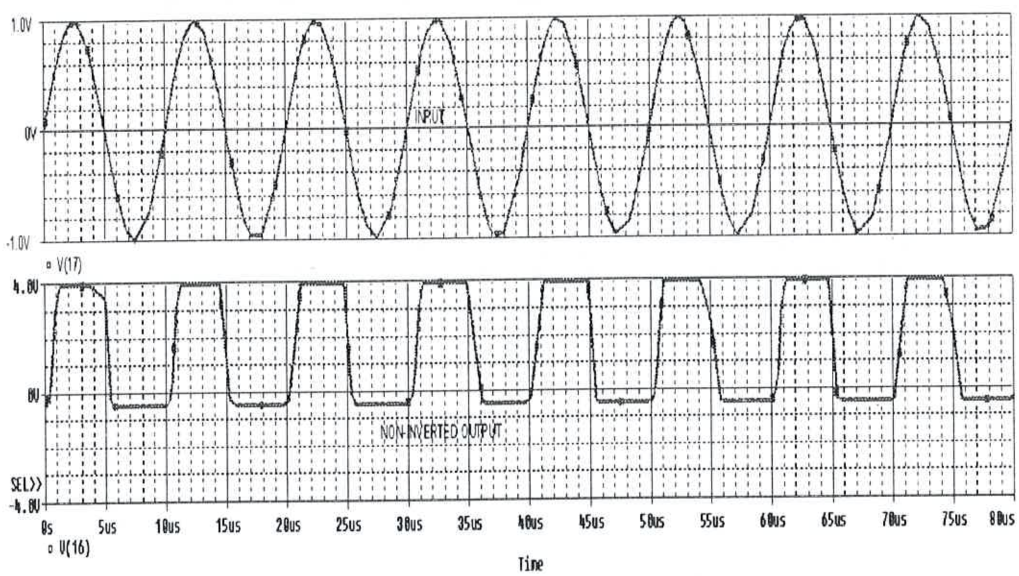

Figure 28: Non-Inverted Output

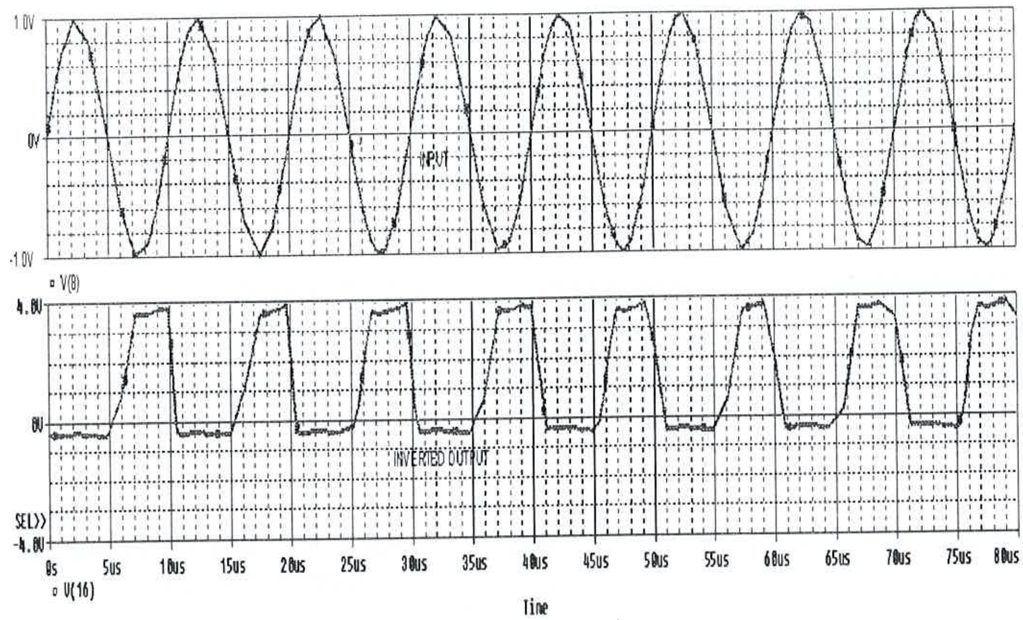

Figure 29: Inverted Output

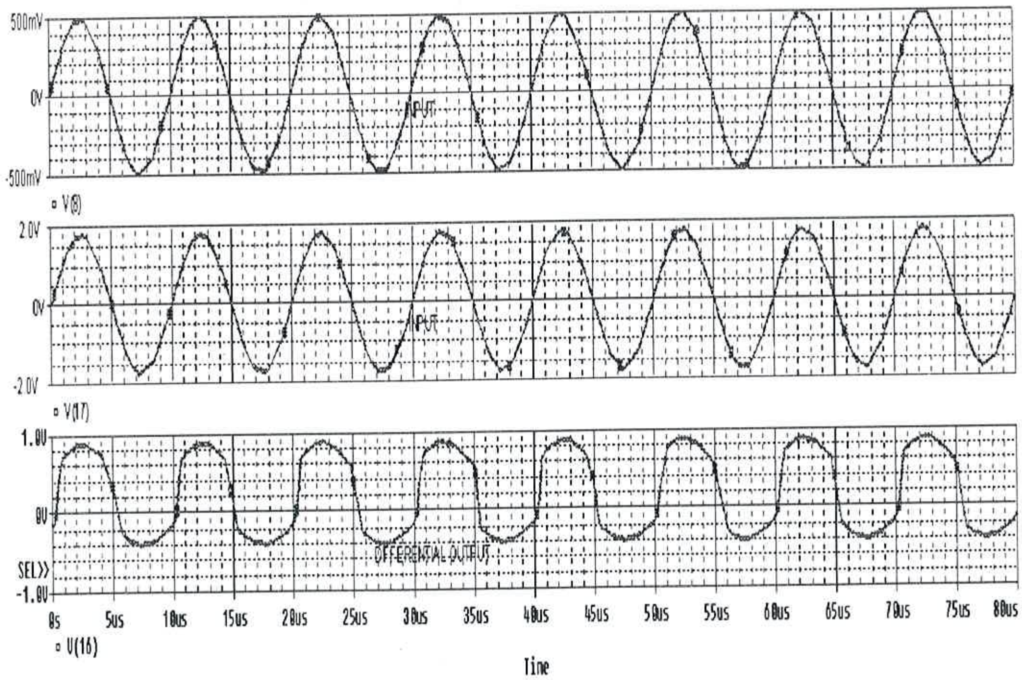

Figure 30: Differential Output

3.2.5 COMPARISON TABLE:

Given below is the comparison between the CMOS voltage feedback circuit and proposed model. Various parameters such as CMRR, Slew Rate and power dissipation have been compared.

	NON-INVERTING CONFIGURATION		INVERTING CONFIGURATION		DIFFERENTIAL CONFIGURATION	
PARAMETERS	**Circuit**	**Proposed circuit**	**Circuit**	**Proposed circuit**	**Circuit**	**Proposed circuit**
SUPPLY POWER	5V DC	5V DC	5V DC	5V DC	5V DC	5V DC
CMRR RATIO	79.23dB	90.28dB	76.45dB	90.22dB	72.45dB	84.35dB
SLEW RATE	5.34 Meg	7.182Meg	2.316 Meg	3.67Meg	229.51 K	2.089Meg
POWER DISSIPATED	1.24×10^{-2}W	1.31×10^{-2} W	1.24×10^{-2} W	1.31×10^{-2} W	6.22×10^{-3}W	1.31×10^{-2}W

Table 2 - Comparison between CMOS VFOA and Proposed CMOS VFOA Circuit

3.3 CURRENT FEEDBACK OPERATIONAL AMPLIFIER USING BJT

3.3.1 Circuit Design-:

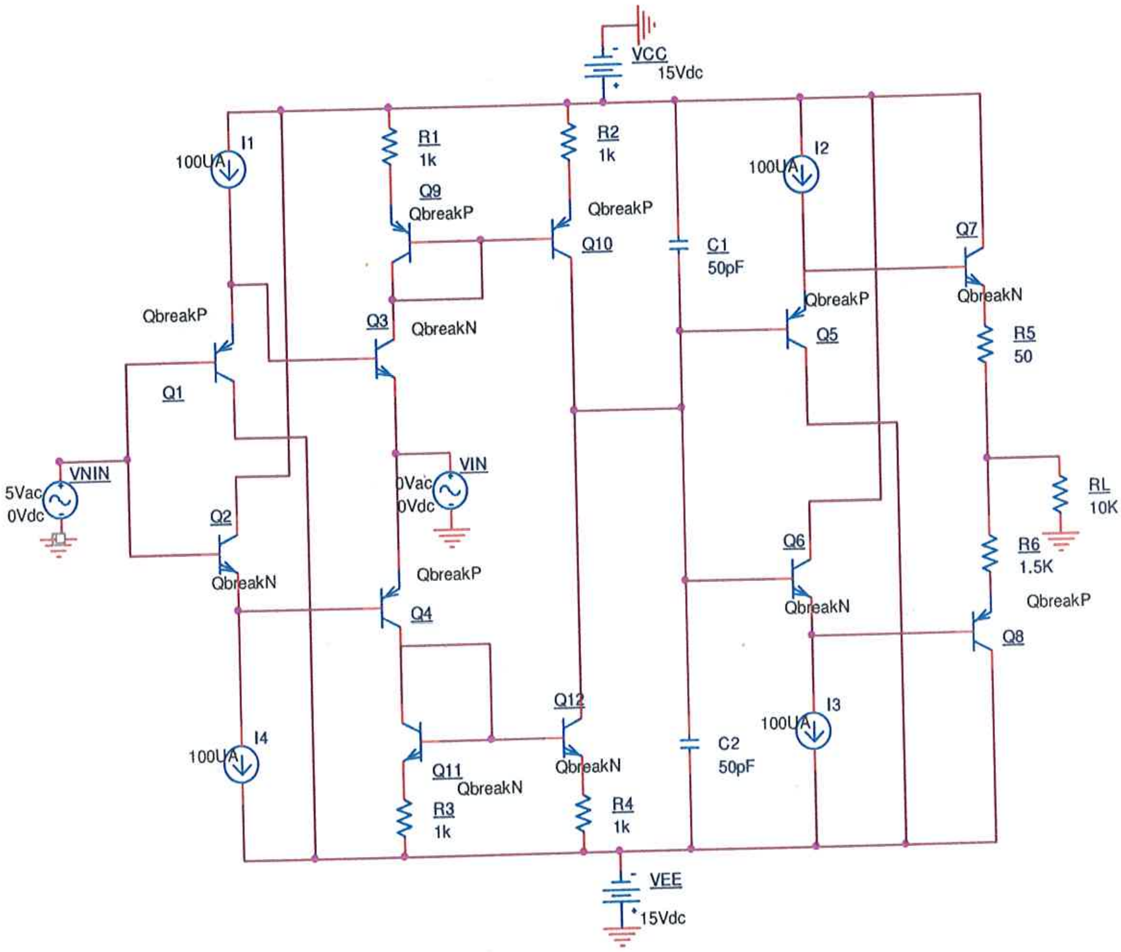

Figure 31 BJT CFOA circuit

Given above is a circuit for current feedback operational amplifier using BJT. The introduction of current sources enhances the performance of the circuit.

3.3.2 OUTPUT WAVEFORMS FOR CURRENT FEEDBACK BJT OP-AMP:

Using P-Spice software, the outputs for the BJT Current Feedback Op-Amp have been traced for the three basic Op-Amp configurations:-

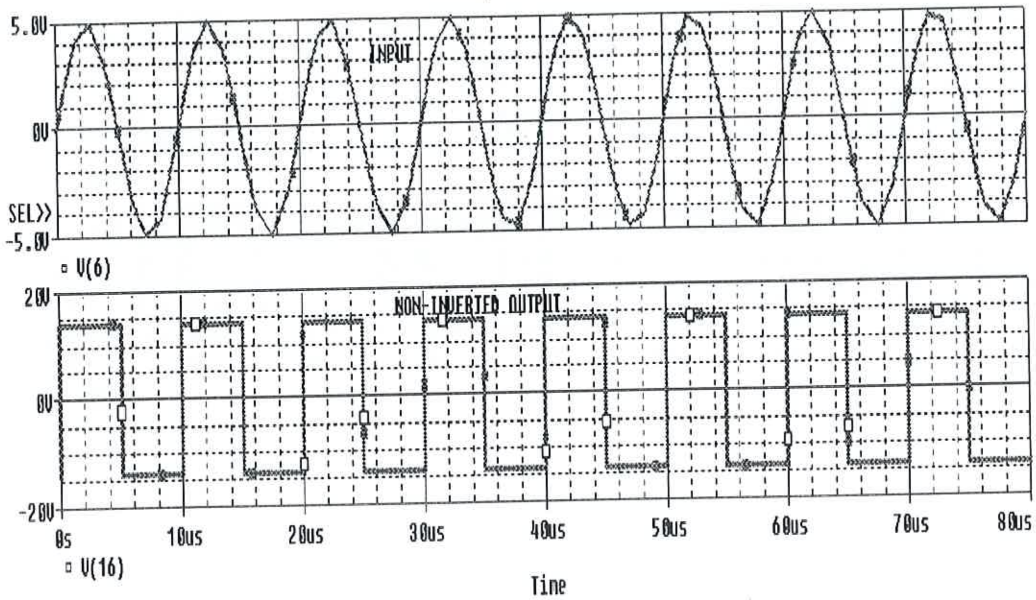

Figure 32: Non-Inverted Output

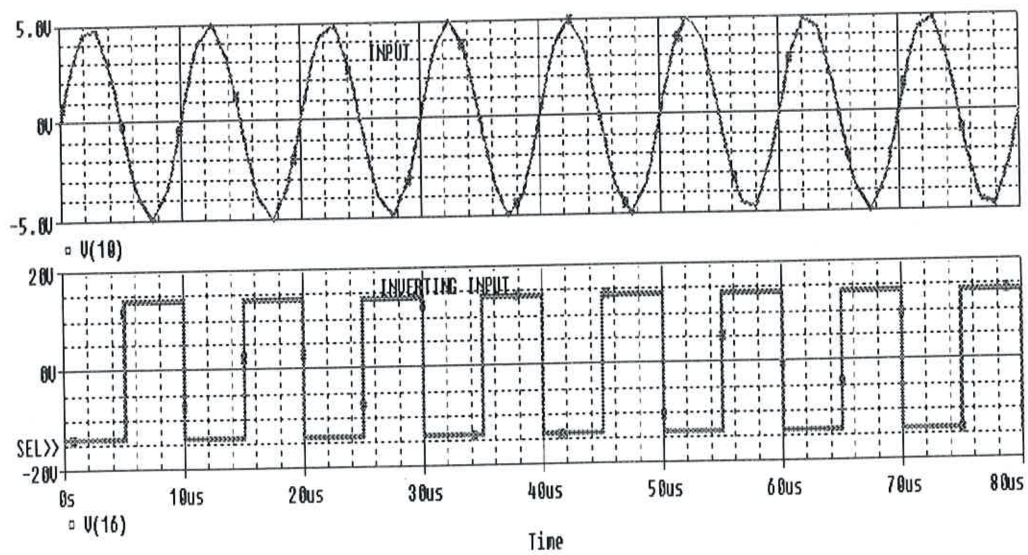

Figure 33: Inverted Outputs

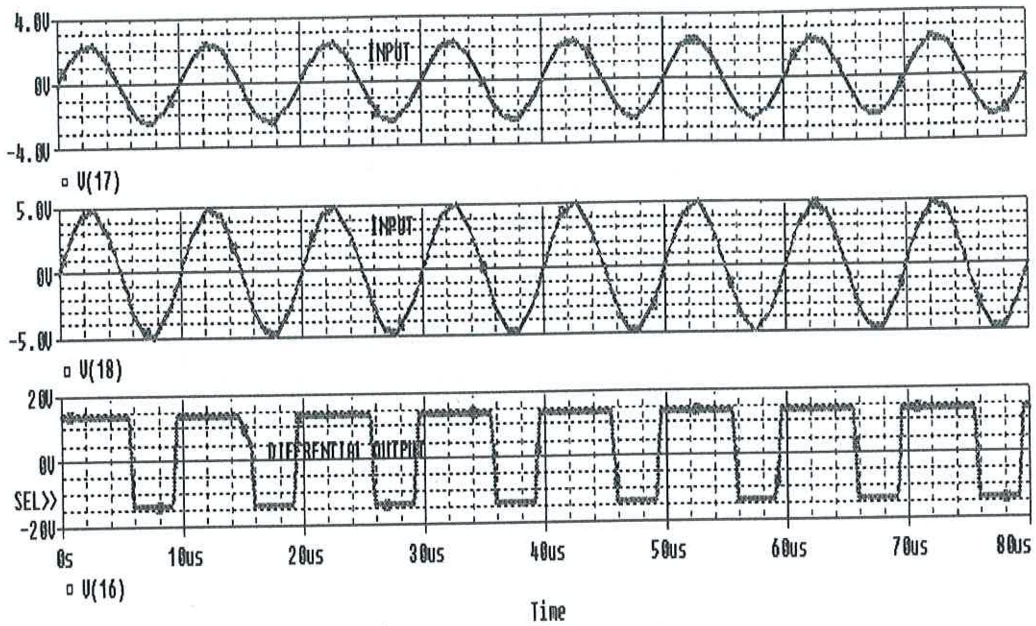

Figure 34: Differential Output

3.3.3 Circuit Design (Proposed) :-

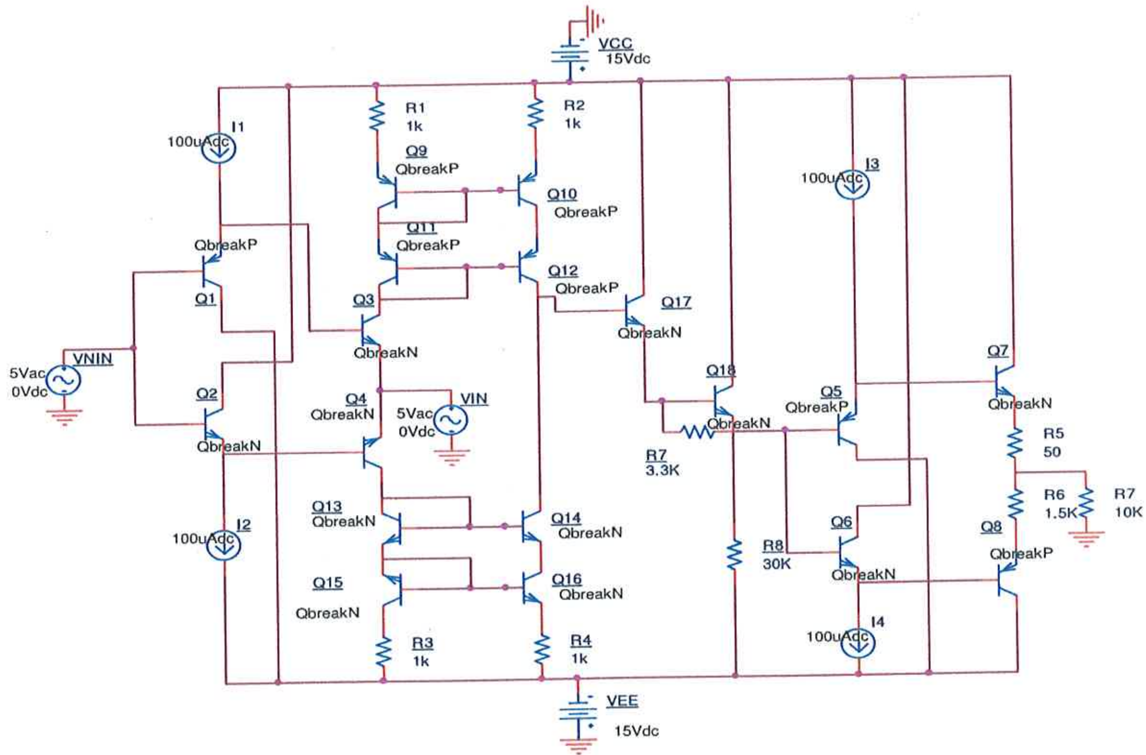

Figure 35 BJT CFOA proposed circuit

3.3.4 OUTPUT WAVEFORMS FOR PROPOSED CURRENT FEEDBACK BJT OP-AMP:

Using P-Spice software, the outputs for the proposed BJT Current Feedback Op-Amp have been traced for the three basic Op-Amp configurations:-

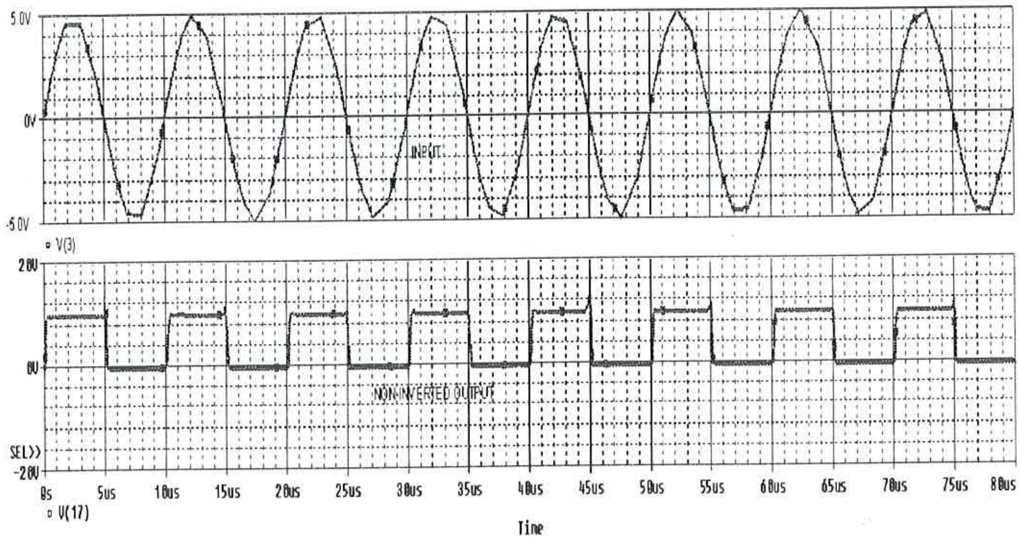

Figure 36: Non-Inverted Output

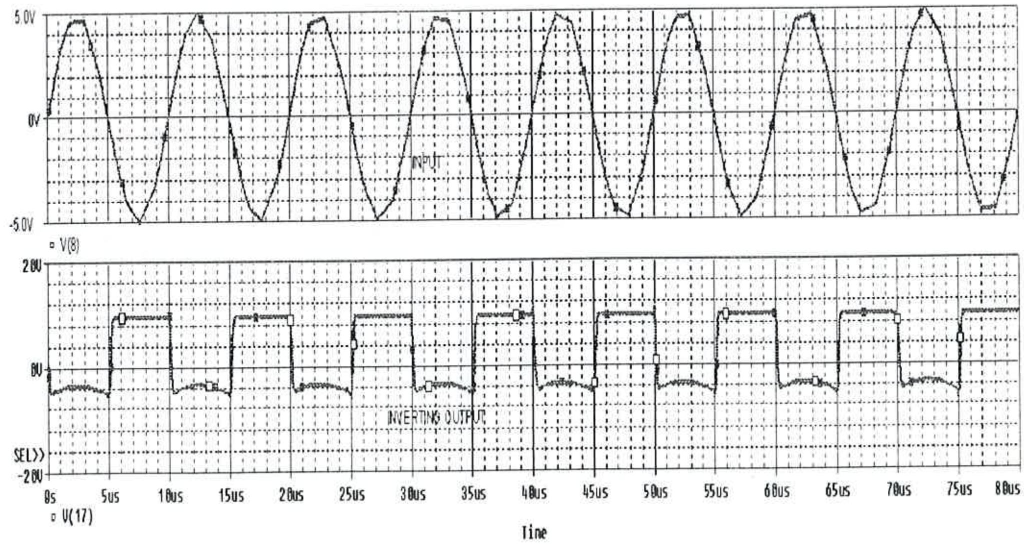

Figure 37: Inverted Output

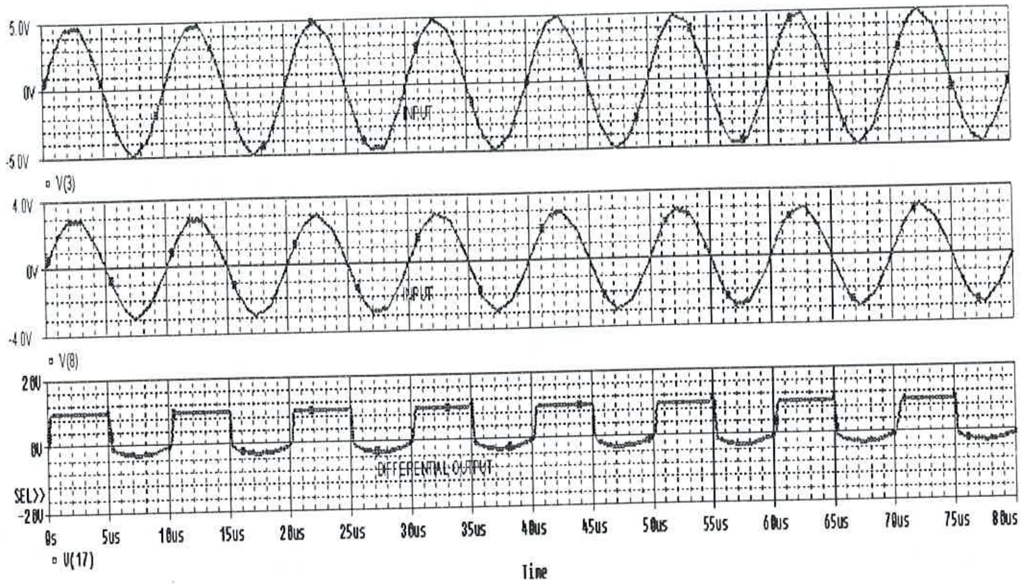

Figure 38: Differential Output

3.3.5 COMPARISON TABLE:

Given below is the comparison between the BJT Current feedback circuit and proposed model. Various parameters such as CMRR, Slew Rate and power dissipation have been compared.

	NON-INVERTING CONFIGURATION		INVERTING CONFIGURATION		DIFFERENTIAL CONFIGURATION	
PARAMETERS	**Circuit**	**Proposed Circuit**	**Circuit**	**Proposed Circuit**	**Circuit**	**Proposed Circuit**
SUPPLY POWER	15V DC	15V DC	15V DC	15V DC	15V DC	15V DC
CMRR RATIO	79.83dB	85.45dB	83.56dB	92.46dB	76.56dB	86.61dB
SLEW RATE	80.25Meg	97.2Meg	76.54Meg	94.37Meg	75.67Meg	96.92Meg
POWER DISSIPATED	1.60×10^{-2} W	1.79×10^{-2} W	1.68×10^{-2} W	1.88×10^{-2} W	1.60×10^{-2} W	1.79×10^{-2} W

Table 3 - Comparison between BJT CFOA and Proposed BJT CFOA Circuit

3.4 CURRENT FEEDBACK OPERATIONAL AMPLIFIER USING CMOS

3.4.1 CIRCUIT DESIGN:-

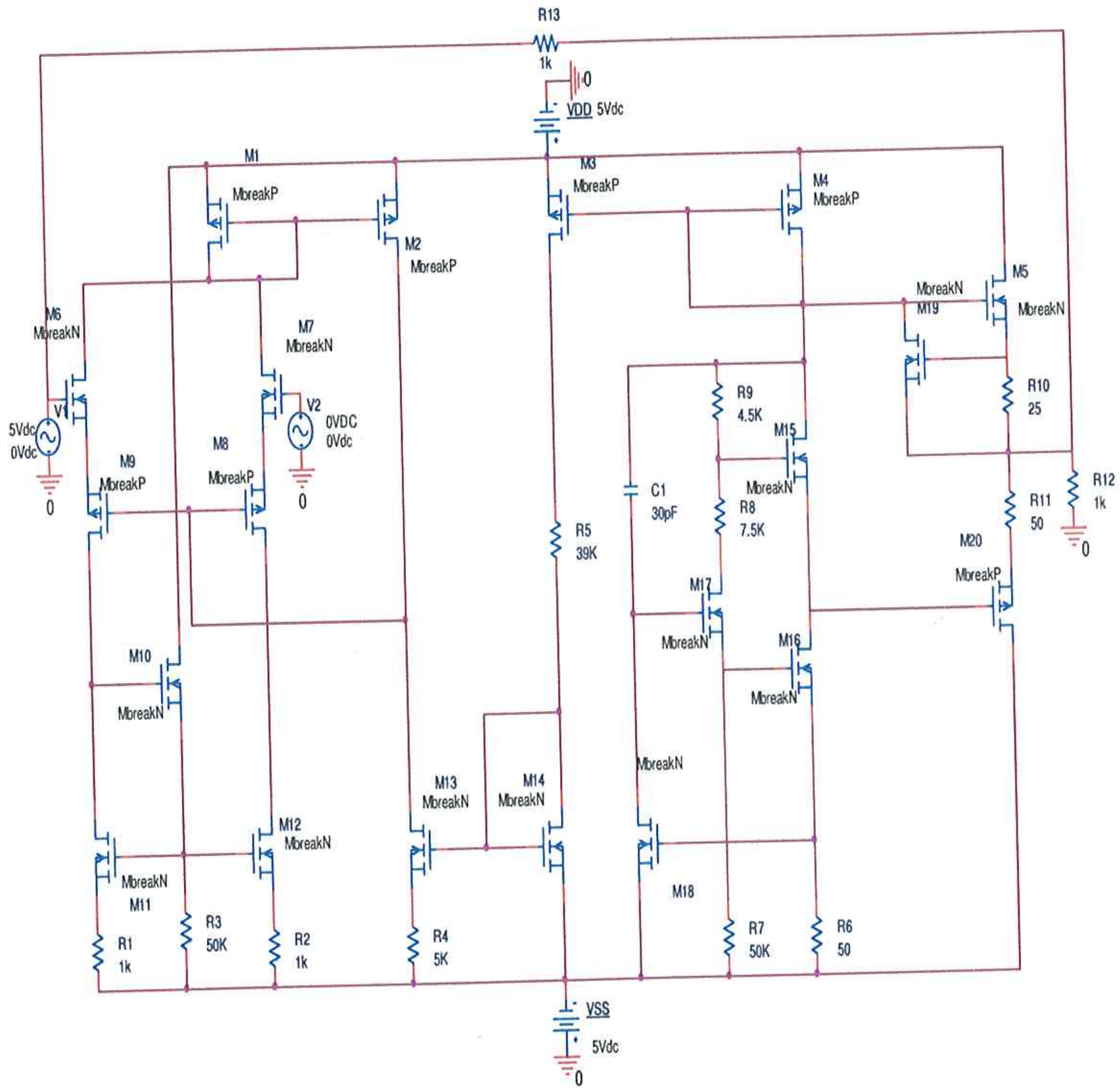

Figure 39 CMOS CFOA circuit

3.4.2 OUTPUT WAVEFORM OF CURRENT FEEDBACK CMOS OP-AMP :

Using P-Spice software, the outputs for the CMOS Current Feedback Op-Amp have been traced for the three basic Op-Amp configurations:-

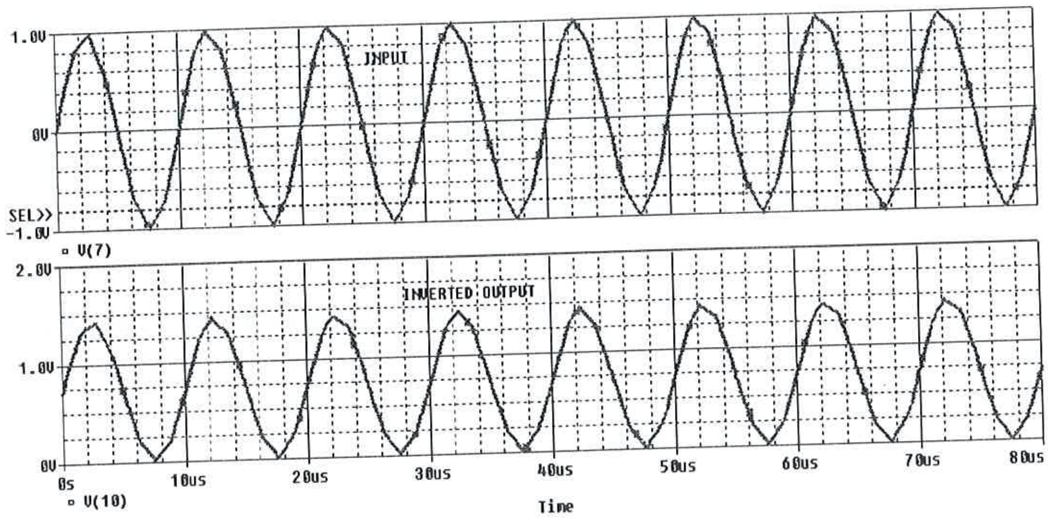

Figure 40: Non-Inverted Output

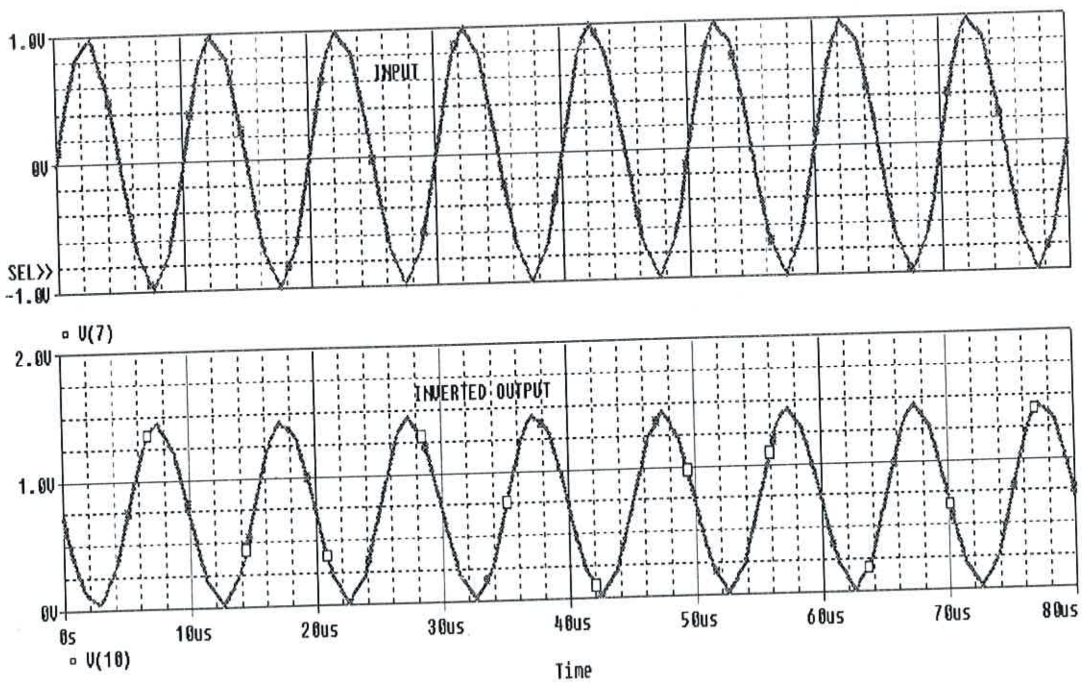

Figure 41 Inverted output

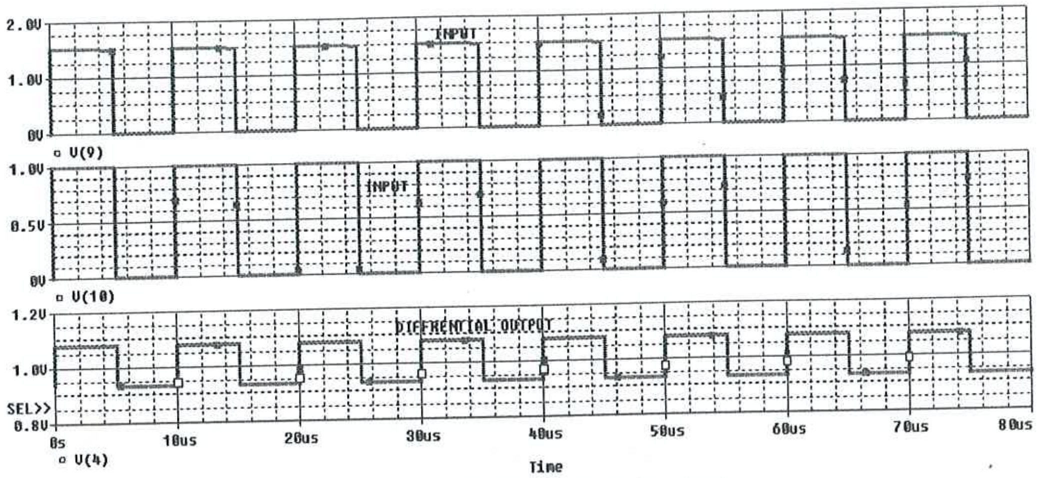

Figure 42 Differentiated output

3.4.3 CIRCUIT DESIGN (PROPOSED):-

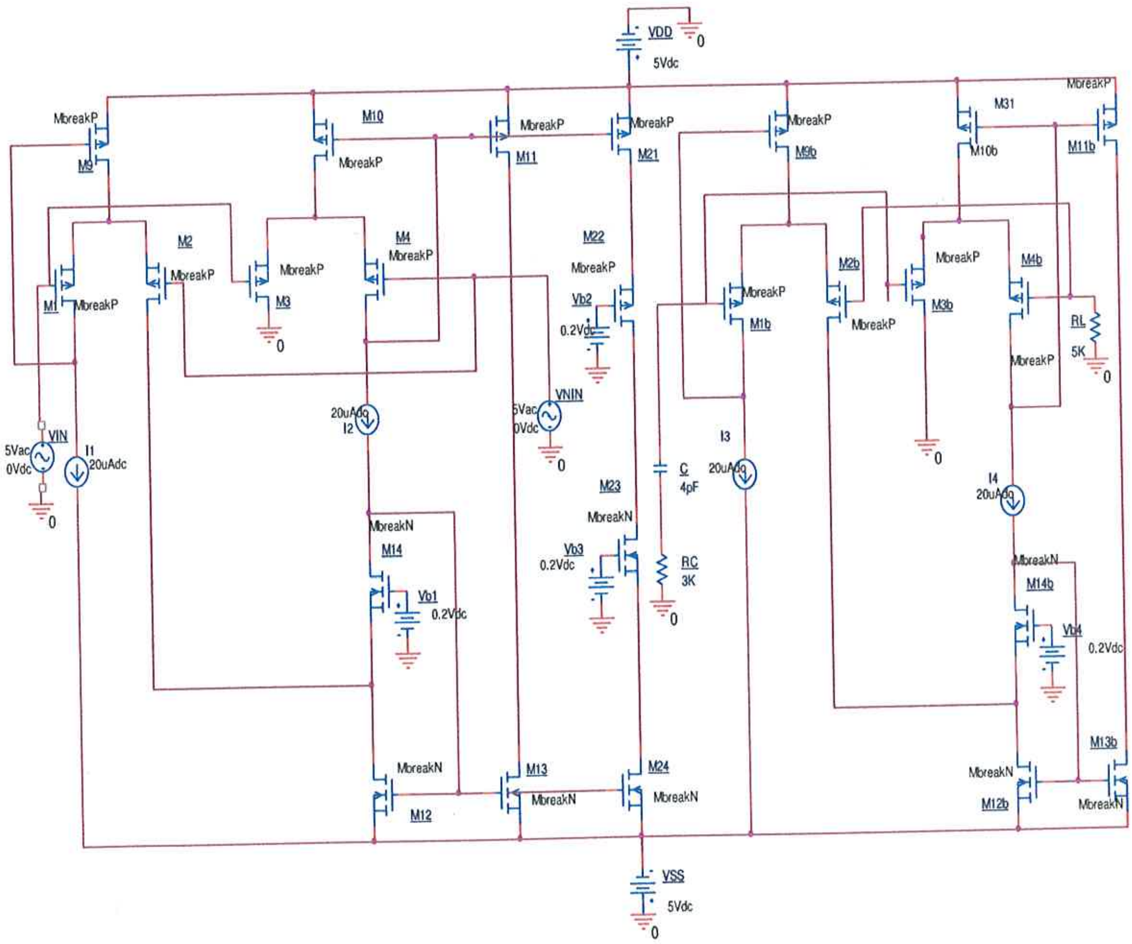

Figure 43 CMOS CFOA proposed circuit

3.4.4 OUTPUT WAVEFORM OF PROPOSED CURRENT FEEDBACK CMOS OP-AMP :

Using P-Spice software, the outputs for the proposed CMOS Current Feedback Op-Amp have been traced for the three basic Op-Amp configurations:-

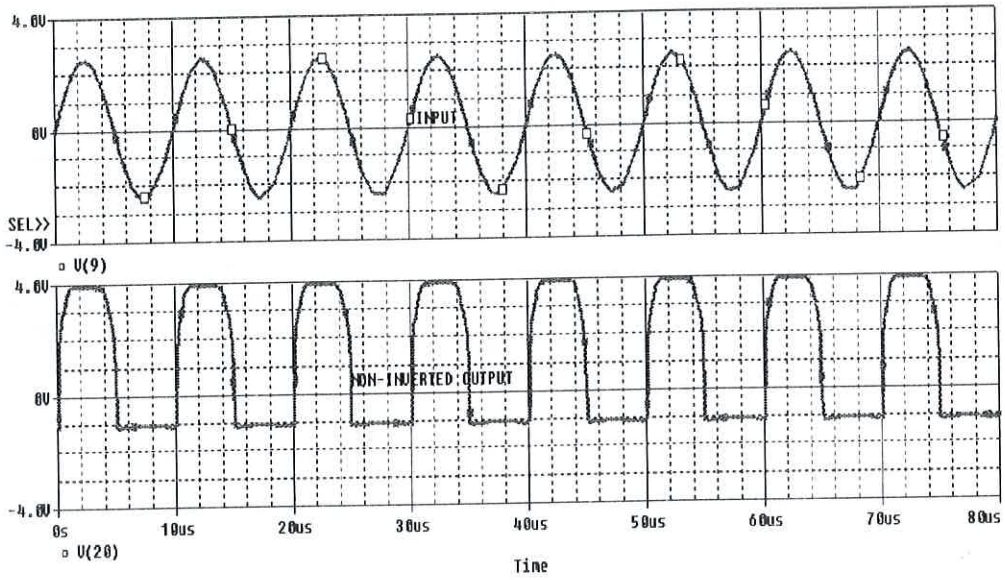

Figure 44: Non-Inverted Output

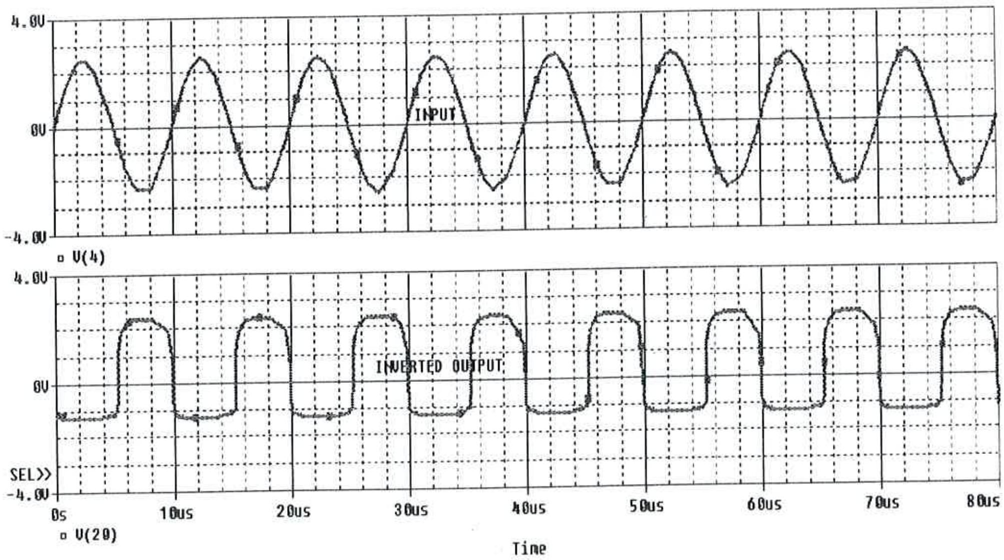

Figure 45: Inverted Output

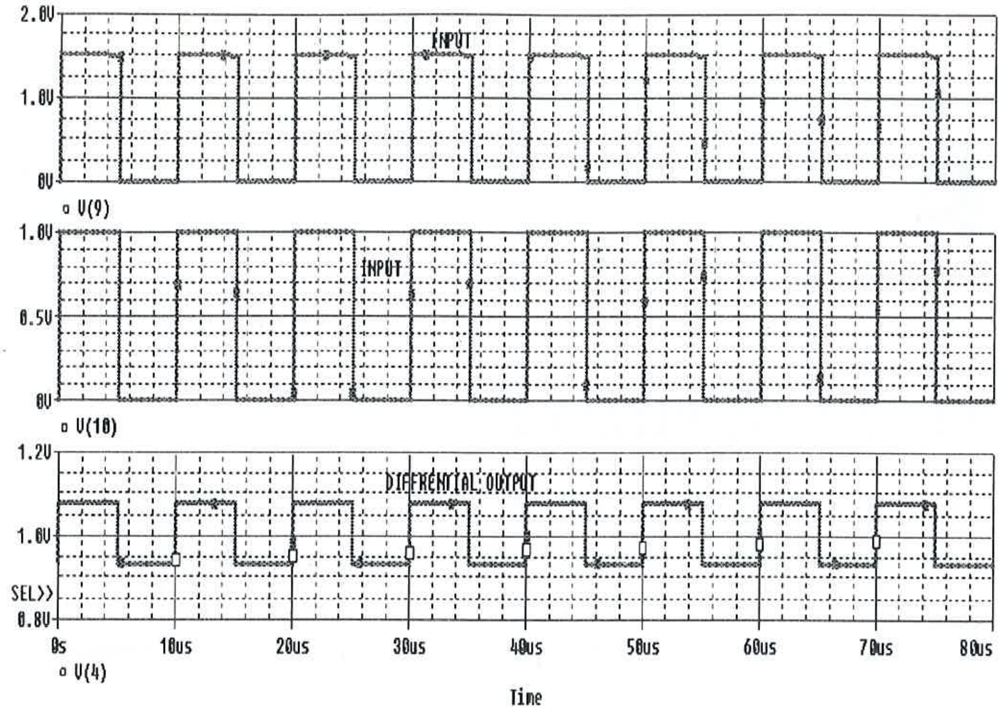

Figure 46: Differential Output

3.5.5 COMPARISON TABLE:

Given below is the comparison between the CMOS current feedback circuit and proposed model. Various parameters such as CMRR, Slew Rate and power dissipation have been compared.

	NON-INVERTING CONFIGURATION		INVERTING CONFIGURATION		DIFFERENTIAL CONFIGURATION	
PARAMETERS	**Circuit**	**Proposed Circuit**	**Circuit**	**Proposed Circuit**	**Circuit**	**Proposed Circuit**
SUPPLY POWER	5V DC	5V DC	5V DC	5V DC	5V DC	5V DC
CMRR RATIO	87.56dB	90.28dB	80.98dB	87.34dB	75.65dB	85.76dB
SLEW RATE	25.32Meg	30.34Meg	17.54Meg	20.025Meg	24.65Meg	26.98Meg
POWER DISSIPATED	1.24×10^{-2} W	1.79×10^{-2} W	1.24×10^{-2} W	1.88×10^{-2} W	1.50×10^{-2} W	1.79×10^{-2} W

Table 4 - Comparison between CMOS CFOA and Proposed CMOS CFOA Circuit

4

COMPENSATION

At higher frequencies (f >>1MHz), the stray capacitance within the op-amp becomes significant. Therefore at higher frequencies, it becomes important to intentionally reduce the open-loop gain of the op-amp. This is called ***compensation.***
It is carried out by by-passing the internal stages of the internal amplifier stage with a high-pass filter.

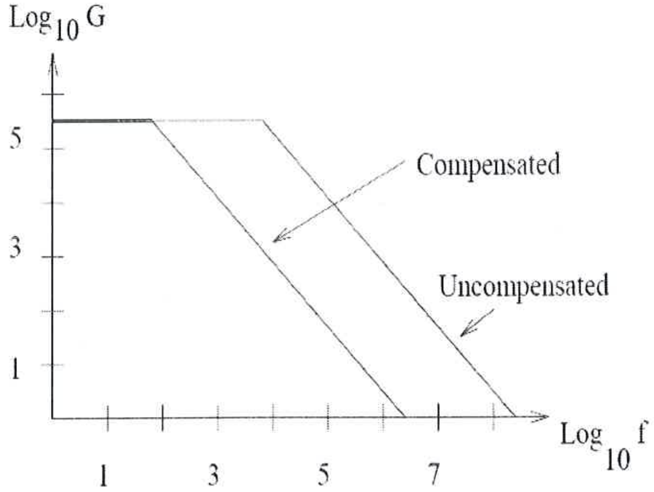

Figure 47 Bode plot showing effect of compensation in op-amp

The above figure is a bode plot showing the effect how the intrinsic gain of a compensated op-amp decreases much sooner as compared to the one without compensation. Objective of compensation is to achieve stable operation when negative feedback is applied across the operational amplifier.

4.1 TYPES OF COMPENSATION :

4.1.1 Miller Compensation :

- For Miller compensation technique, we use a capacitor feeding back around a high-gain and inverting stage in an op-amp.
- Compensation capacitor (Cc) between the output of the gain stages causes pole-splitting and achieves dominant pole compensation
- When Miller compensation is used, a zero is introduced that can limit the design in some cases

4.1.2 Gain Compensation :

- The occasion always arises where the closed loop gain must be one or less, thereby precluding the use of gain compensation; thus the designer must resort to other techniques to achieve the circuit performance.
- An alternate method of compensation is called lead compensation, and it consists of putting a zero in the loop transfer function to cancel out one of the poles.

4.1.3 Dominant Pole Compensation

- Dominant pole compensation circuits tend to be associated with the op amp, and they usually are not part of the feedback circuit.
- Since these pole locations are inherent in the op amp design, the circuit designer must live with them, but the effects of these poles can be modified with external feedback components.

5

BODE PLOT AND NYQUIST PLOT

Bode plot is a graphical representation of a transfer function for determining the stability of the control system. Bode plot consist of two separate plots. One of the plots is of the logarithm of the magnitude of a sinusoidal transfer function while other is a plot of the phase angle. Both the plots are plotted against the frequency on a logarithmic scale.

The curves are drawn on semi-log graph paper, using the log scale for frequency and linear scale for magnitude (in decibels) or phase angle (in degrees).

The magnitude is represented in decibels. Thus, the bode plot consist of

i. $20 \log_{10} |G(j\omega)|$ V_s $\log(\omega)$.

ii. Phase shift V_s $\log(\omega)$

5.1 BASIC FACTORS OF $G(j\omega)\ H(j\omega)$:

The main advantage of using the logarithmic plot is the relative ease of plotting the frequency-response curves. The basic factors that very frequently occur in an arbitrary transfer function $G(j\omega)\ H(j\omega)$ are

i. Gain K.
ii. Integral and derivative factors $(j\omega)^{\pm 1}$
iii. First order factors $(1+j\omega T)^{\pm 1}$

Adding the logarithms of the gain corresponds to multiplying them together.

5.2 The Gain K :

The number greater than unity has a positive value in decibels, while a number less than unity has a negative value. The log magnitude graph for a constant gain K is a horizontal line at a magnitude of 20 *log(K)* decibels. The phase angle for constant gain is zero.

The effect of varying the gain K in the transfer function is that it raises or lowers the log-magnitude graph of the logarithmic-magnitude graph by the corresponding amount, but it has no effect on phase curve.

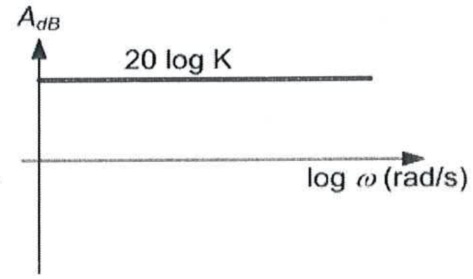

Figure 48 Magnitude plot

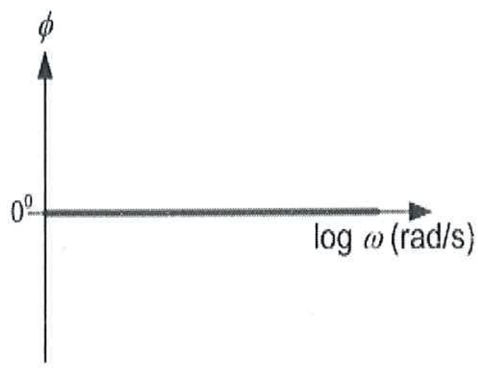

Figure 49 Phase Plot

5.3 Integral and Derivative Factor $(j\omega)^{\pm 1}$:

The logarithmic magnitude of $1/(j\omega)$ in decibels is

$$20\log\left|\frac{1}{j\omega}\right| = -\,20\log\omega \text{ dB}$$

The phase angle of $1/j\omega$ is constant and is equal to -90°.

In bode plot, the frequency ratios are expressed in terms of octave and decades. An octave is a frequency band from ω_1 to $2\omega_1$, where ω_1 is any frequency value. A decade is a frequency band from ω_1 to $10\omega_1$, where ω_1 is any frequency value.

If the log magnitude $-20log(\omega)$ dB is plotted against ω on the logarithmic scale, it is a straight line. The slope of the line is -20dB/decade. (or -6dB/octave). Similarly, the log magnitude of $j\omega$ in decibels is

$$20 \log | j\omega | = 20 \log \omega \text{ dB}$$

The phase angle of $j\omega$ is constant and equal to 90°.The log-magnitude curve is a straight line with a slope of 20 dB/decade.

If the transfer function contains the factor $(1/ j\omega)^n$ and $(j\omega)^n$, the log-magnitude becomes respectively,

$$20\log\left|\frac{1}{(j\omega)^n}\right| = -20n \log\omega \text{ dB}$$

$$20\log | (j\omega)^n | = 20n \log\omega \text{ dB}$$

The slopes of the log-magnitude curves for the factors $(1/ j\omega)^n$ and $(j\omega)^n$ are thus $20n$dB/decade and $20n$ dB/decade, respectively. The phase angle of (lljw)" is equal to $(-90° \times n)$ over the entire frequency range, while that of $(j\omega)^n$ is equal to $(90° \times n)$ over the entire frequency range.

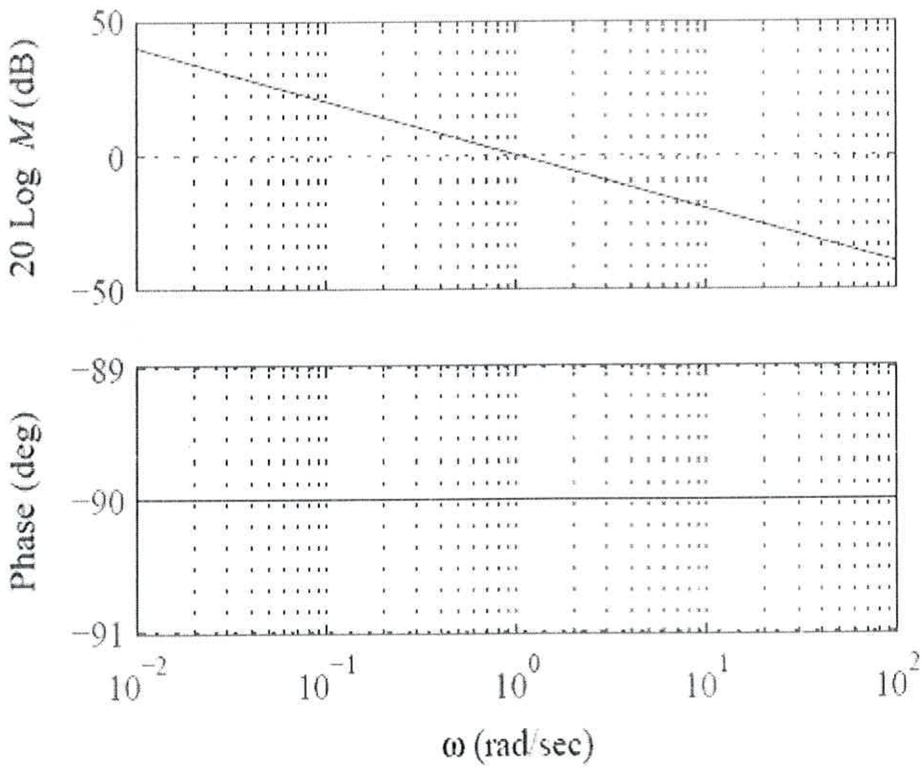

Figure 50 Bode plot for $G(j\omega)=1/ (j\omega)$

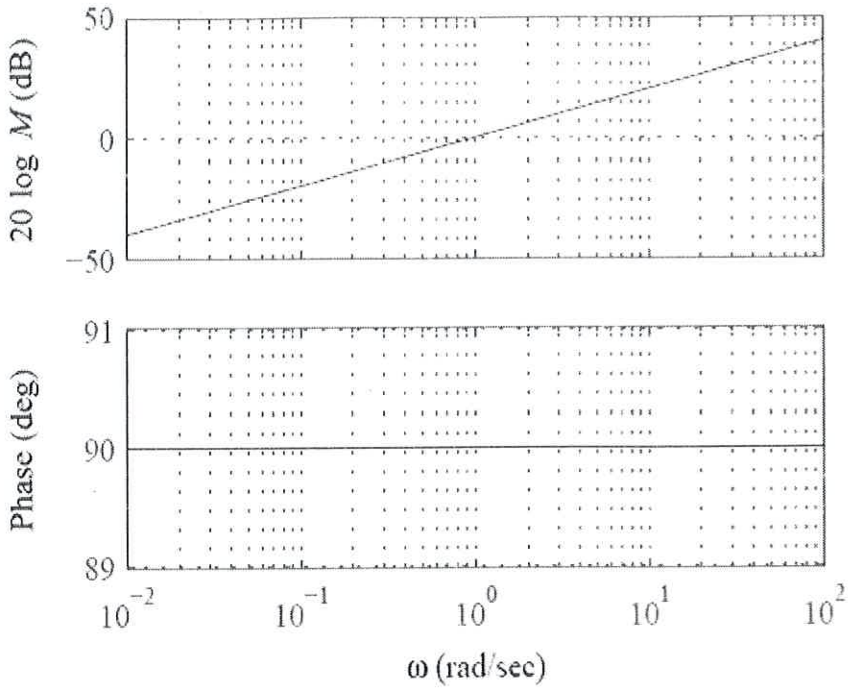

Figure 51 Bode plot for G($j\omega$)= $j\omega$

5.4 First-Order Factors $(1+j\omega T)^{\pm 1}$:

The log magnitude of the first-order factor $\dfrac{1}{(1+j\omega T)}$ is

$$20\log\left|\frac{1}{(1+j\omega T)}\right| = -20log\sqrt{1+(\omega T)^2}\ \text{dB}$$

For low frequencies, such that $\omega << 1/T$, The log magnitude may be approximated by

$$-20log\sqrt{1+(\omega T)^2} = -20\ log(1) = 0\ \text{dB}$$

This is an approximate expression for the high-frequency range. At $\omega = 1/T$, the log magnitude equals 0 dB; at $\omega = 10/T$, the log magnitude is -20 dB. Thus, the value of -20 log(ωT) dB decreases by 20 dB for every decade of ω. For $\omega >> 1/T$, the log-magnitude curve is thus a straight line with a slope of -20 dB/decade (or -6 dB/octave).

The logarithmic representation of the frequency-response curve of the factor 1/(1 + jωT) can be approximated by two straight-line asymptotes, one a straight line at 0 dB for the frequency range $0 < \omega < 1/T$ and the other a straight line with slope -20 dB/decade (or -6 dB/octave) for the frequency range $1/T < \omega < \infty$.

The frequency at which the two asymptotes meet is called the corner frequency or break frequency. For the factor $1/(1 + j\omega T)$, the frequency $\omega = 1/T$ is the corner frequency since at $\omega = 1/T$, the two asymptotes have the same value. The corner frequency divides the frequency-response curve into two regions: a curve for the low-frequency region and a curve for the high-frequency region.

The exact phase angle Φ of the factor $\dfrac{1}{(1+j\omega T)}$ is

$$\phi = -\tan^{-1}(\omega T)$$

At zero frequency, the phase angle is 0°. At the corner frequency, the phase angle is

$$\phi = -\tan^{-1}\frac{T}{T} = -\tan^{-1}1 = -45^{\circ}$$

At infinity, the phase angle becomes -90°. Since the phase angle is given by an inverse tangent function, the phase angle is skew symmetric about the inflection point at $\phi = -45°$.

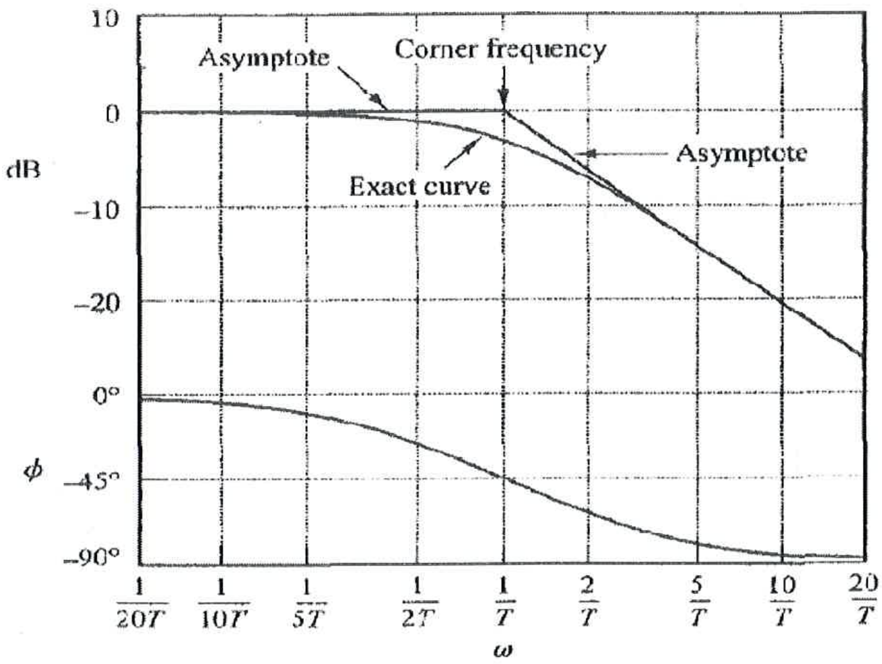

Figure 52 Log-magnitude curve and the phase-angle curve of 1/(1 +jωT)

5.5 Advantages Of Bode Plots :

- Both low and high frequency characteristics of the transfer function can be shown in one diagram.
- Gain margin and phase margin can be obtained with minimum computational effort from bode plot.
- They can be easily constructed using asymptotic assumptions.
- Data from constructing polar plots and Nyquist plots for complex transfer can be easily obtained from bode plots.
- Frequency domain specifications can be easily obtained from bode plot.
- The product term $G(j\omega)$ becomes additive terms since logarithm are used.
- Stability of the open loop transfer function can be obtained by using bode plots.

5.6 BODE PLOT FOR COMPENSATED VFOA AND CFOA USING BJT :

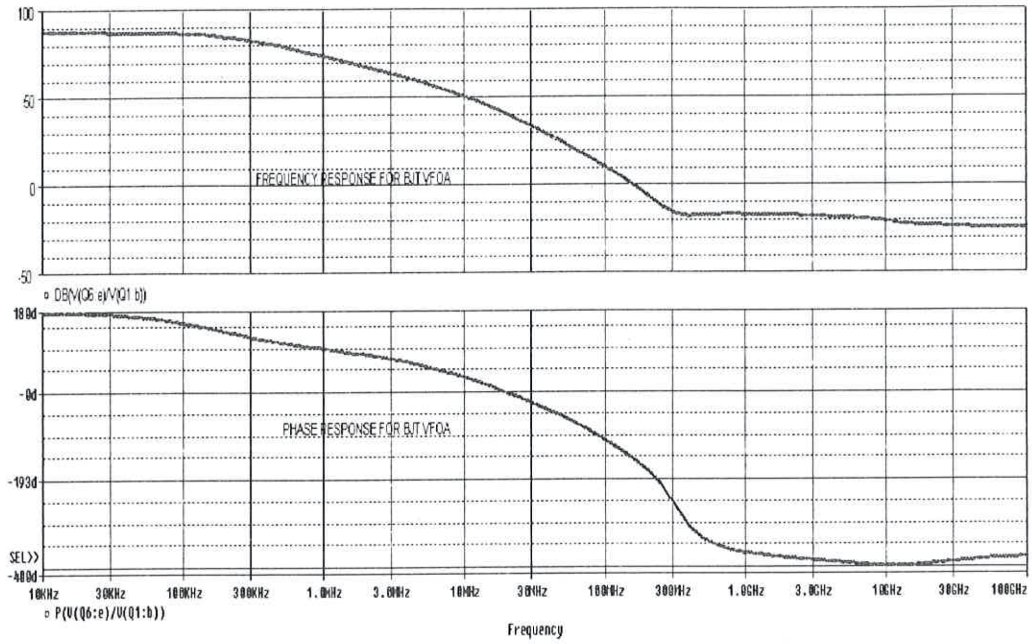

Figure 53 Bode plot for BJT VFOA

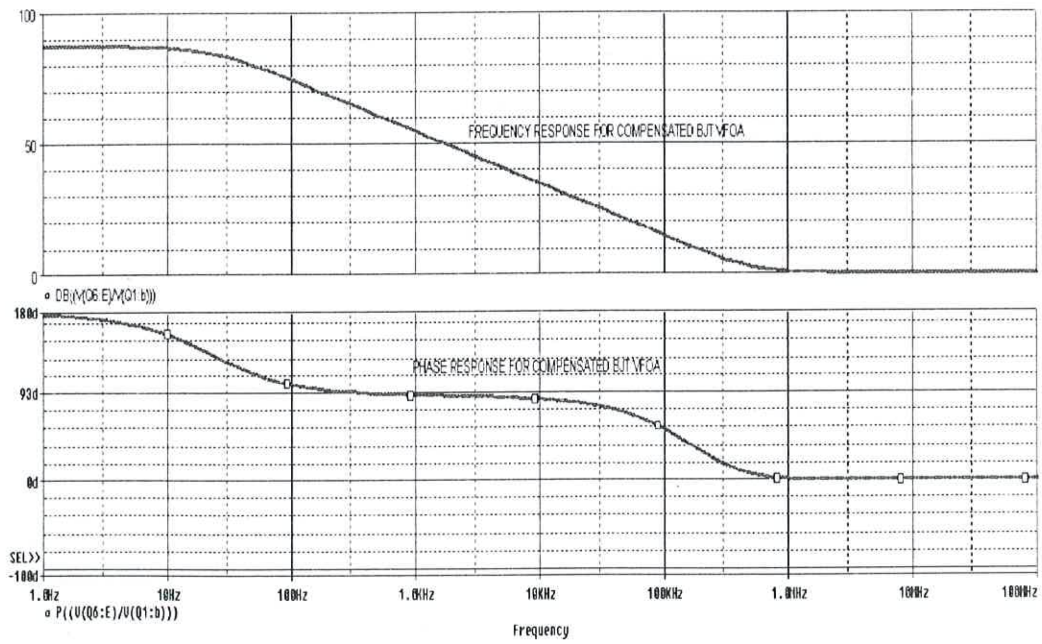

Figure 54 Bode plot for Compensated BJT VFOA

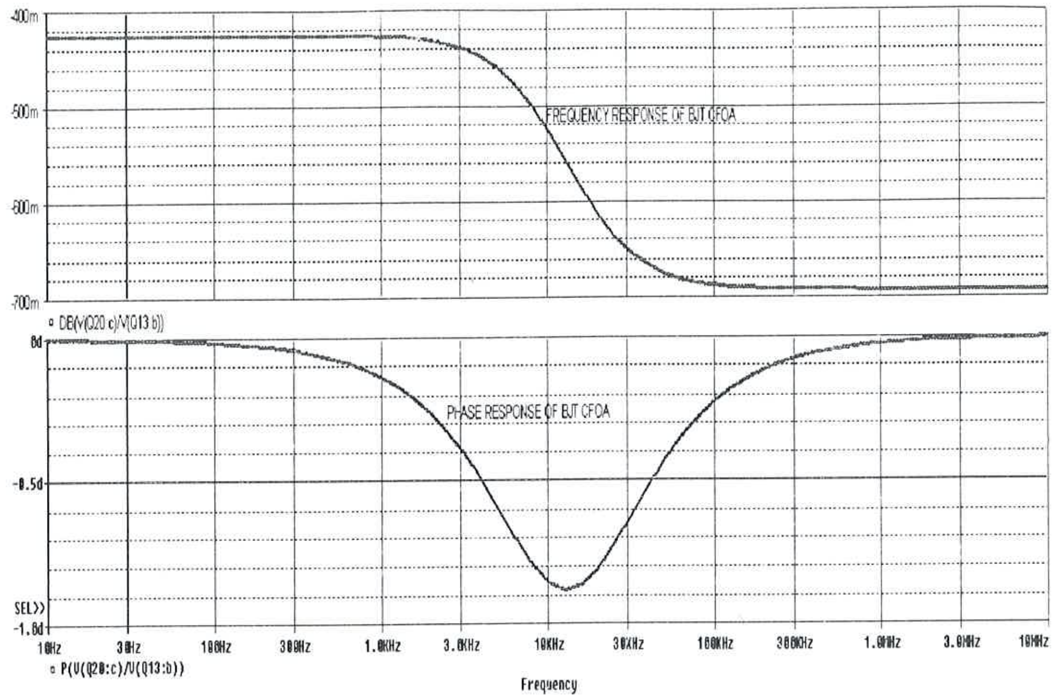

Figure 55 Bode plot for BJT CFOA

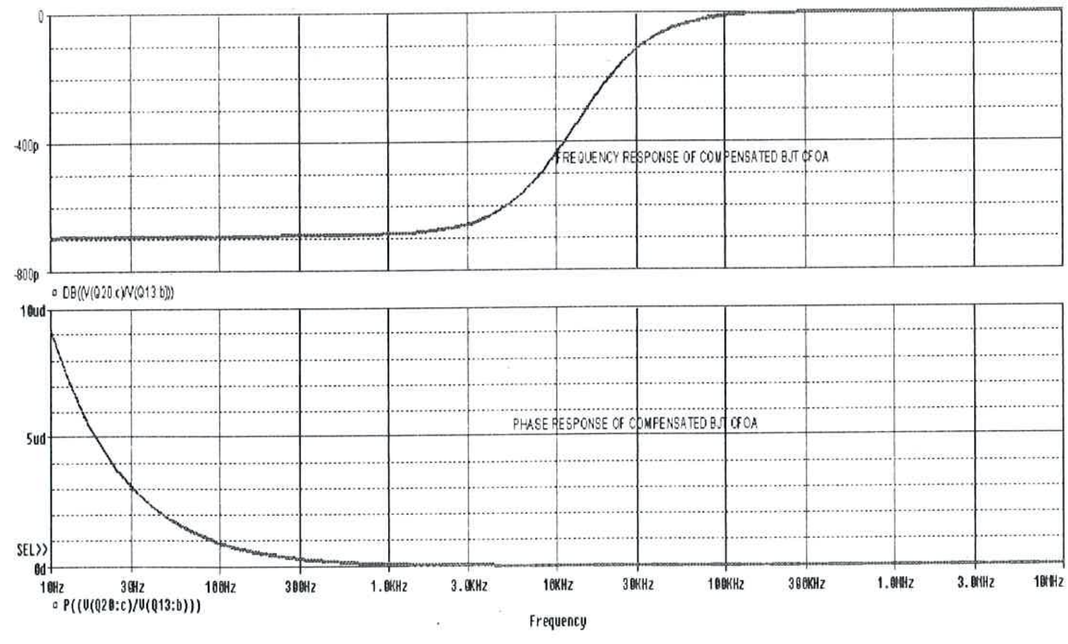

Figure 56 Bode plot for Compensated BJT CFOA

5.7 BODE PLOT FOR COMPENSATED VFOA AND CFOA USING CMOS :

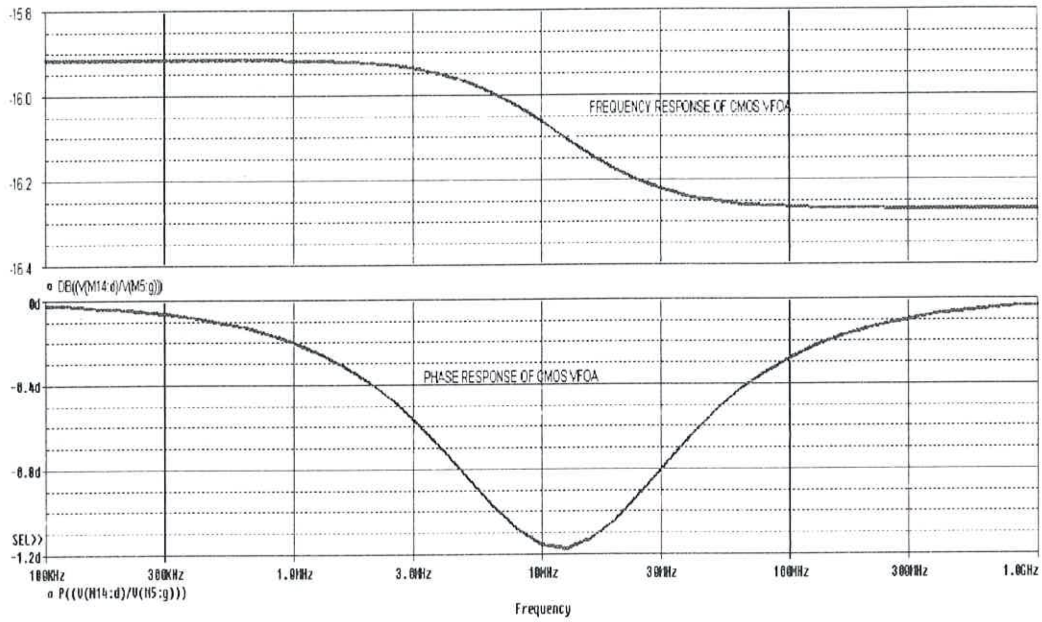

Figure 57 Bode plot for CMOS VFOA

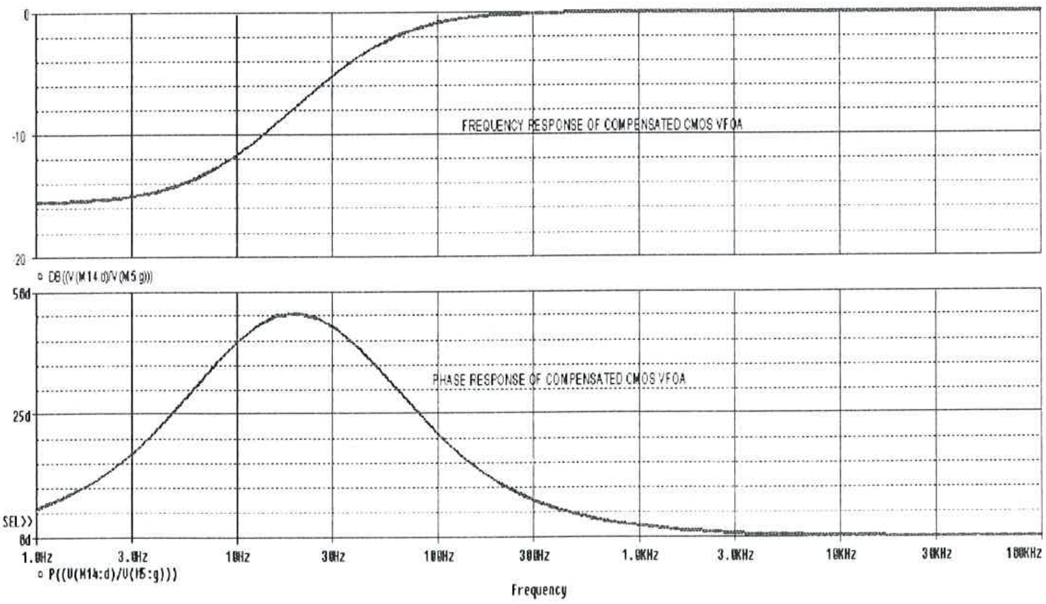

Figure 58 Bode plot for Compensated CMOS VFOA

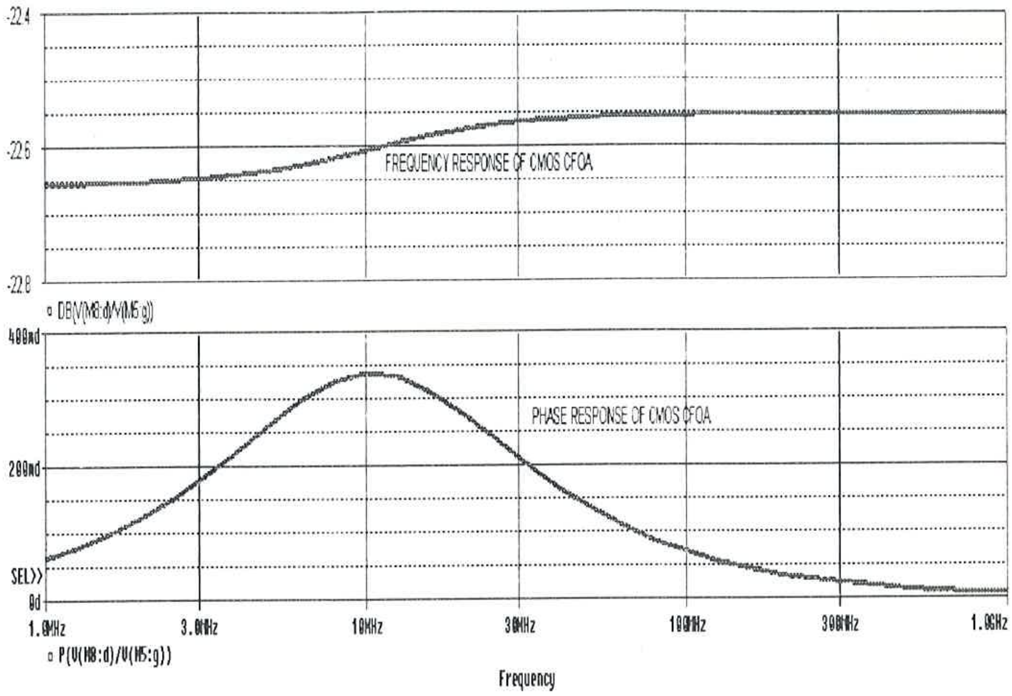

Figure 59 Bode plot for CMOS CFOA

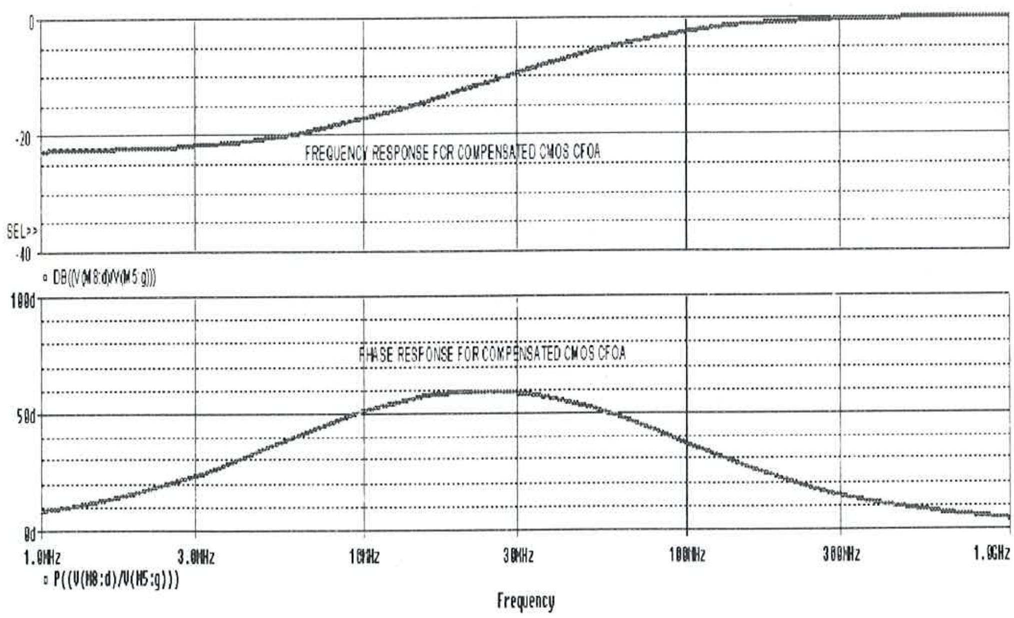

Figure 60 Bode plot for compensated CMOS CFOA

5.8 THE NYQUIST PLOT

The Nyquist plot of a sinusoidal transfer function $G(j\omega)$ is a plot of the magnitude of $G(j\omega)$ versus the phase angle of $G(j\omega)$ on polar coordinates as ω is varied from zero to infinity.

Thus, the nyquist plot is the locus of vectors $|G(j\omega)|$angle($G(j\omega)$) as ω is varied from zero to infinity. In polar plots a positive (negative) phase angle is measured counter-clockwise (clockwise) from the positive real axis.

Each point on the polar plot of $G(j\omega)$ represents the terminal point of a vector at a particular value of ω. In the nyquist plot, it is important to show the frequency graduation of the locus. The projections of $G(j\omega)$ on the real and imaginary axes are its real and imaginary components.

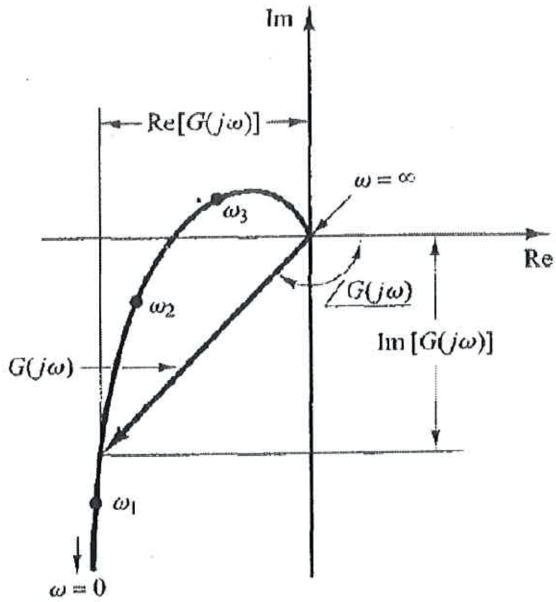

Figure 61 Nyquist Plot

5.9 NYQUIST STABILITY CRITERION :

Nyquist stability criterion is a graphical method to determine the stability of a closed loop system by examining the behavior of the frequency domain in response to the open-loop system. Nyquist stability criterion determines the stability of the closed-loop system based on the open-loop transfer function of that system.

The stability of a closed loop system can be determined by means of a characteristic equation, that is $F(s) = 1 + G(s)H(s)$ in the S-plane when s equals to the point on the Nyquist Path.

The study of the behavior of the plot, comparing with the origin in the S-plane is called the nyquist plot for $1 + G(s)H(s)$.

However, to simplify the things, it is easy to construct a nyquist plot for $G(s)H(s)$ in the $G(s)H(s)$-plane rather than $1 + G(s)H(s)$-plane.

There are two types of stability to be examined in any system

- Open-loop stability.
- Closed-loop stability.

By using the Nyquist criterion

- The stability of the open loop system can be found by studying the behaviour of the Nyquist plot for G(s)H(s) in relative to the origin of the G(s)H(s)-plane although the poles of G(s)H(s) are not known.
- The stability of the closed loop system can be found by studying the behaviour of Nyquist plot for G(s)H(s) in relative to the (-1,*j*0) point

5.10 NYQUIST PATH:

A path that goes in counter-clockwise direction that encloses the right-half-S-plane and does not pass through the poles of F(s) = 1+G(s)H(s) = 0, located in the imaginary axis instead the Nyquist path encircles half way and proceeds downwards.

5.11 ADVANTAGES OF NYQUIST PLOT :

- Nyquist plot provides information about the absolute stability of the system.
- The stability of a closed loop with pure time delay can be studied using Nyquist plot.
- It indicated relative stability giving the values of gain margin and phase margin.
- Frequency domain characteristics can be easily calculated from it.
- It is useful in analysing conditionally stable systems.

5.12 NYQUIST PLOT FOR COMPENSATED VFOA AND CFOA USING BJT:

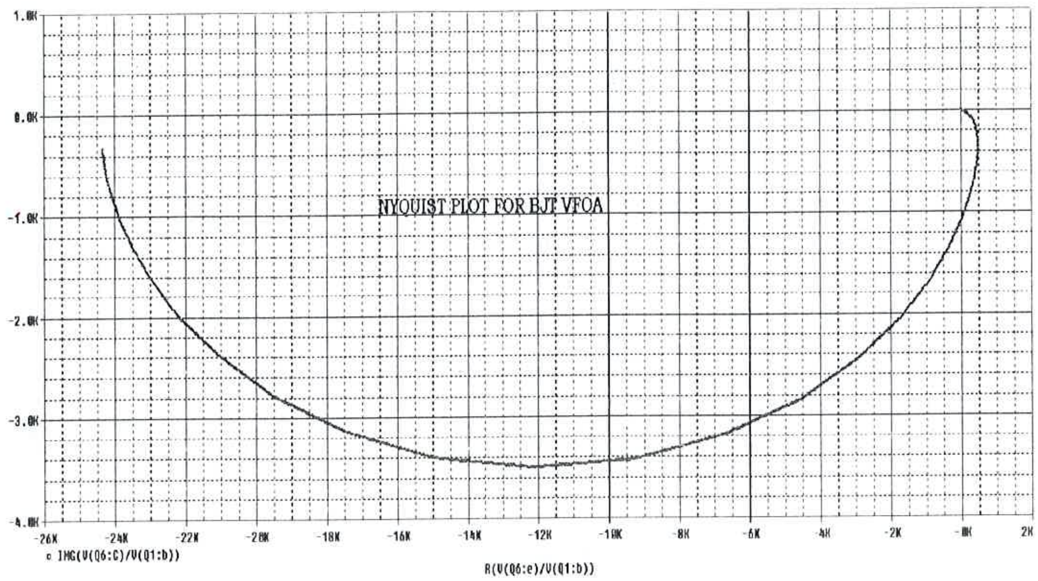

Figure 62 Nyquist plot for BJT VFOA

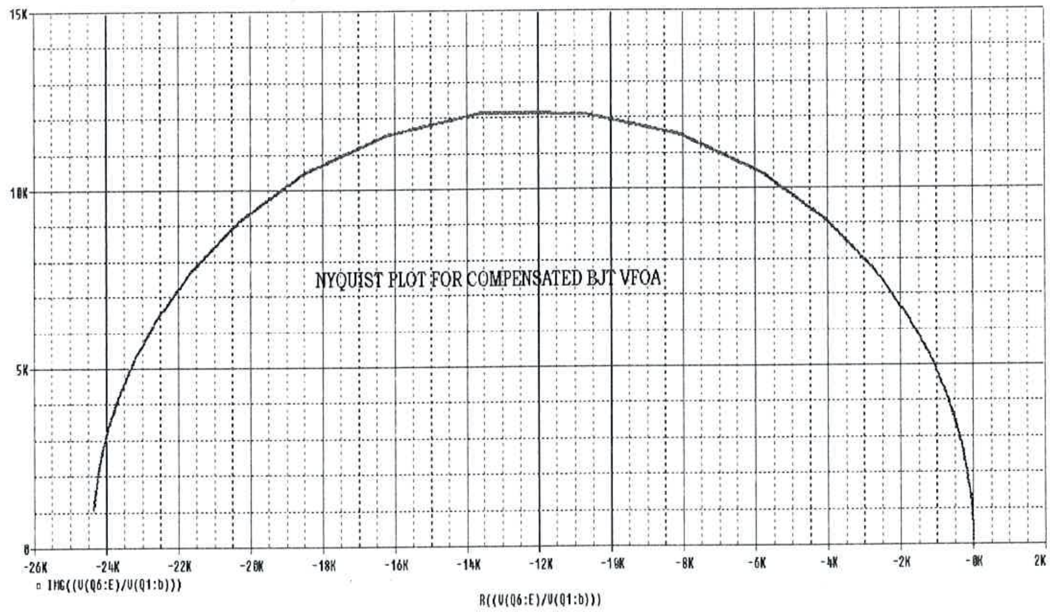

Figure 63 Nyquist plot for Compensated BJT VFOA

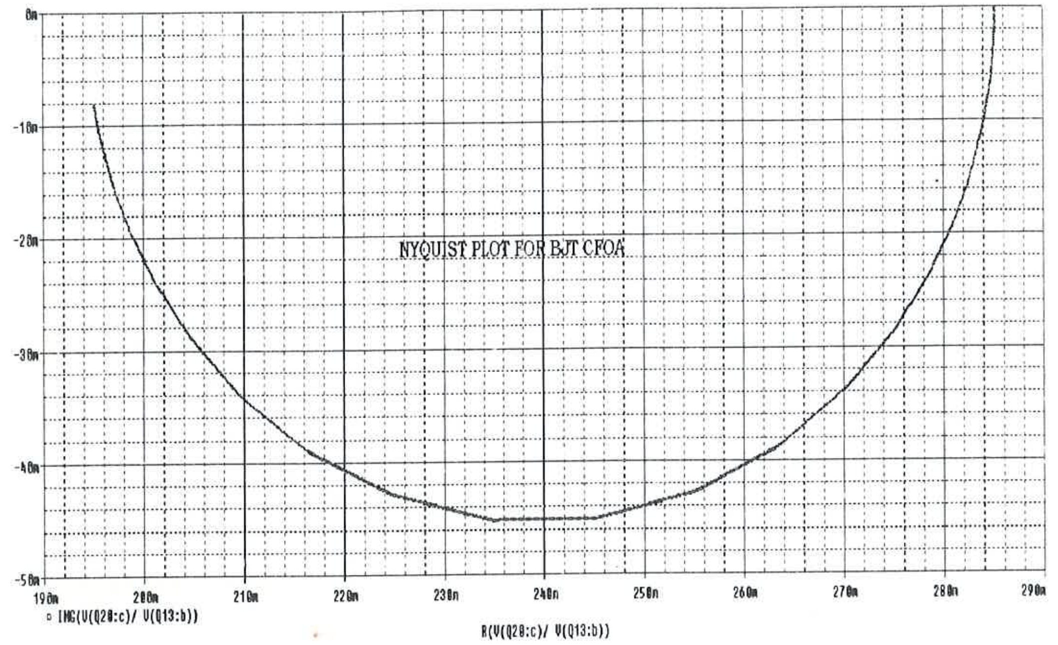

Figure 64 Nyquist plot for BJT CFOA

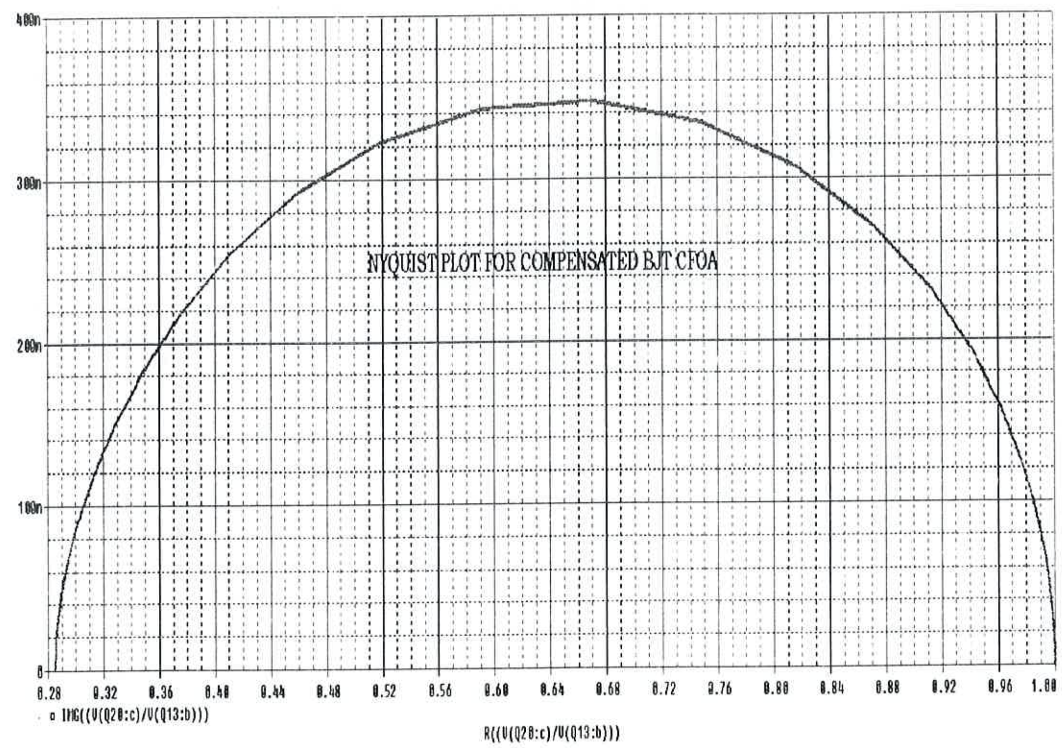

Figure 65 Nyquist plot for Compensated BJT CFOA

5.13 NYQUIST PLOT FOR COMPENSATED VFOA AND CFOA USING CMOS:

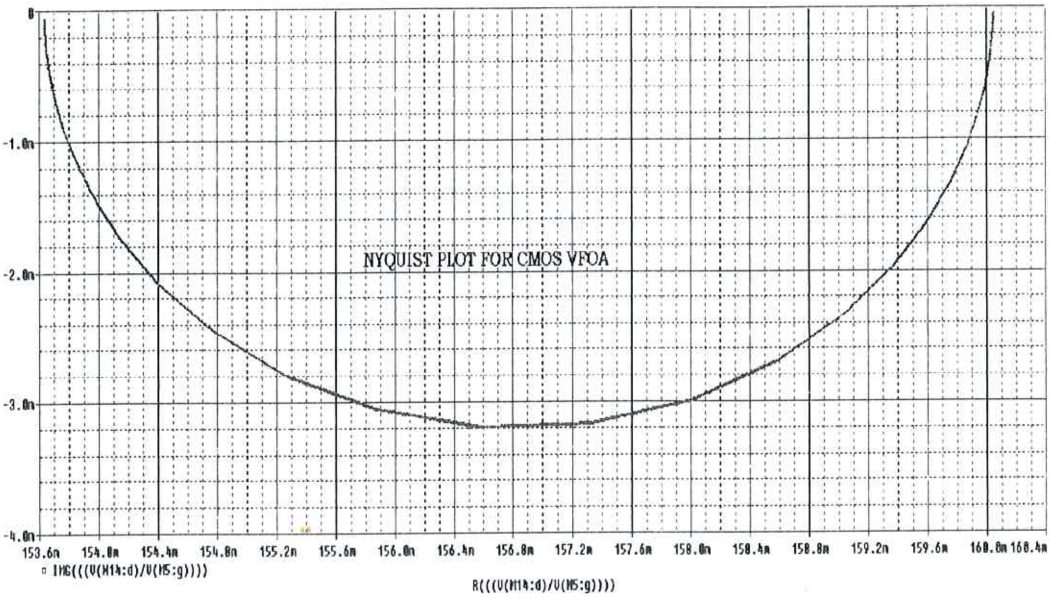

Figure 66 Nyquist plot for CMOS VFOA

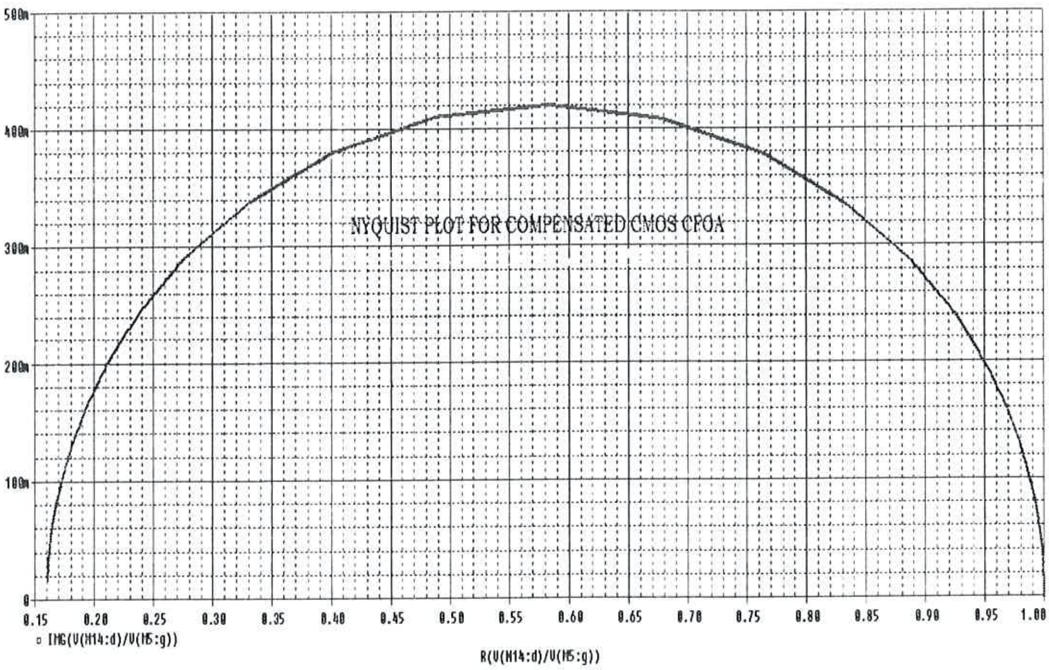

Figure 67 Nyquist plot for Compensated CMOS VFOA

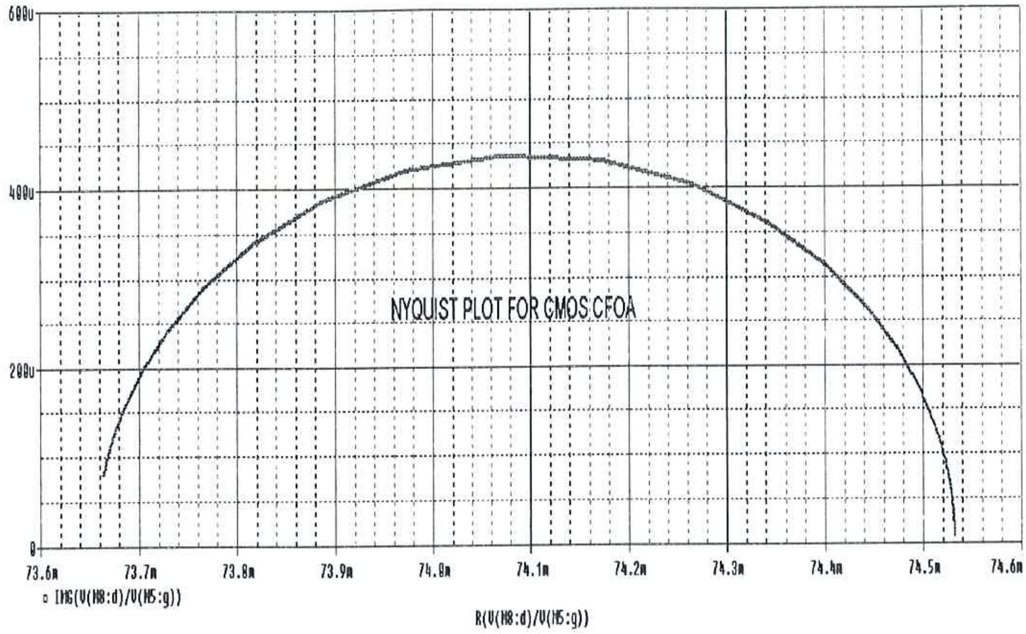

Figure 68 Nyquist plot for CMOS CFOA

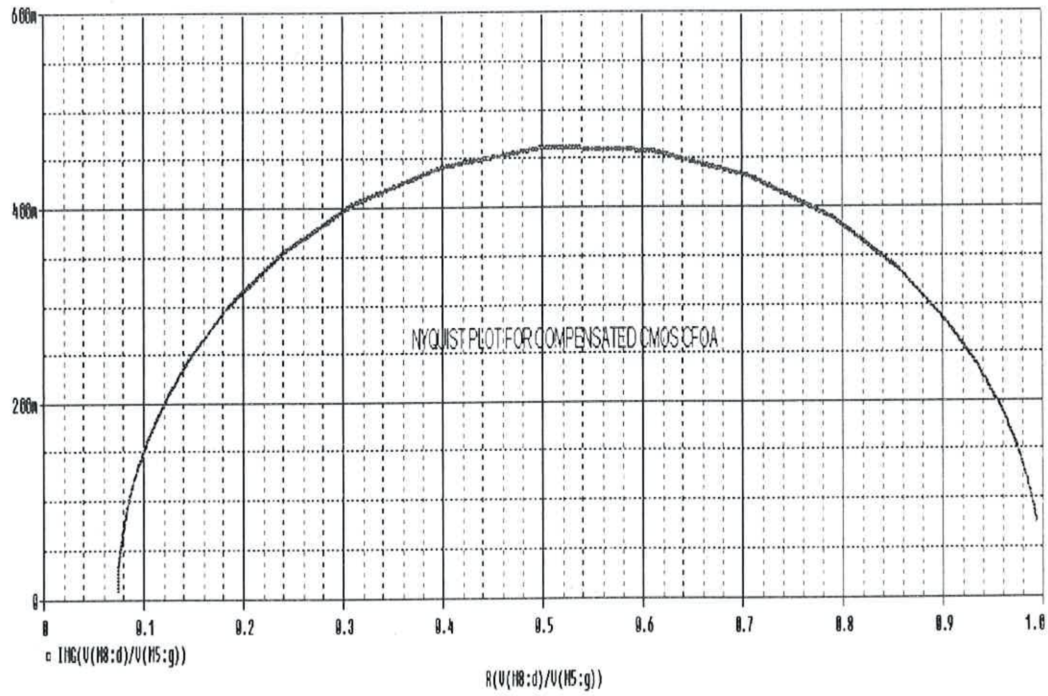

Figure 69 Nyquist plot for Compensated CMOS CFOA

CONCLUSION

Having studied the basics of an Op-Amp and understanding the working of the different stages of the amplifier and with development of more efficient circuits, the following conclusions can be made

- The Power dissipation in case of BJT operational amplifier is much more than CMOS op-amp.
- The circuits proposed for BJT voltage feedback has higher CMRR, almost double slew rate than the traditional circuits.
- The slew rate for CMOS op-amp is generally larger than BJT op-amp. Therefore the time taken to draw output from CMOS op-amp is less as compared to BJT op-amp.
- Current feedback op-amp have higher CMRR and skew rate than Voltage feedback op-amp. This makes them a preferable option in case of high-voltage applications.
- In case of Voltage feedback BJT op-amp, the non-inverting configuration is most efficient because it has highest value of CMRR and slew rate.
- In case of Voltage feedback CMOS op-amp, the non-inverting configuration is most efficient because it has highest value of CMRR and slew rate.
- In case of Current feedback BJT op-amp, the inverting configuration is most efficient because it has highest value of CMRR and slew rate.
- In case of Current feedback CMOS op-amp, the non-inverting configuration is most efficient because it has highest value of CMRR and slew rate.
- Using a parallel capacitor to the feedback resistance smoothens the frequency and phase response of the op-amp. Also similar phase response can now be achieved at a very low frequency by using parallel capacitor.
- Using compensation has improved the output frequency and phase response in op-amp. The phase response does not sink when compensation is applied for CMOS voltage feedback op-amp.
- Nyquist plots for uncompensated op-amps are negative while for compensated op-amp's are positive. This shows attainment of stability on applying compensation technique.

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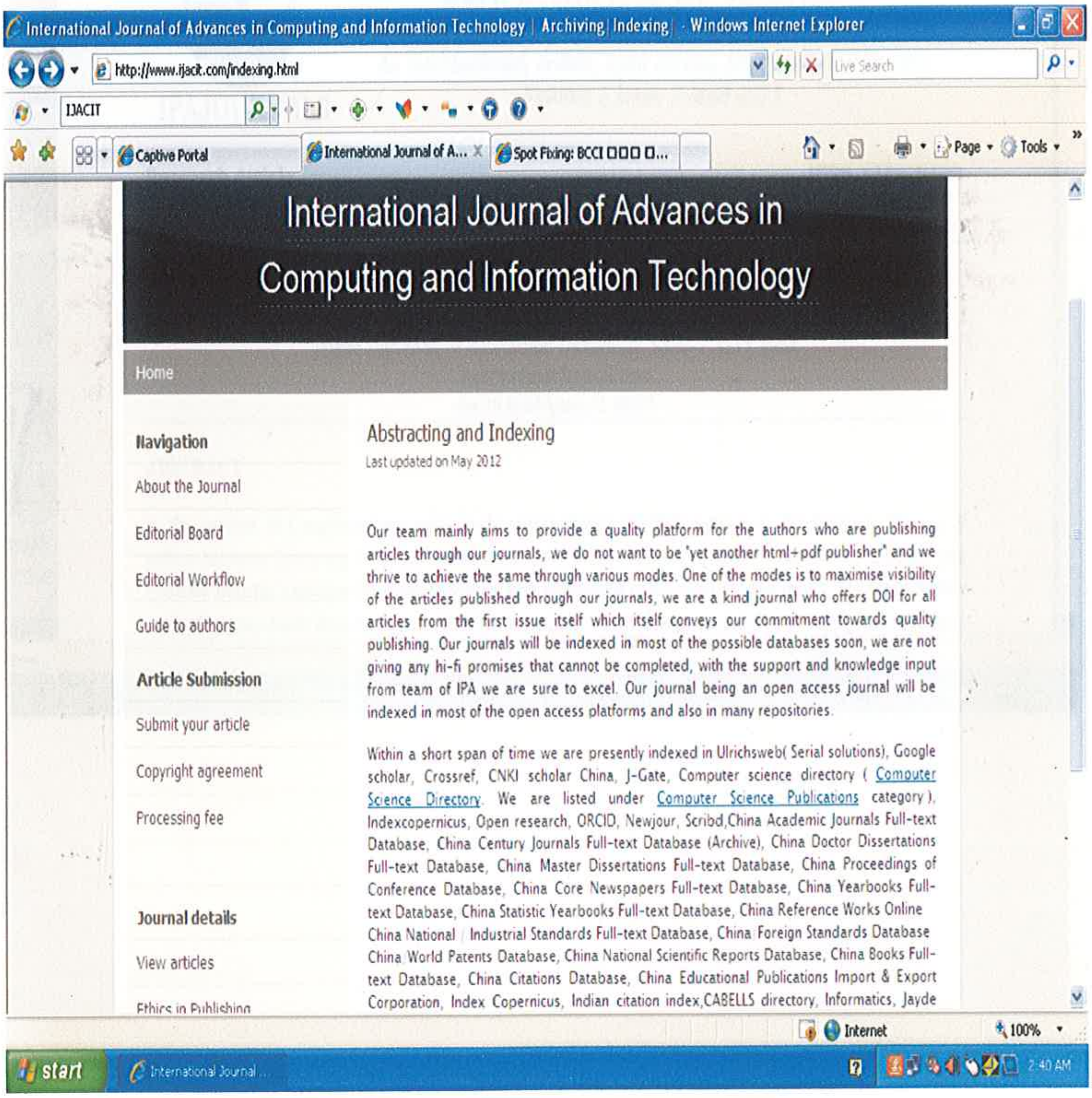
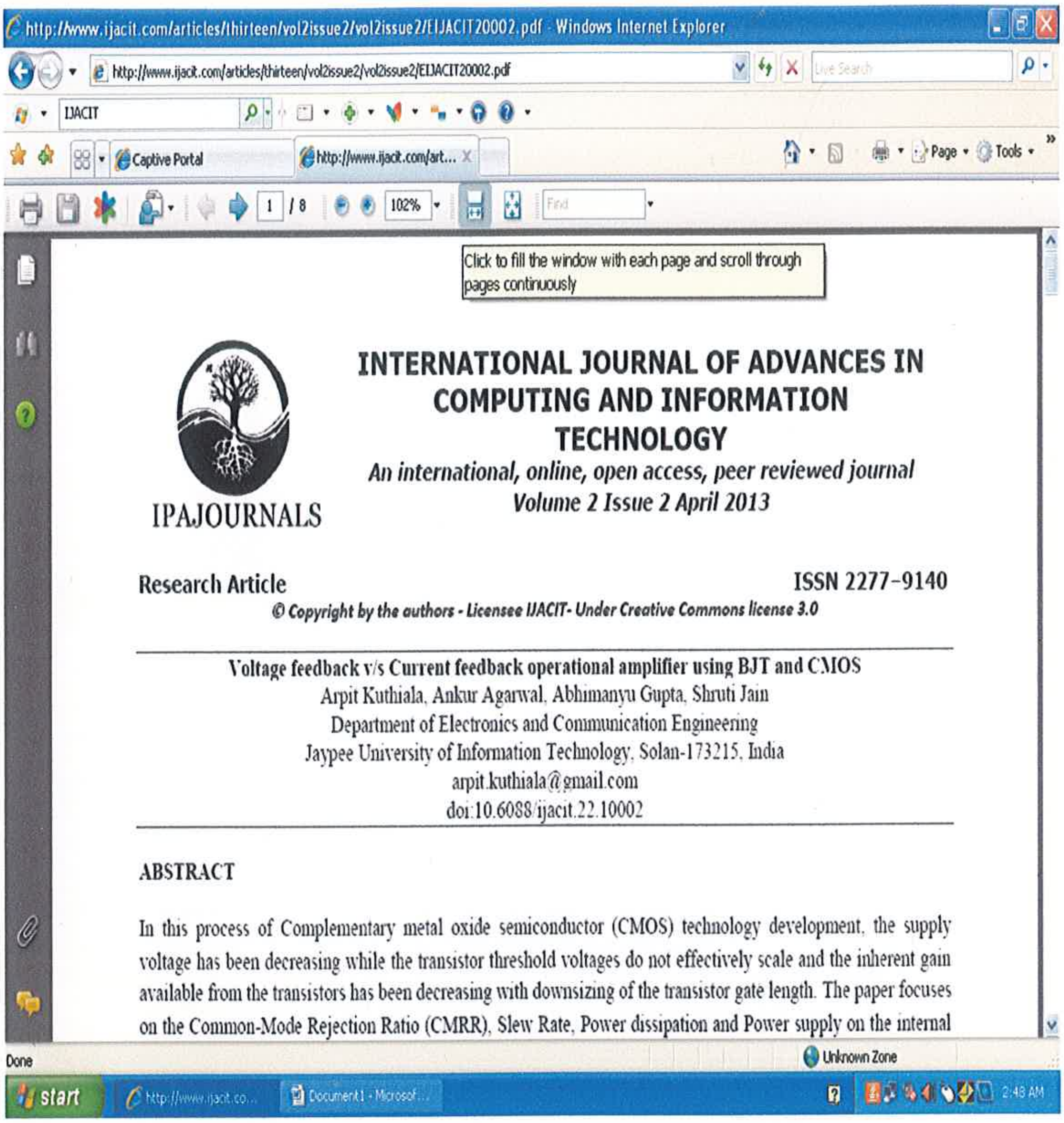
RESEARCH AND PUBLICATIONS

Paper titled " **Voltage feedback v/s current feedback operational amplifier using BJT and CMOS** " published in Volume 2 issue 2 April 2013 of International Journal of Advances in Computing and Information Technology (IJACIT)





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Voltage feedback v/s Current feedback operational amplifier using BJT and CMOS

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ABSTRACT

In this process of Complementary metal oxide semiconductor (CMOS) technology development, the supply voltage has been decreasing while the transistor threshold voltages do not effectively scale and the inherent gain available from the transistors has been decreasing with downsizing of the transistor gate length. The paper focuses on the Common-Mode Rejection Ratio (CMRR), Slew Rate, Power dissipation and Power supply on the internal