IMPROVING MOSFET CHARACTERISTICS

Project Report submitted in partial fulfillment of the requirement for the degree of

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In

Electronics and Communication Engineering

Under the Supervision of

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To

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Certificate

This is to certify that project report entitled "Improving MOSFET Characteristics", submitted by Shikha Sehrawat(091114), Sameer Kumar Misra(091120) and Tushar Gupta(091121) in partial fulfillment for the award of degree of Bachelor of Technology in Electronics and Communication Engineering to Jaypee University of Information Technology, Waknaghat, Solan has been carried out under my supervision.

This work has not been submitted partially or fully to any other University or Institute for the award of this or any other degree or diploma.

Date: 27-05-2013

Dr. Ghanshyam Singh

Designation

Acknowledgement

It is our esteemed pleasure to present a project report on "**IMPROVING MOSFET CHARACTERISTICS**".

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Abstract

High performance, high speed MOSFETs have been building blocks of high performance, high speed and high density integrated circuits, both analog and digital. During the past decade, excellent high speed and performance have been achieved through improved design, the use of higher quality material, and most importantly, gate length reduction. However, a major problem persists: Short channel effect.

The detrimental short channel effects occur when gate length is reduced to same order as the channel depth. The predominant features are lack of pinch-off and saturation and large leakage current. We have demonstrated that the dual material MOSFET structure is an effective means to overcome the short channel effects. The gate of DM-MOSFET consists of two laterally contacting materials with different work functions. This structure takes advantage of material work function difference in such a way that the threshold voltage near the source is more positive than near the drain (for n-channel device, opposite for p-channel), resulting in a more rapid acceleration of charge carriers in the channel and a screening effect to suppress the short channel effects. Using this structure, the principle, simulation results, design guidelines, processing and characterization are done in detail. Also, a brief discussion of Triple Material MOSFET (the improvement in Dual Material) has also been discussed.

Chapter 1: Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

1.1.History of Transistors

The transistor is the fundamental building block of modern electronic devices, and is ubiquitous in modern electronic systems. Developed by John Bardeen, Walter Brattain, and William Shockley at the Bell Laboratories on December 23, 1947. In 1954, IBM announced it was no longer planning to use vacuum tubes in its computers and introduced its first computer that had 2000 transistors. Transistors replaced vacuum tubes and today are found in virtually all electronic devices. A transistor stands for transfer resistance and it is a semiconductor device used to amplify and switch electronic signals and electrical power. A transistor regulates current or voltage flow and acts as a switch or gate for electronic signals. A transistor consists of three layers of a semiconductor material, each capable of carrying a current. A semiconductor is a material such as germanium and silicon that conducts electricity in a "semi-enthusiastic" way. It's somewhere between a real conductor such as copper and an insulator (like the plastic wrapped around wires).The semiconductor material is given special properties by a chemical process called doping. The doping results in a material that either adds extra electrons to the material (which is then called N-type for the extra negative charge carriers) or creates "holes" in the material's crystal structure (which is then called P-type because it results in more positive charge carriers).

The transistor's three-layer structure contains an N-type semiconductor layer sandwiched between P-type layers (a PNP configuration) or a P-type layer between N-type layers (an NPN configuration).A small change in the current or voltage at the inner semiconductor layer (which acts as the control electrode) produces a large, rapid change in the current passing through the entire component. The component can thus act as a switch, opening and closing an electronic gate many times per second.In 1954, IBM announced it was no longer planning to use vacuum tubes in its computers and introduced its first computer

that had 2000 transistors. Transistors replaced vacuum tubes and today are found in virtually all electronic devices.

Starting from the most fundamental switching device, the diode. Diodes were the first semiconductor electronic devices. The discovery of crystals' rectifying abilities was made by German physicist Ferdinand Braun in 1874. The first semiconductor diodes, called cat's whisker diodes, developed around 1906, were made of mineral crystals such as galena. Today most diodes are made of silicon, but other semiconductors such as germanium are sometimes used. However, unlike a resistor, a diode does not behave linearly with respect to the applied voltage as the diode has an exponential I-V relationship and therefore we cannot describe its operation by simply using an equation such as Ohm's law.

If a suitable positive voltage (forward bias) is applied between the two ends of the PN junction, it can supply free electrons and holes with the extra energy they require to cross the junction as the width of the depletion layer around the PN junction is decreased. By applying a negative voltage (reverse bias) results in the free charges being pulled away from the junction resulting in the depletion layer width being increased. This has the effect of increasing or decreasing the effective resistance of the junction itself allowing or blocking current flow through the diode. The depletion layer widens with an increase in the application of a reverse voltage and narrows with an increase in the application of a forward voltage. This is due to the differences in the electrical properties on the two sides of the PN junction resulting in physical changes taking place.

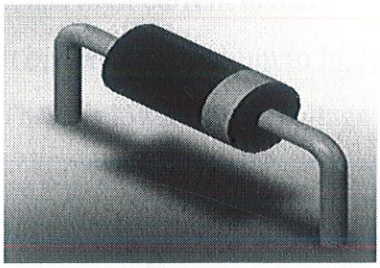
1.2.Diode as an On Switch

When a diode is connected in a Forward Bias condition, a negative voltage is applied to the N-type material and a positive voltage is applied to the P-type material. If this external voltage becomes greater than the value of the potential barrier, approx. 0.7 volts for silicon and 0.3 volts for germanium, the potential barriers opposition will be overcome and current will start to flow. This is because the negative voltage pushes or repels electrons towards the junction giving them the energy to cross over and combine with the holes being pushed in the opposite direction towards the junction by the positive voltage. This results in a

characteristics curve of zero current flowing up to this voltage point, called the "knee" on the static curves and then a high current flow through the diode with little increase in the external voltage as shown below.

1.3.Diode as an Off Switch

When a diode is connected in a Reverse Bias condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material. The positive voltage applied to the N-type material attracts electrons towards the positive electrode and away from the junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode. The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator. The result is that a high potential barrier is created thus preventing current from flowing through the semiconductor material.



1.4.Drawbacks of diode:

- Turn on and turn off characteristics of a diode is not under control.
- Following the end of forward conduction in diode, reverse current flows for a short time. The device doesn't attain its full blocking capability until the reverse current ceases.
- The reverse current flows in the interval called reverse recovery time. During this time, charge carriers stored in the diode at the end of forward conduction are removed.
- The recovery time is in range of a few μs(1-5)μs in a conventional diode to several hundred nanoseconds in fast recovery diodes.
- This recovery time is of great significance in high frequency operation.

1.5.Bipolar Junction Transistor

The invention of the bipolar transistor in 1948 ushered in a revolution in electronics. Technical feats previously requiring relatively large, mechanically fragile, power-hungry vacuum tubes were suddenly achievable with tiny, mechanically rugged, power-thrifty specks of crystalline silicon. This revolution made possible the design and manufacture of lightweight, inexpensive electronic devices. . It is a three-terminal electronic device constructed of doped semiconductor material. It is called 'Bipolar' because charge is carried by both, electrons and holes. Hence, operation of the device is due to bi poles (or opposite charges). Charge flow in a BJT is due flow of charges flow across a junction between two regions of different charge concentrations. The following are the advantages of BJT:

- It has high current density.
- It operates in medium to high voltage range.
- There is low forward voltage drop.

1.6.Advantages Of MOSFET

1.6.1 MOSFET Impedance

MOSFETs have higher input impedance than BJTs. The input impedance is a measure of the resistance of the input terminal of the transistor to electrical current. Higher input impedance allows any amount of voltage to be fed into the load without absorbing power thus making the operation of a transistor better in an electrical circuit.

Size: MOSFETs can be made much smaller than BJTs. Many more MOSFETs can be placed in a smaller area than BJTs, thus increasing the packing density.

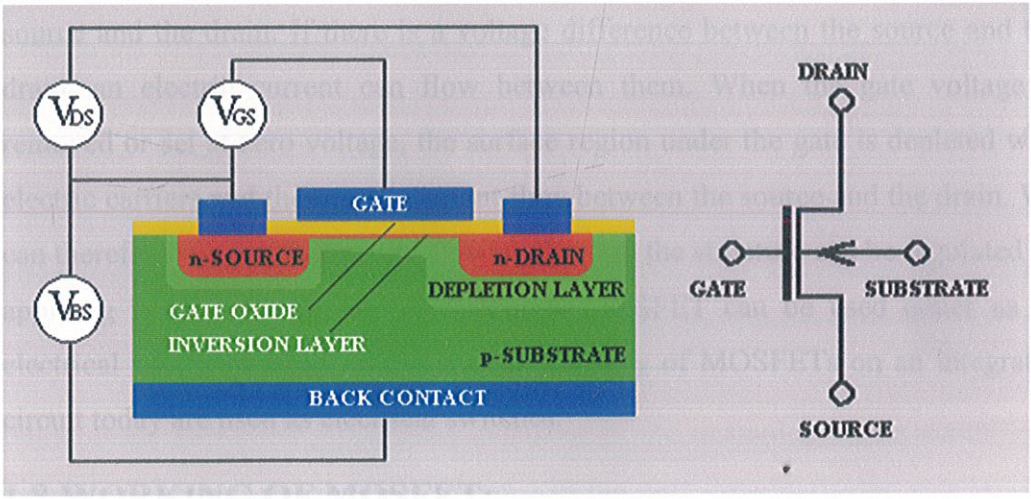
Easy to manufacture: MOSFETs are also easier to manufacture than BJTs because they take fewer steps to make.

Noise Immunity: MOSFETs are less noisy than BJTs. In an electronics context noise refers to random interference in a signal. When a transistor is used to

amplify a signal the internal processes of the transistor will introduce some of this random interference. BJTs generally introduce more noise into the signal than MOSFETs.

Thermal Runaway: BJTs suffer from a property known as "thermal runaway." Thermal runaway happens because it has negative temperature coefficient. It means as the temperature increases the resistance decreases and thus the conductivity of a BJT increases. Because transistors tend to heat up in proportion to current flowing through them this means that the conductivity and temperature of BJTs can increase exponentially. This can damage the BJT and makes designing circuits for BJTs more difficult. MOSFETs do not suffer from thermal runaway since they have negative temperature coefficient.

Power Consumption: MOSFET consumes lesser power and is therefore more efficient.



1.7.The MOSFET

Metal oxide semiconductor field-effect transistor, is a fundamental switching device in very-large-scale integrated (VLSI) circuits. A MOSFET has at least three terminals, which are designated as gate, source, and drain. The gate electrode is separated electrically from the source and the drain by a thin dielectric film, usually silicon dioxide. The source and the drain are doped with impurities that are opposite in polarity to the substrate, which is doped with boron for N-channel transistors and with arsenic or phosphorous for P-channel transistors. This source, substrate, and drain doping effectively produces two back to-back junction diodes from the source terminal to the drain terminal. When a sufficiently large positive voltage is applied to the gate of an N-channel transistor (which creates an electric field, hence the field effect), the silicon surface is ''inverted''—the conduction band is populated and forms a narrow conducting layer between the source and the drain. If there is a voltage difference between the source and the drain, an electric current can flow between them. When the gate voltage is removed or set at zero voltage, the surface region under the gate is depleted with electric carriers and there is no current flow between the source and the drain. We can therefore see that the current flowing through the structure can be regulated by applying voltage to the gate electrode. A MOSFET can be used either as an electrical switch or as an amplifier. The majority of MOSFETs on an integrated circuit today are used as electrical switches.

1.8.WORKING OF MOSFET:

There are three regions of operation in a MOSFET

- $0<V_{gs}<V_T$: The gated region between the source and drain is depleted and no carrier flow is observed, $I_d=0V$. The MOSFET is said to operate in the cut-off region. Now as the gate voltage is increased beyond the threshold voltage, the mid gap energy level at the surface is pulled below the Fermi level, causing the surface potential to turn positive and to invert the surface.
- $V_{gs}>V_t$ and $V_{ds}=0$: Thermal equilibrium exists in the inverted channel and Id=0. If a small drain voltage V_{ds} is applied, a drain current proportional to V_{ds} will flow from the source to the drain through the conducting channel. Now the device

operates in linear region. As the drain voltage is increased the inversion layer charge and the channel depth at the drain end start to decrease. Eventually at $V_{ds}=V_{ds\ sat}$, the inversion charge at the drain end is reduced to zero, which is called the pinch off point.

- $V_{gs}>V_t$ and $V_{ds}>V_{dssat}$:a depleted surface region forms adjacent to the drain, and this depletion region grows towards the source with increasing drain voltages. This operation mode of the MOSFET is called the saturation mode.

Today the world is continuously striving to advance the technology by reducing the minimum feature size of integrated circuits. This has helped the microelectronic industry to produce products with spectacular increase in computational capability and integration density at lower cost. Smaller transistors operate faster than larger ones, and for a given chip technology, the cost of a chip decreases with area rather than with the number of transistors. The exponential scaling trend surely will eventually hit fundamental limits, but the many predictions of a near-term end of device scaling have proven too pessimistic. How fast a MOSFET can be switched on and off is therefore a critical figure of merit to determine the competitiveness of the technology. The two major factors that control the speed of MOSFETs are the channel length from the source to the drain and the speed at which channel charge carriers travel from the source to the drain. With the introduction of the production of 90-nm node technology in 2004, the semiconductor industry is entering the Bnano[era(1). (The B90-nmnode[refers to the smallest half-pitch metal lines available in the technology. The actual gate lengths of the devices are about 50 nm.) In the next decade, device gate lengths will be scaled to below 10 nm . We discuss below the challenges in device scaling and possible solutions in maintaining the performance trend.

1.9.Shrinking the Transistor

Shrinking transistors not only packs more devices into a given area but also shortens the distance between source and drain, or the gate length, which can improve the switching speed. The two challenges in decreasing MOSFET size are

fabrication and maintaining performance. The backbone of MOSFET fabrication is a process called lithography, which resembles the printing of a photograph by shining light through a negative onto a photosensitive surface. Lithography allows complex patterns to be created through a series of printing and etching steps. The ability to print ever-smaller fine lines is mandatory for continued device scaling. Advanced photolithography techniques have enabled the industry to keep pace with the demand imposed by increasingly smaller structures. However, the smallest feature size is related to the fundamental limit of wavelength used in conventional optical lithography. Alternative technologies capable of writing features far smaller than those produced by conventional optics have also been demonstrated and include the use of extreme ultraviolet (EUV) radiation, x-rays, and electron beams. Recently, the self-assembly process has attracted much attention because of its potential in producing nanoscale patterns. The concern is whether any of these alternatives can be scaled up to meet the throughput, control, and cost requirements for manufacturing. Given the ability to create smaller device features, to what extent can the gate length be reduced before the MOSFET ceases to function as a switch? The gate terminal can lose the control of channel electric carriers when the source and the drain are brought into proximity without scaling.

MOSFET can be described as a short channel device if the effective channel length is approximately equal to the source and drain junction depths. The short channel effects that arise in this case are attributed to two physical phenomena:

- The limitations imposed on electron drift characteristics in the channel.
- The modification of the threshold voltage due to the shortening channel length.

1.10. Types of Short Channel Effects

- Drain induced barrier lowering: As we know when the gate to source voltage is less than the threshold voltage, the device acts as an OFF. But in case of short channel even if the gate to source voltage is less than threshold voltage but the

drain voltage is increased then the device gets turned ON ,thereby the revealing that the control of the gate over the channel has reduced.

- Surface Scattering: As the channel length decreases the electric field in the vertical direction in the channel increases, due to which electrons going towards the drain have to undergo large number of collisions from those going towards interface.
- Velocity Saturation: At low electric field drift velocity of electrons is proportional to electric field. But as electric field increases with decrease in channel length, drift velocity reaches saturation value
- Impact Ionization: High velocity electrons moving in the channel generate electron-hole pairs by ionization.
- Hot Electrons: High energy electrons due to the high electric field can enter the oxide layer, where they can be trapped and cause permanent change in oxide interface charge density.

MOSFETId-VdsCharacteristics

- For Vgs<V_T, I_d= 0

As VDS increases at a fixed Vgs,$I_d$increases in the triode region due to the increased lateral field, but at a decreasing rate since the inversion layer density is decreasing.

- Once pinch off is reached, further V_{ds}increases only increase $I_D$due to the formation of the high field region The device starts in triode, and moves into saturation at higher V_{ds}

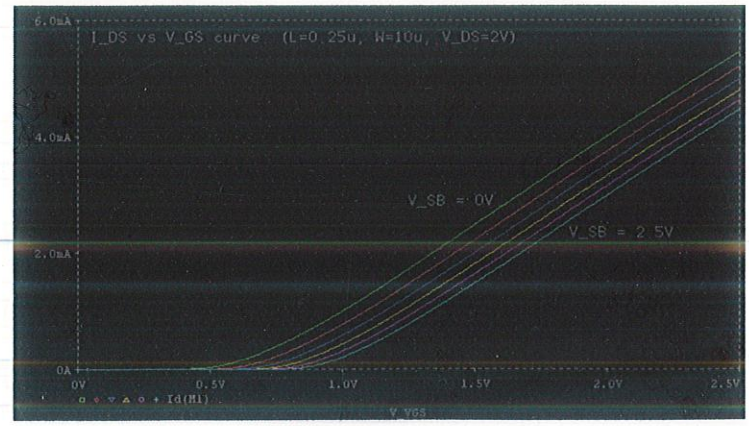


Figure 1: MOSFET Id-Vds Characteristics simulated in PSPICE

MOSFET Id-Vgs Characteristics

- As Idis increased at fixed V_{ds}, No current flows until the inversion layer is established.
- For Vgsslightly above threshold, the device is in saturation since there is little inversion layer density (the drain end is pinched off).
- As V_{gs}increases, a point is reached where the drain end is no longer pinched off, and the device is in the triode region.A larger V_{DS}value postpones the point of transition to triode

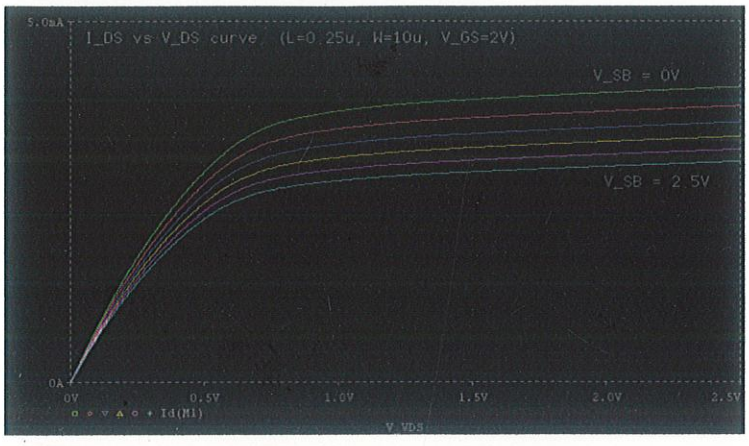


Figure 2: MOSFET I_d-V_{gs} Characteristics simulated in PSPICE

CHAPTER 2: Dual Material MOSFET

2.1 Introduction:

High performance and high speed Metal Oxide Semiconductor Field Effect Transistors have been building blocks of high performance, high speed , high density integrated circuits, both analog and digital. During the past decade, excellent high speed and performance have been achieved through improved design , the use of higher quality material and most importantly, gate length reduction. However, a major problem persists, 'short channel effect'.

It has been demonstrated that the Dual Gate FET structure is an effective means to overcome short channel effects, due to the screening of the drain voltage by the second gate

In a field effect transistor, electrons enter into the channel with a low initial velocity, gradually accelerating toward the drain. The electrons move very fast in the region near the drain but relatively slow in the region near the source. Hence, the speed of the device is affected by a relatively slow electron drift velocity in the channel near the source region. We use two different materials with different work functions for the two gates in a DG-FET and merge them into one single gate by making them contacting laterally to obtain a new device structure-dual material gate (DMG) MOSFET.

In addition, we select a material with higher work function as the gate's material 1, which is close to the source, and a material with lower work function as material 2, which is close to the drain. The concept of and improvement of carrier transport efficiency are thus realized. More importantly, a step function in channel potential ensues, which is the fundamental reason why the DMG structure can also reduce short-channel effects without sacrificing other device behavior as in the case of dual gate or other gate structures.

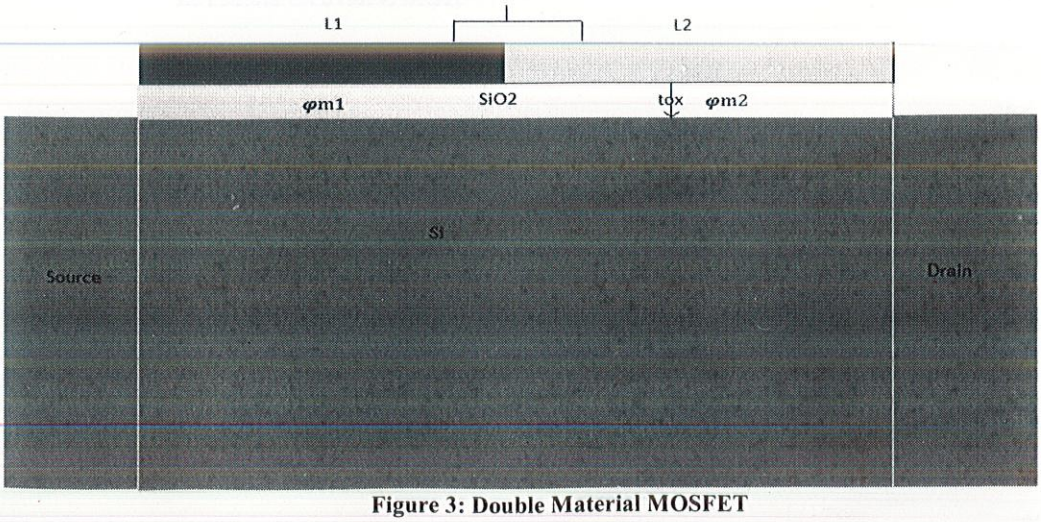


Figure 3: Double Material MOSFET

Double Material MOSFETs offer a number of advantages viz. low power dissipation, higher operating speed, denser packing, elimination of latch-up, simpler design, radiation-hardness and improved immunity to short channel effects. They can be either fully . The focus of this research is on decreasing short channel effects in MOSFETs. With the continuous down scaling of the CMOS technology into the deep-submicron era, the control of the gate on the threshold voltage decreases as the channel length shrinks because of the increased charge sharing from source and drain. Therefore the threshold voltage reduction with decreasing channel lengths and drain induced barrier lowering are the issues that need to be addressed while providing immunity against short channel effects (SCEs).

In a DMG-MOSFET, the work function of metal gate 1 (M1) is greater than metal gate 2 (M2) i.e., φM1 > φM2 for an n-channel MOSFET and vice-versa for

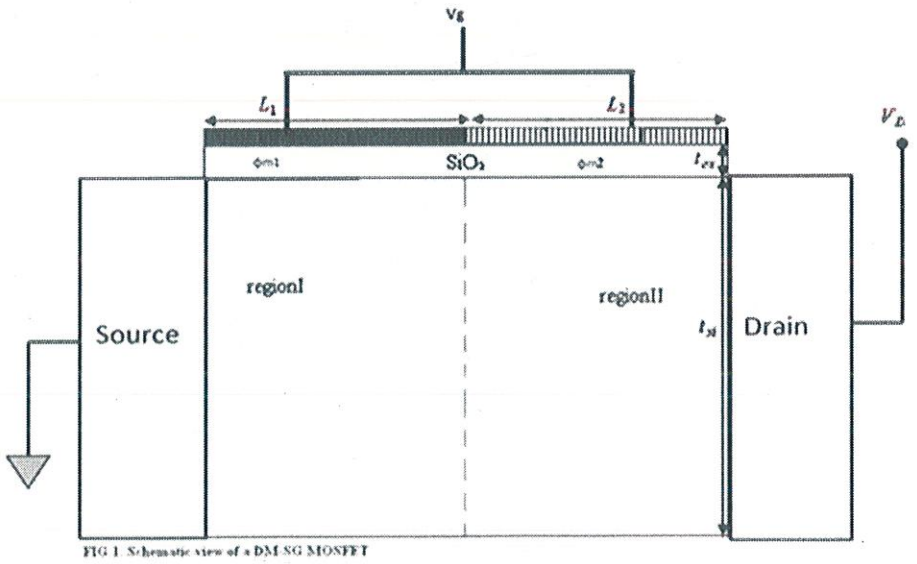


FIG 1 Schematic view of a DM SG MOSFET

Figure 4: Dual Material Schematic

p-Channel MOSFET. The aim of this work is, therefore, to study for the first time the potential benefits offered by the DMG gate in suppressing the short-channel effects in MOSFETs using two-dimensional modeling and numerical

simulation.As the channel length shrinks, the control of gate voltage on the threshold voltage decreases due to increased charge sharing from source and drain. Therefore, the threshold voltage reduction with decreasing channel lengths and drain induced barrier lowering (DIBL) are important issues that need to be addressed while providing immunity against short-channel effects (SCEs).To enhance the immunity against short channel effects, a new structure called dual material gate (DMG) MOSFET was proposed. The structure, which uses two metals in the gate M1 and M2 with different work functions, provides simultaneous increase in trans conductance and suppressed SCEs. In the DMG structure, the peak electric field at the drain end is reduced which ensures that the average electric field under the gate is increased. The step in the potential profile ensures screening of the channel region under the gate material on the source side (M1) from variations in the drain potential. To incorporate the advantages of DMG structures, we, in this research work, propose a new structure for dual material gate (DMG) MOSFETs.

2.3 Calculation of Drain Current of DMG MOSFET

Calculation of Drain Current of the DMG MOSFET is same as with the Classical MOSFET but with a little Change In Algorithm. In this method we use the method of hypothetical MOSFET and add their current together as one.

2.3.1 Method Of Calculation

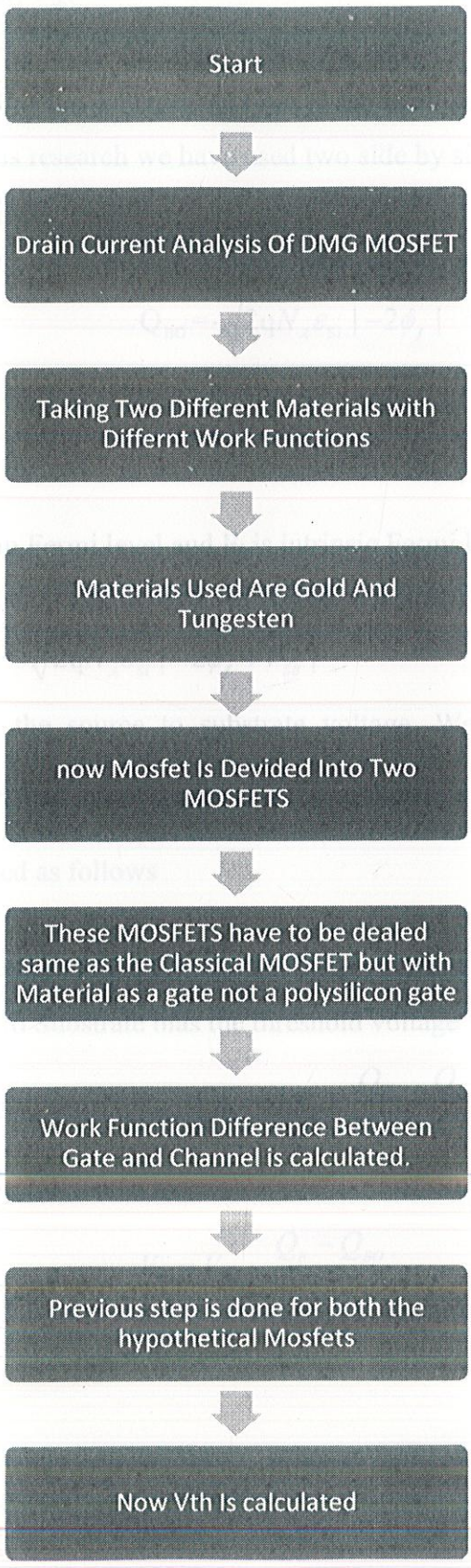


Figure 5:Method Used For Calculation

2.4 Numerical Calculations

2.4.1 Threshold Voltage

To calculate the VT following parameters affecting the threshold voltage are explained below: $\phi_{gc} = \phi_f(substrate) - \phi_m(metal)$

Where ϕgc is the work function difference between gate and channel, ϕf is the Fermi potential of the substrate and ϕm is the work function of the metal gate we are using. In this research we have used two side by side connected materials with ϕm1 = 4.8eV, ϕm2 = 4.6eV

We can calculate the depletion region charge density at surface inversion using

$$Q_{BO} = -\sqrt{2qN_A\varepsilon_{Si}\,|-2\phi_f|}$$

Where Na is acceptor concentration, Ɛsi=11.7Ɛ0 and to calculate ϕf we have

$$\phi_f = \frac{E_f - E_i}{q}$$

E_f is equilibrium Fermi level and E_i is intrinsic Fermi level.

Depletion region charge density expressed as a function of the source to substrate voltage is $Q_{BO} = -\sqrt{2qN_A\varepsilon_{Si}\,|-2\phi_f + V_{SB}|}$

Where V_{SB} is the source to substrate voltage. We Have Cox as gate oxide capacitance per unit area $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$. For zero substrate bias the threshold voltage VTo is expressed as follows

$$V_{TO} = \phi_{gc} - 2\phi_f - \frac{Q_{BO}}{C_{OX}} - \frac{Q_{ox}}{C_{ox}}$$

and For non-zero Substrate bias the threshold voltage VT is expressed as follows

$$V_{TO} = \phi_{gc} - 2\phi_f - \frac{Q_B}{C_{OX}} - \frac{Q_{ox}}{C_{ox}}$$

and now VT Can be calculated as

$$V_T = V_{TO} - \frac{Q_B - Q_{BO}}{C_{ox}}.$$

Drain Current

$$I_D(lin) = \frac{\mu_p C_{OX}}{2} \cdot \frac{W}{L} \cdot \left[2.\left(V_{gs} - V_T\right)V_{ds} - \left(Vds\right)^2 \right]$$

Now as we have two drain currents with us after the calculations i.e. I_{d1} for the region 1 and I_{d2} For the region 2 hence we now See the Direction of the current Flowing According as we know it flows from source to drain we can now just add both the currents i.e. Id1+Id2

Hence we can get the Drain Current for the following DMG MOSFET

CHAPTER 3: Poisson Analysis

3.1.Poisson's Equation and its application in MOSFET

Poisson's equation is a partial differential equation named after the French mathematician and physicist Simeon-Denis Poisson. Derived from Coulomb's law and Gauss's law, it is a second-order partial differential equation used for solving problems, such as finding the electric potential for a given charge distribution, or modeling gravitational fields. It is commonly used in the fields of electrostatics, mechanical engineering, and theoretical physics.

The Poisson equation is

$$\Delta\phi = f$$

Where, Δ is the Laplace operator, and $f \& \phi$ are real or complex valued functions. The Laplace operator is often denoted as ∇^2 and so, the Poisson equation is frequently written as

$$\nabla^2\phi = f$$

In three dimensional Cartesian coordinates, it takes the form

$$(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}).\phi(x,y,z) = f(x,y,z)$$

For vanishing f, it becomes Laplace's equation.

$$\nabla^2\phi = 0$$

The Poisson equation may be solved using a Green's function

3.2.How to solve using Green's function: an example

Suppose we have a differential equation of the form

$$y'' - y = 0 \qquad \text{(i)}$$

With the boundary conditions,

$$y(0) = y(1) = 0 \qquad \text{(ii)}$$

In this case, let $\frac{d}{dx} = D$, substituting this in equation (i), we get

$$(D^2 - 1)y = 0$$

Solving this expression, we get $D = \pm 1$

For an equation of the form of equation (i), the Green's function is of the form

$$y(x) = A\sinh(x) + B\cosh(x) \qquad \text{(iii)}$$

Using the given boundary conditions, we will find the constants A and B which come out as 0 and 0 respectively. Having the constants as 0 implies that we have a trivial solution and now, the Green's function can be constructed for the given equation using the following steps

Substituting $B = 0$, we get $y(x) = \sinh(x)$. For $A = 1$, $y_1(x) = \sinh(x)$.

From the boundary conditions, $y(1) = 0$, using (iii) we get

$$A\sinh(1) + B\cosh(1) = 0$$

$$\Rightarrow A = \frac{-B\cosh(1)}{\sinh(1)},$$

Substitute this value in (iii) to get the following simplified expression

$$y(x) = B\frac{\sinh(x-1)}{\sinh(1)} \qquad \text{(iv)}$$

Now assume B in such a way so that (iv) is in a simple form. We have assumed $B = \sinh(1)$ so the denominator cancels out with B. So we get,

$$y_2(x) = \sinh(x-1)$$

Now, we have to find the Wronskian ,

$$W(y_1(t), y_2(t)) = \begin{pmatrix} y_1(t) & \cdots y_2(t) \\ \vdots & \ddots \quad \vdots \\ y_1'(t) & \cdots y_2'(t) \end{pmatrix}$$

This comes out to be $\sinh(1)$

Now, the green's function is defined as

$$G(x,t) = \begin{Bmatrix} \frac{-y_1(x).y_2(t)}{c}, 0 \le x < t \\ \frac{-y_1(t).y_2(x)}{c}, t < x \le 1 \end{Bmatrix}$$

Where, $c = p(t)W(y_1(t), y_2(t))$

So, the solution for (i) , using Green's function comes out to be

$$G(x,t)=\begin{cases}\dfrac{\sinh(x).\sinh(t-1)}{\sinh(1)}, 0\le x<t\\ \dfrac{\sinh(t).\sinh(x-1)}{\sinh(1)}, t<x\le 1\end{cases}$$

So, the basic steps to find solution using Green's equation were as explained above and Green's function, G, must satisfy the following conditions:

- G must satisfy the boundary conditions
- G must be continuous at x=t
- Jump Discontinuity

$$\left.\frac{\partial G_2}{\partial x}\right]_{x=t+0} - \left.\frac{\partial G_1}{\partial x}\right]_{x=t-0} = -\frac{1}{p(t)}$$

3.3. **Poisson's Equation Applied in Single Material** MOSFET

We have obtained an analytical solution for the potential distribution of the two-dimensional Poisson's equation with given boundary conditions for MOSFET by using Green's function method and the effects of source and drain junction curvature and depth are properly considered.

For a very large scale integration of MOS circuits, the miniaturization of the MOSFET device has been the trend of technology development. However, due to scaling of device channel length, the short channel length effects become extremely important, which have been shown to deteriorate some important device characteristics. Due to high sensitivity of the electrical characteristics of short channel MOSFET's to the process fluctuation, the device design to satisfy a given circuit performance is becoming more difficult, but the problems can be solved by using an accurate device analysis.

Here, a generalized method to solve the electrostatic potential of the two dimensional Poisson's equation for a MOSFET operated in the sub threshold region has been explained.

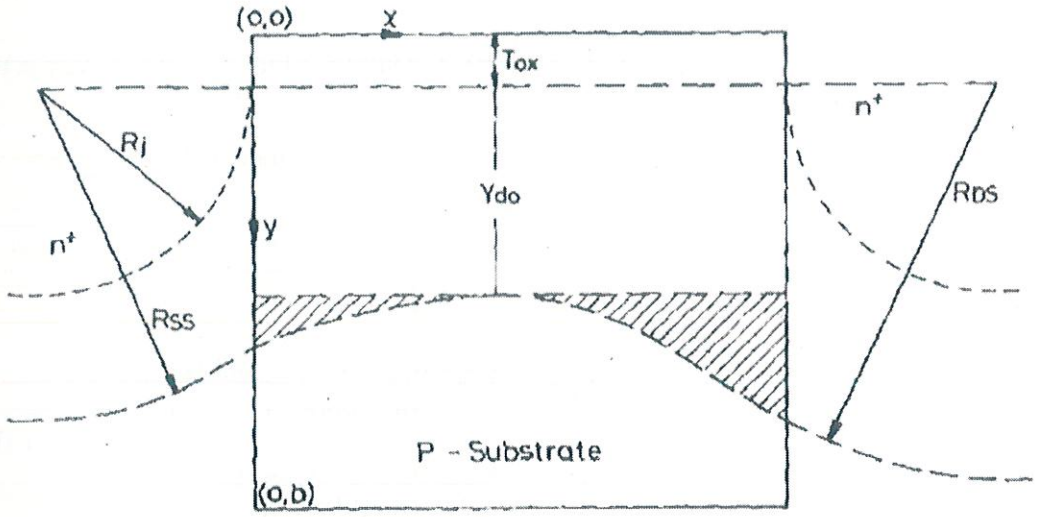


Figure 6: Rectangular Co-ordinate system of MOSFET

The finite source-drain junction depth is approximated by the cylindrical junction with a radius R

3.4.ANALYTICAL CALCULATIONS FOR THE POTENTIAL DISTRIBUTION

3.4.1 Green's Function

Considering the two-dimensional Poisson's equation in a rectangular coordinate system as shown in the figure, the differential equation for the potential distribution in an n-channel MOS structure can be written as

$$\nabla^2\Psi(x,y)=\begin{cases}0, 0<y<T_{ox}\\ -\dfrac{\rho(x,y)}{\varepsilon_{si}}=\dfrac{qN_Af(y)}{\varepsilon_{si}}, T_{ox}<y<Y_d(x)\end{cases}$$

Where N_A is the substrate doping concentration and f(y) is the non-uniform doping function.

The solution of the two-dimensional Poisson's equation in a finite region with the given boundary conditions can be obtained by the means of Greens' function technique as explained earlier.

Potential distribution is given by the following expression

$$\Psi(x,y)=\iint\frac{\rho(x',y')}{\varepsilon}G(x,y;x',y')dx'dy'-\oint\phi(x',y')\frac{\partial G}{\partial n'}ds' \quad \text{(i)}$$

The Green's function G for the rectangular system shown in the figure is given by

$$G(x,y;x',y') = \frac{2}{L}\sum_{m=1}^{\infty}\sin(k_m x)\sin(k_m x')H(y;y';k_m)$$

$$= \frac{2}{b}\sum_{n=1}^{\infty}\sin(k_n y)\sin(k_n y')F(x;x';k_n) \qquad \text{(ii)}$$

In which $H(y;y';k_m)$ and $F(x;x';k_n)$ are

$$H(y;y';k_m) = \begin{cases} \dfrac{\sinh(k_m y)\sinh k_m(b-y')}{k_m \sinh(k_m b)}, y < y' \\ \dfrac{\sinh(k_m y')\sinh k_m(b-y)}{k_m \sinh(k_m b)}, y' < y \end{cases}$$

$$F(x;x';k_n) = \begin{cases} \dfrac{\sinh(k_n x)\sinh k_n(L-x')}{k_n \sinh(k_n L)}, x < x' \\ \dfrac{\sinh(k_n x')\sinh k_n(L-x)}{k_n \sinh(k_n L)}, x' < x \end{cases}$$

Where, $k_m = \dfrac{m\pi}{L}$ and $k_n = \dfrac{n\pi}{b}$

Substituting (ii) into (i) , and on further simplification, we obtain

$$\psi_0(x,y) = \sum_{m=odd}^{\infty}\sin(k_m x)\frac{\rho_A(m)}{\varepsilon}\int_{T_{ox}}^{T_{ox}+Y_{d0}} f(y')H(y;y';k_m)dy'$$

$$+\sum_{m=odd}^{\infty}\sin(k_m x).\frac{\sinh k_m(b-y)}{\sinh(k_m b)}.\frac{4V'_{GS}}{m\pi}+\sum_{m=odd}^{\infty}\sin(k_m x).\frac{\sinh(k_m y)}{\sinh(k_m b)}.\frac{4V_{BS}}{m\pi}+$$

$$\sum_{n=1}^{\infty}\sin(k_n y).\frac{\sinh k_n(L-x)}{\sinh(k_n L)}.\frac{2}{b}\int_0^b \phi(0,y')\sin(k_n y')dy'+$$

$$\sum_{n=1}^{\infty}\sin(k_n y).\frac{\sinh(k_n x)}{\sinh(k_n L)}.\frac{2}{b}\int_0^b \phi(L,y')\sin(k_n, y')dy'$$

Where $\psi_0(x,y)$ is the potential distribution in the same homogeneous system with the same dielectric constant and $V'_{GS} = V_{GS} - V_{FB}$

Nomenclature

- VBI : Built in potential between the source and the substrate when the substrate bias is zero
- Tox : The gate oxide thickness.
- Rj: The source-drain junction depth.
- Na: The substrate doping concentration.
- Ydo: The minimum depletion depth.
- Rss/RDS: The radius of the depletion edge of the cylindrical source-drain junction.
- L/b: The length/width of the specified rectangular coordinate system.
- VFB :The flat-band voltage of the MOSFET.
- L* :The effective length in which the diffusion
- Dn :The diffusivity of electrons.
- W :The effective width of a MOSFET.
- ψ^* : The minimum surface potential.
- φ :The potential othn e boundaries.
- ψ : The two-dimensional potential distribution.

3.5.Poisson's Equation Applied to Dual Material MOSFET

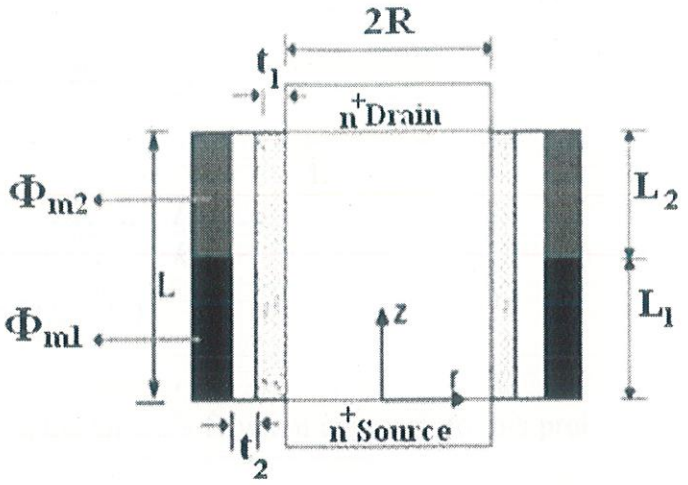


Figure 7: Schematic for Dual Material MOSFET Analysis

The potential distribution in the silicon substrate of our double material MOSFET is given in the form of the following differential equation

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\phi(r,z)}{\partial r}\right)+\frac{\partial^2\phi(r,z)}{\partial z^2}=\frac{qN_A}{\varepsilon_{si}}$$

Where, N_A is silicon film doping concentration and $\phi(r,z)$ is the electrostatic potential

The given boundary conditions for this problem are

$$\frac{\partial^2\phi_{s1}(z)}{\partial z^2}-k^2\phi_{s1}(z)=\beta_1,$$

For $0\le z\le L_1$

And $\frac{\partial^2\phi_{s2}(z)}{\partial z^2}-k^2\phi_{s2}(z)=\beta_2,$

For $L_1\le z\le(L_1+L_2)$

Where, ϕ_{s1} and ϕ_{s2} are the surface potential under the gate near the source end and under the gate near the drain end respectively.

Where, $\beta=\frac{qN_A}{\varepsilon_{si}}-k^2(V_{gs}-V_{FB})$ and $k^2=\frac{2C_{ox}}{\varepsilon_{si}R}$

With $C_{ox} = \dfrac{\varepsilon_{ox}}{\left[R \ln\left(1+\dfrac{t_{ox}}{R}\right)\right]}$

The solution of the equation of the given type is of the form

$$\phi_{s1}(z) = Ae^{kz} + Be^{-kz} - \frac{\beta_1}{k^2} \quad *$$

For $0 \le z \le L_1$

$$\phi_{s2}(z) = Ce^{kz} + De^{-kz} - \frac{\beta_2}{k^2}$$

For $L_1 \le z \le (L_1 + L_2)$

On applying the Green's function approach to this problem, we get the following results,

$$A = \delta\left[2C_2 + C_3(\eta\eta_1^{-1} + \eta^{-1}\eta_1) - 2\eta^{-1}C_1\right]$$
$$B = \delta\left[2C_1\eta - 2C_2 - C_3(\eta\eta_1^{-1} + \eta^{-1}\eta_1)\right]$$
$$C = \delta\left[2C_2 - 2C_1\eta^{-1} + C_3(\eta^{-1}\eta_1^{-1} + \eta^{-1}\eta_1)\right]$$
$$D = \delta\left[2C_1\eta - 2C_2 - C_3(\eta\eta_1 + \eta\eta_1^{-1})\right]$$

Where,

$$\eta = e^{(k(L_1+L_2))}$$
$$\eta_1 = e^{(k(L_1))}$$
$$\delta = \left[2(\eta - \eta^{-1})\right]^{-1}$$
$$C_1 = \frac{\beta_1}{k^2}$$
$$C_2 = \left(\frac{\beta_2}{k^2}\right) + V_{bi} + V_{ds}$$
$$C_3 = \frac{(\beta_1 - \beta_2)}{k^2}$$

The electric field in the high metal workfunction and low metal workfunction region can be obtained by differentiating $\phi_{s1}(z)$ and $\phi_{s2}(z)$ respectively

Minimum Surface Potential

The position of minimum surface potential, Z_{min} is obtained by differentiating * with respect to z and then equating the result to zero, as

$$Z_{min} = \frac{1}{2k} \ln\left[\frac{B}{A}\right]$$

Minimum surface potential $\phi_{s\,min}$ is then obtained from * as ,

$$\phi_{s\,min} = 2\sqrt{AB} - \frac{\beta_1}{k^2}$$

Sub-threshold Slope

Sub-threshold slope, S is defined as $S = \frac{KT}{q} \log_{10}\left[\frac{1}{\frac{\partial(\phi_{s\,min}(Z_{min})}{\partial V_{gs}}}\right]$

Substituting the value of $\phi_{s\,min}$, S can be obtained as

$$S = \frac{KT}{q} \ln_{10}\left[\frac{1}{\frac{1}{\sqrt{AB}}\left\{B\left(\eta\left[2\delta^{-1}-2\right]\right)+A\left(\eta\left[2-2\delta\right]\right)\right\}+1}\right]$$

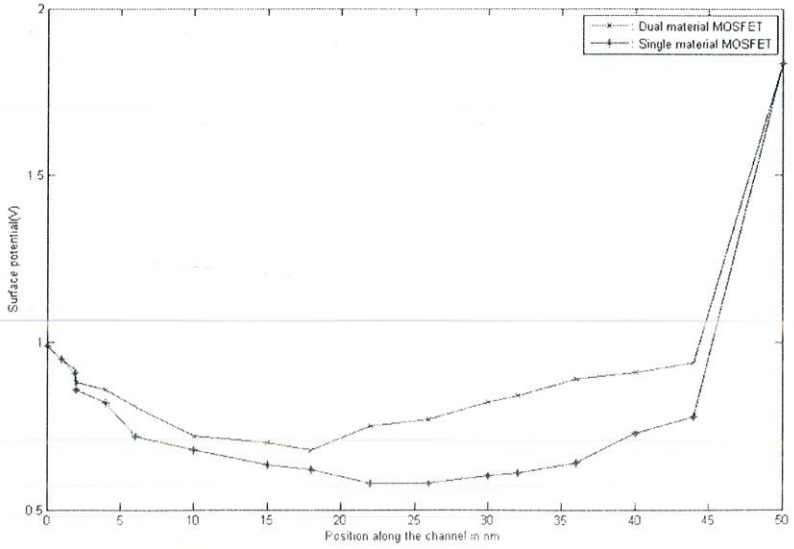


Figure 8: DIBL Lowering Graph

This graph shows the variation of surface potential along the channel for a dual material MOSFET and a normal single material MOSFET. It can be seen that Dual material MOSFET exhibits a step function in the surface potential along the channel as compared to the single material MOSFET. This step profile at the junction of the two gate metal electrodes screens the region near the source end from the variations in the drain voltage and the increase in drain voltage is dropped across the region. Hence, it leads to reduction in Drain Induced Barrier Lowering (DIBL).

Boundary conditions

$$\phi(x, 0) = V'_{GS}$$

$$\phi(x, b) = V_{BS}$$

$$\phi(0, y) = \begin{cases} V'_{GS} + \dfrac{V_{BI} - V'_{GS}}{T_{ox}} y, & \text{for } 0 \le y \le T_{ox} \\ V_{BI} + \dfrac{qN_A}{4\epsilon_{si}} (y - T_{ox})^2 - \dfrac{qN_A}{4\epsilon_{si}} R_{SS}^2 \ln\left[1 + \dfrac{(y - T_{ox})^2}{R_j^2}\right], \\ \quad \text{for } T_{ox} \le y \le T_{ox} + (R_{SS}^2 - R_j^2)^{1/2} \\ V_{BS}, \quad \text{for } T_{ox} + (R_{SS}^2 - R_j^2)^{1/2} \le y \le b \end{cases}$$

$$\phi(L, y) = \begin{cases} V'_{GS} + \dfrac{V_{BI} + V_{DS} - V'_{GS}}{T_{ox}} y, & \text{for } 0 \le y \le T_{ox} \\ V_{BI} + V_{DS} + \dfrac{qN_A}{4\epsilon_{si}} (y - T_{ox})^2 - \dfrac{qN_A}{4\epsilon_{si}} R_{DS}^2 \ln\left[1 + \dfrac{(y - T_{ox})^2}{R_j^2}\right], \\ \quad \text{for } T_{ox} \le y \le T_{ox} + (R_{DS}^2 - R_j^2)^{1/2} \\ V_{BS}, \quad \text{for } T_{ox} + (R_{DS}^2 - R_j^2)^{1/2} \le y \le b \end{cases}$$

CHAPTER 4: Device Fabrication

4. Device Fabrication

As shown in Figure 2, the basic process to realize such a device structure can be given as follows.

4.1.STI(Shallow Trench Isolation)

Shallow trench isolation (STI), also known as **Box Isolation Technique**, is an integrated circuit feature which prevents electrical current leakage between adjacent semiconductor device components. STI is generally used on CMOS process technology nodes of 250 nanometres and smaller. Older CMOS technologies and non-MOS technologies commonly use isolation based on LOCOS.

STI is created early during the semiconductor device fabrication process, before transistors are formed. The key steps of the STI process involve etching a pattern of trenches in the silicon, depositing one or more dielectric materials (such as silicon dioxide) to fill the trenches, and removing the excess dielectric using a technique such as chemical-mechanical planarization.

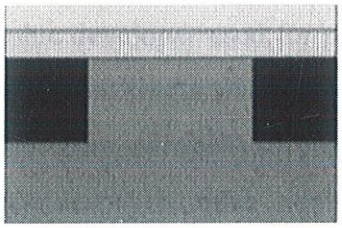
Certain semiconductor fabrication technologies also include deep trench isolation, a related feature often found in analog integrated circuits.

The effect of the trench edge has given rise to what has recently been termed the "reverse narrow channel effect" or "inverse narrow width effect". Basically, due to the electric field enhancement at the edge, it is easier to form a conducting channel (by inversion) at a lower voltage. The threshold voltage is effectively reduced for a narrower transistor width. The main concern for electronic devices is the resulting sub threshold leakage current, which is substantially larger after

the threshold voltage reduction.

4.2.Nitride deposition (Protective Nitride + Oxide Film)

Chemical vapour deposition (CVD) is a chemical process used to produce high-purity, high-performance solid materials. The process is often used in the semiconductor industry to produce thin films. In a typical CVD process, the wafer (substrate) is exposed to one or more volatile precursors, which react and/or decompose on the substrate surface to produce the desired deposit. Frequently, volatile by-products are also produced, which are removed by gas flow through the reaction chamber. Micro fabrication processes widely use CVD to deposit materials in various forms, including: mono-crystalline, polycrystalline, amorphous, and epitaxial. These materials include: silicon, carbon fibre, carbon nano-fibers, filaments, carbon nanotubes, SiO_2, silicon-germanium, tungsten, silicon carbide, silicon nitride, silicon oxynitride, titanium nitride, and various high-k dielectrics. The CVD process is also used to produce synthetic diamonds.



The nitride layer acts as a sacrificial layer which defines the silicon film thickness and oxide layer serves as a sacrificial gate. This process is followed by the process of deposition of thin oxide film. This process is also called as Stack Deposition.

4.3.Dry etch

Etching is used in micro fabrication to chemically remove layers from the surface of a wafer during manufacturing. Etching is a critically important process module, and every wafer undergoes many etching steps before it is complete. For many etch steps, part of the wafer is protected from the etchant by a "masking" material

which resists etching. In some cases, the masking material is a photoresist which has been patterned using photolithography. Other situations require a more durable mask, such as silicon nitride.

The two fundamental types of etchants

4.4. Liquid-phase ("wet")

The first etching processes used liquid-phase ("wet") etchants. The wafer can be immersed in a bath of etchant, which must be agitated to achieve good process control. For instance, buffered hydrofluoric acid (BHF) is used commonly to etch silicon dioxide over a silicon substrate.

Different specialised etchants can be used to characterise the surface etched. Wet etchants are usually isotropic, which leads to large bias when etching thick films. They also require the disposal of large amounts of toxic waste. For these reasons, they are seldom used in state-of-the-art processes.

However, the photographic developer used for photoresist resembles wet etching. As an alternative to immersion, single wafer machines use the Bernoulli principle to employ a gas (usually, pure nitrogen) to cushion and protect one side of the wafer while etchant is applied to the other side. It can be done to either the front side or back side.

The etch chemistry is dispensed on the top side when in the machine and the bottom side is not affected. This etch method is particularly effective just before "backend" processing (BEOL), where wafers are normally very much thinner after wafer back grinding, and very sensitive to thermal or mechanical stress.

Etching a thin layer of even a few micrometres will remove micro cracks produced during back grinding resulting in the wafer having dramatically increased strength and flexibility without breaking.

4.5.Plasma-phase ("dry")

Some wet etchants etch crystalline materials at very different rates depending upon which crystal face is exposed. In single-crystal materials (e.g. silicon

wafers), this effect can allow very high anisotropy. For instance, potassium hydroxide (KOH) displays an etch rate selectivity 400 times higher in <100> crystal directions than in <111> directions. EDP (an aqueous solution of ethylene diamine and pyrocatechol), displays a <100>/<111> selectivity of 17X, does not etch silicon dioxide as KOH does, and also displays high selectivity between lightly doped and heavily boron-doped (p-type) silicon. Use of these etchants on wafers that already contain CMOS integrated circuits requires protecting the circuitry. KOH may introduce mobile potassium ions into silicon dioxide, and EDP is highly corrosive and carcinogenic, so care is required in their use. Tetramethylammonium hydroxide (TMAH) presents a safer alternative than EDP, with a 37X selectivity between {100} and {111} planes in silicon.

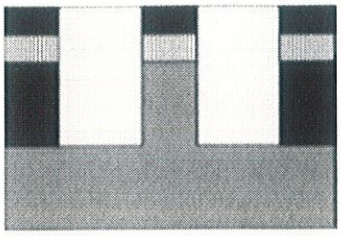
4.5.1 Plasma Etching

Modern VLSI processes avoid wet etching, and use plasma etching instead. Plasma etchers can operate in several modes by adjusting the parameters of the plasma. Ordinary plasma etching operates between 0.1 and 5 Torr. (This unit of pressure, commonly used in vacuum engineering, equals approximately 133.3 pascals.) The plasma produces energetic free radicals, neutrally charged, that react at the surface of the wafer. Since neutral particles attack the wafer from all angles, this process is isotropic.

Plasma etching can be isotropic, i.e., exhibiting a lateral undercut rate on a patterned surface approximately the same as its downward etch rate, or can be anisotropic, i.e., exhibiting a smaller lateral undercut rate than its downward etch rate. Such anisotropy is maximized in deep reactive ion etching. The use of the term anisotropy for plasma etching should not be conflated with the use of the same term when referring to orientation-dependent etching.

The source gas for the plasma usually contains small molecules rich in chlorine or fluorine. For instance, carbon tetrachloride (CCl_4) etches silicon and aluminium, and trifluoromethane etches silicon dioxide and silicon nitride. A plasma containing oxygen is used to oxidize ("ash") photoresist and facilitate its removal. Ion milling, or sputter etching, uses lower pressures, often as low as 10^{-4} Torr (10 mPa). It bombards the wafer with energetic ions of noble gases, often Ar^+, which

knock atoms from the substrate by transferring momentum. Because the etching is performed by ions, which approach the wafer approximately from one direction, this process is highly anisotropic. On the other hand, it tends to display poor selectivity. Reactive-ion etching (RIE) operates under conditions intermediate between sputter and plasma etching (between 10^{-3} and 10^{-1}Torr). Deep reactive-ion etching(DRIE) modifies the RIE technique to produce deep, narrow features.Anisotropic plasma etching of SiO2/Si3N4-Si is performed to define the future source/drain (S/D).



4.5Trench Fill With Oxide.

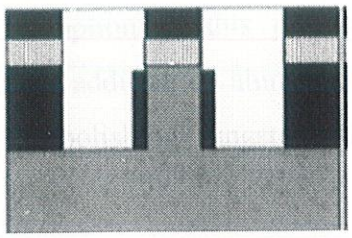
The exposure of silicon grows oxide which formsthe isolation near the S/D region.Under exposure to oxygen, a silicon surface oxidizes to form silicon dioxide (SiO2). Native silicon dioxide is a high-quality electrical insulator and can be used as a barrier material during impurity implants or diffusion, for electrical isolation of semiconductor devices, as a component in MOS transistors, or as an interlayer dielectric in multilevel metallization structures such as multichip modules. The ability to form a native oxide was one of the primary processing considerations which led to silicon becoming the dominant semiconductor material used in integrated circuits today.

Thermal oxidation of silicon is easily achieved by heating the substrate to temperatures typically in the range of 900-1200 degrees C. The atmosphere in the furnace where oxidation takes place can either contain pure oxygen or water

vapor. Both of these molecules diffuse easily through the growing SiO2 layer at these high temperatures. Oxygen arriving at the silicon surface can then combine with silicon to form silicon dioxide. The chemical reactions that take place are either for so-called "dry oxidation" or

$$Si + O_2 \rightarrow SiO_2$$

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$



for "wet oxidation". Due to the stoichiometric relationships in these reactions and the difference between the densities of Si and SiO2, about 46% of the silicon surface is "consumed" during oxidation

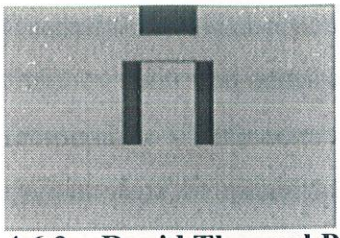
4.6Chemical Mechanical Polishing/Planarization

A process of smoothing surfaces with the combination of chemical and mechanical forces. It can be thought of as a hybrid of chemical etching and free abrasive polishing. The process uses abrasive and corrosive chemical slurry (commonly a colloid) in conjunction with a polishing pad and retaining ring, typically of a greater diameter than the wafer. The pad and wafer are pressed together by a dynamic polishing head and held in place by a plastic retaining ring. The dynamic polishing head is rotated with different axes of rotation (i.e., not concentric). This removes material and tends to even out any irregular topography, making the wafer flat or planar. This may be necessary in order to set up the wafer for the formation of additional circuit elements. For example, this might be necessary in order to bring the entire surface within the depth of field of a photolithography system, or to selectively remove material based on its position. Typical depth-of-field requirements are down to Angstrom levels for the latest 22 nm technology.

Before about 1990 CMP was looked on as too "dirty" to be included in high-precision fabrication processes, since abrasion tends to create particles and the abrasives themselves are not without impurities. Since that time, the integrated circuit industry has moved from aluminium to copper conductors. This required the development of an additive patterning process, which relies on the unique abilities of CMP to remove material in a planar and uniform fashion and to stop repeatably at the interface between copper and oxide insulating layers (see Copper-based chips for details). Adoption of this process has made CMP processing much more widespread. In addition to aluminum and copper, CMP processes have been developed for polishing tungsten, silicon dioxide, and (recently) carbon nanotubes.

4.6.1 How CMP Used In Shallow Trench Isolation

Shallow trench isolation (STI), a process used to fabricate semiconductor devices, is a technique used to enhance the isolation between devices and active areas. Moreover, STI has a higher degree of planarity making it essential in photolithographic applications, depth of focus budget by decreasing minimum line width. To planarize shallow trenches, a common method should be used such as the combination of resist etching-back (REB) and chemical mechanical polishing (CMP). This process comes in a sequence pattern as follows. First, the isolation trench pattern is transferred to the silicon wafer. Oxide is deposited on the wafer in the shape of trenches. A photo mask, composed of silicon nitride, is patterned on the top of this sacrificial oxide. A second layer is added to the wafer to create a planar surface. After that, the silicon is thermally oxidized, so the oxide grows in regions where there is no Si3N4 and the growth is between 0.5 and 1.0 μm thick. Since the oxidizing species such as water or oxygen are unable to diffuse through the mask, the nitride prevents the oxidation. Next, the etching process is used to etch the wafer and leave a small amount of oxide in the active areas. In the end, CMP is used to polish the SiO_2 overburden with an oxide on the active area. Chemical-mechanical polish (CMP) is carried out to the excess epi-silicon using the top oxide as a polish stop layer.



4.6.2 Rapid Thermal Processing

Rapid Thermal Processing (or **RTP**) refers to a semiconductor manufacturing process which heats silicon wafers to high temperatures (up to 1,200 °C or greater) on a timescale of several seconds or less. During cooling, however, wafer temperatures must be brought down slowly so they do not break due to thermal shock. Such rapid heating rates are often attained by high intensity lamps or lasers. These processes are used for a wide variety of applications in semiconductor manufacturing including dopant activation, thermal oxidation, metal reflow and chemical vapor deposition.

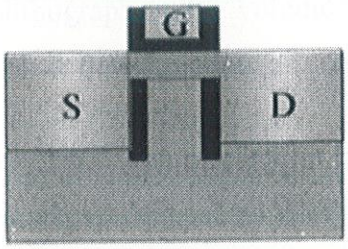
4.6.3 Rapid Thermal Annealing

Rapid thermal anneal (RTA) is a subset of Rapid Thermal Processing. It is a process used in semiconductor device fabrication which consists of heating a single wafer at a time in order to affect its electrical properties. Unique heat treatments are designed for different effects. Wafers can be heated in order to activate dopants, change film-to-film or film-to-wafer substrate interfaces, densify deposited films, change states of grown films, repair damage from ion implantation, move dopants or drive dopants from one film into another or from a film into the wafer substrate.

Rapid thermal anneals are performed by equipment that heats a single wafer at a time using either lamp based heating, a hot chuck, or a hot plate that a wafer is brought near. Unlike furnace anneals they are short in duration, processing each wafer in several minutes.

To achieve short time annealing time trade-off is made in temperature and process uniformity, temperature measurement and control and wafer stress as well as throughput.

Recently, RTP-like processing has found applications in another rapidly growing field — solar cell fabrication. RTP-like processing, in which an increase in the temperature of the semiconductor sample is produced by the absorption of the optical flux, is now used for a host of solar cell fabrication steps, including phosphorus diffusion for N/P junction formation and impurity gettering, hydrogen diffusion for impurity and defect passivation, and formation of screen-printed contacts using Ag-ink for the front and Al-ink for back contacts, respectively.



4.6.4 Gate Formation

The new DMG structure requires additional processing step or steps in order to laterally form two well-controlled contacting gate materials. To make a DMG-MOSFET using lithography facility, the method of tilt angle evaporation was used to deposit gate material 1, with a photoresist layer as the shadow. The relationship of the tilt angle the photoresist thickness and the gate length is $\tan\theta = lm_2 / d$

For the deposition of gate material 2, we used normal evaporation. As a reference for comparison, conventional SMG-MOSFET's with polysilicon gate were also fabricated, using the same materials and processes. The advantages of the DMG-MOSFET over the SMG-MOSFET are obvious. Etching And Applying Polysilicon Gate Is tougher and economically expensive then applying TAE in DMG MOSFET.

Apart from TAE method two different methods can also be used

4.6.5 E-Beam Writing

Electron beam lithography (often abbreviated as **e-beam lithography**) is the practice of emitting a beam of electrons in a patterned fashion across a surface covered with a film (called the resist),[1] ("exposing" the resist) and of selectively removing either exposed or non-exposed regions of the resist ("developing"). The

purpose, as with photolithography, is to create very small structures in the resist that can subsequently be transferred to the substrate material, often by etching. It was developed for manufacturing integrated circuits, and is also used for creating nanotechnology architectures.

The primary advantage of electron beam lithography is that it is one of the ways to beat the diffraction limit of light and make features in the nanometer regime. This form of maskless lithography has found wide usage in photomask-making used in photolithography, low-volume production of semiconductor components, and research & development.

The key limitation of electron beam lithography is throughput, i.e., the very long time it takes to expose an entire silicon wafer or glass substrate. A long exposure time leaves the user vulnerable to beam drift or instability that may occur during the exposure. Also, the turn-around time for reworking or re-design is lengthened unnecessarily if the pattern is not being changed the second time.

4.6.6 Lightly Doped Drain

Reduced doping of the drain region in very small geometry MOS/CMOS transistor; part of the drain engineering strategy in advanced MOSFET; designed to control drain-substrate breakdown; the reduced doping gradient between drain and channel lowers electric field in the channel in the vicinity of the drain; implementation: moderate implant before spacer formation, heavy implant after spacer formation.

4.6.7 Advantages of Using LDD

Light-doped region of drain below gate electrode

- parasitic capacitance is suppressed
- the intensity of electric field in drain is decreased
- Suppressed the probability of formation of hot electrons.
- Reduction in DIBL(Drain Induced Barrier Lowering).

Process Flow Of DMG-MOSFET

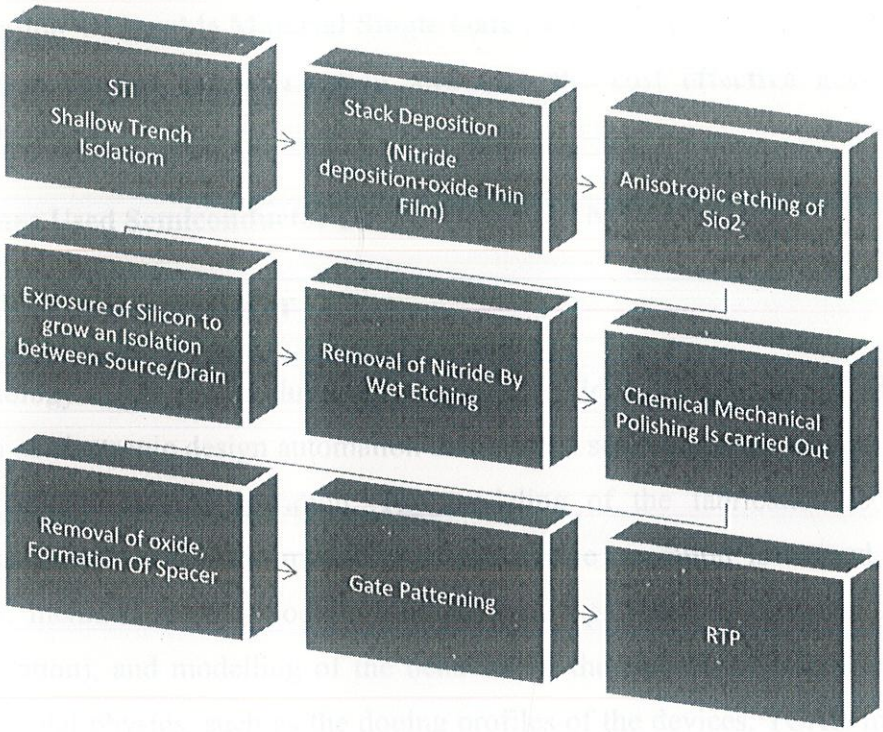


Figure 9: Dual Material Process Flow

CHAPTER 5: SIMULATION

Simulation Of Double Material Single Gate MOSFET (To check whether the design is correct for fabrication and also the cost effective ness of the MOSFET)

Software Used Semiconductor Device Modeling: NOVA TCAD

5.13D TCAD Simulator

Technology CAD (or **Technology Computer Aided Design**, or **TCAD)** is a branch of electronic design automation that models semiconductor fabrication and semiconductor device operation. The modeling of the fabrication is termed Process TCAD, while the modeling of the device operation is termed Device TCAD. Included are the modelling of process steps (such as diffusion and ion implantation), and modelling of the behavior of the electrical devices based on fundamental physics, such as the doping profiles of the devices. TCAD may also include the creation of compact models (such as the well-known SPICEtransistor models), which try to capture the electrical behavior of such devices but do not generally derive them from the underlying physics. (However, the SPICE simulator itself is usually considered as part of ECAD rather than TCAD.)

5.2 Introduction

Technology files and design rules are essential building blocks of the integrated circuit design process. Their accuracy and robustness over process technology, its variability and the operating conditions of the IC—environmental, parasitic interactions and testing, including adverse conditions such as electro-static discharge—are critical in determining performance, yield and reliability. Development of these technology and design rule files involves an iterative process that crosses boundaries of technology and device development, product design and quality assurance. Modeling and simulation play a critical role in support of many aspects of this evolution process.

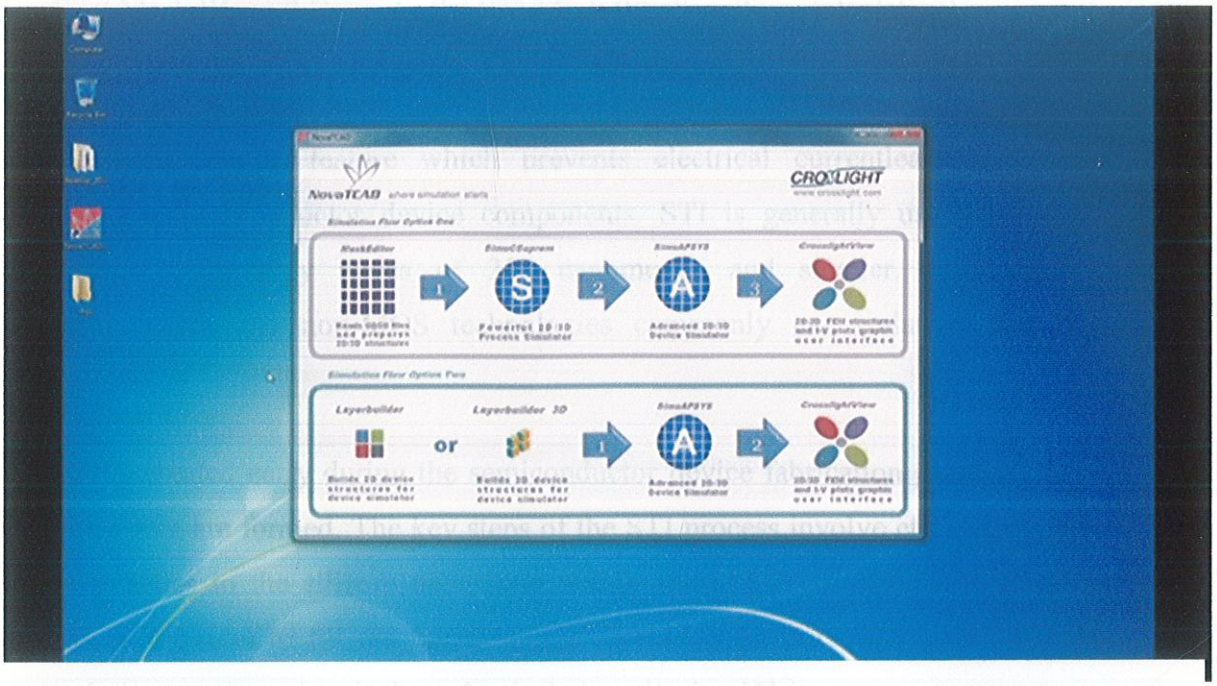
The goals of TCAD start from the physical description of integrated circuit devices, considering both the physical configuration and related device properties,

and build the links between the broad range of physics and electrical behavior models that support circuit design. Physics-based modeling of devices, in distributed and lumped forms, is an essential part of the IC process development. It seeks to quantify the underlying understanding of the technology and abstract that knowledge to the device design level, including extraction of the key parameters that support circuit design and statistical metrology. Although the emphasis here is on Metal Oxide Semiconductor (MOS) transistors—the workhorse of the IC industry—it is useful to briefly overview the development history of the modeling tools and methodology that has set the stage for the present state-of-the-art.

Current major suppliers of TCAD tools include Synopsys, Silvaco, Crosslight, CogendaSoftware|VisualTCAD and Global TCAD Solutions. The open source GSS,[11] Archimedes[12] Aeneas[13] and NanoTCADViDES has some of the capabilities of the commercial products. TCAD Central maintains an information resource for available TCAD software.

For the use of our Project we are using NOVA TCAD and 3D TCAD. These Simulators are industrial based simulators. These Simulators are not available for free on the internet. So the following Simulation was conducted at **FIBCOM Pvt. Ltd Gurgaon .Simulations Are Industrial Based So they were Run Under the Supervision Of Mr.Rajiv Dewan(Director FIBCOM Pvt. Ltd.**

5.3 Simulation



Mask Editor

Main Aim Of the Mask Editor is to import GTS files to be used in the Fabrication Industries to design Mask Layouts.

Step 1.

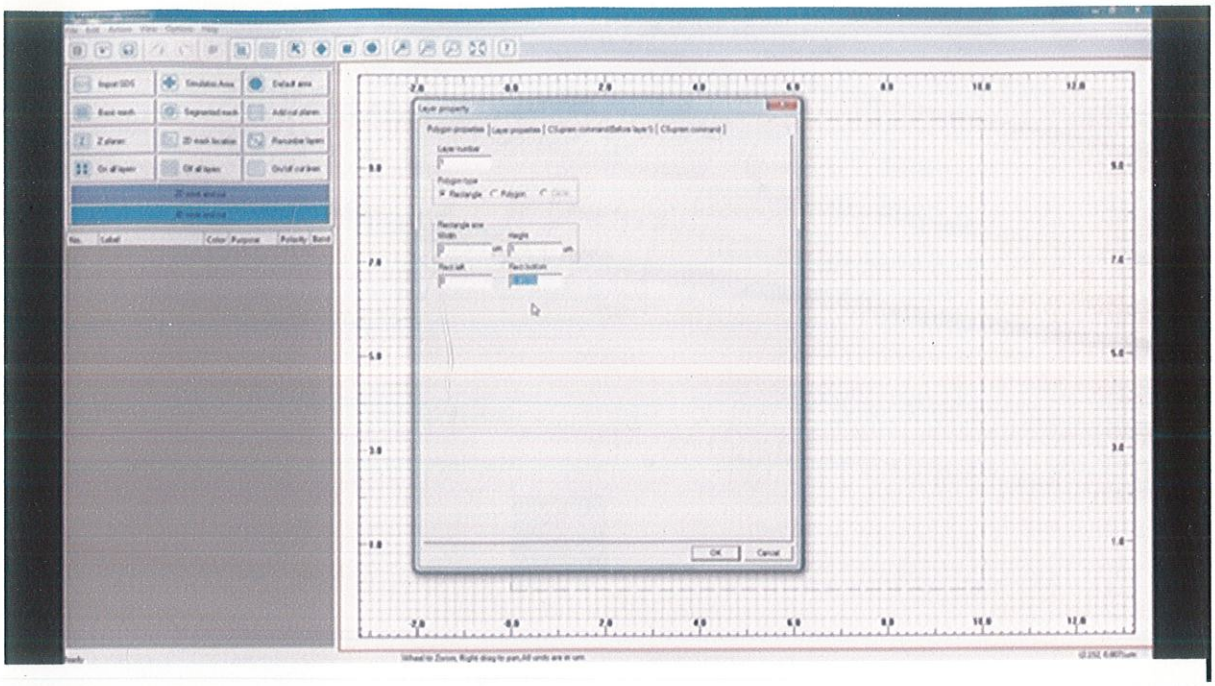
First Mask We will Draw As the STI Mask (Shallow Trench Isolation)

Shallow trench isolation (STI), also known as **Box Isolation Technique**, is an integrated circuit feature which prevents electrical currentleakage between adjacent semiconductor device components. STI is generally used on CMOS process technology nodes of 250 nanometers and smaller. Older CMOS technologies and non-MOS technologies commonly use isolation based on LOCOS.[1]

STI is created early during the semiconductor device fabrication process, before transistors are formed. The key steps of the STI process involve etching a pattern of trenches in the silicon, depositing one or more dielectric materials (such as silicon dioxide) to fill the trenches, and removing the excess dielectric using a technique such as chemical-mechanical planarization.[1]

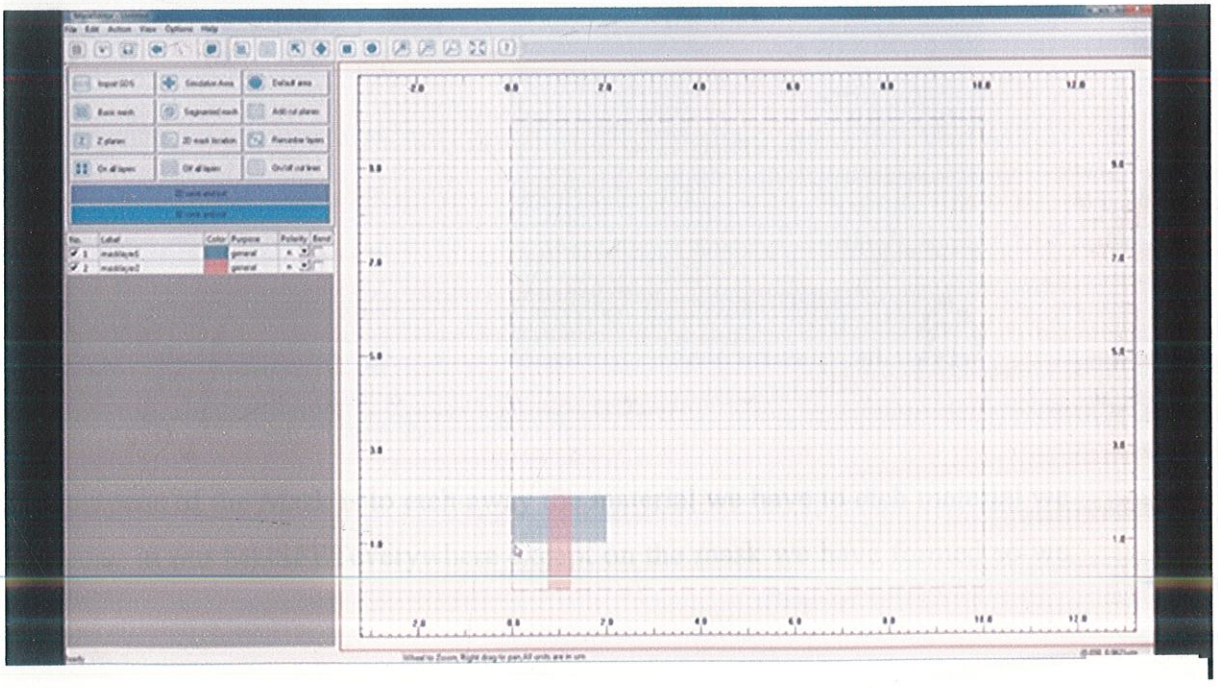
Certain semiconductor fabrication technologies also include deep trench isolation, a related feature often found in analog integrated circuits.

The effect of the trench edge has given rise to what has recently been termed the "reverse narrow channel effect"[2] or "inverse narrow width effect".[3] Basically, due to the electric field enhancement at the edge, it is easier to form a conducting channel (by inversion) at a lower voltage. The threshold voltage is effectively reduced for a narrower transistor width.[4][5] The main concern for electronic devices is the resulting subthreshold leakage current, which is substantially larger after the threshold voltage reduction.



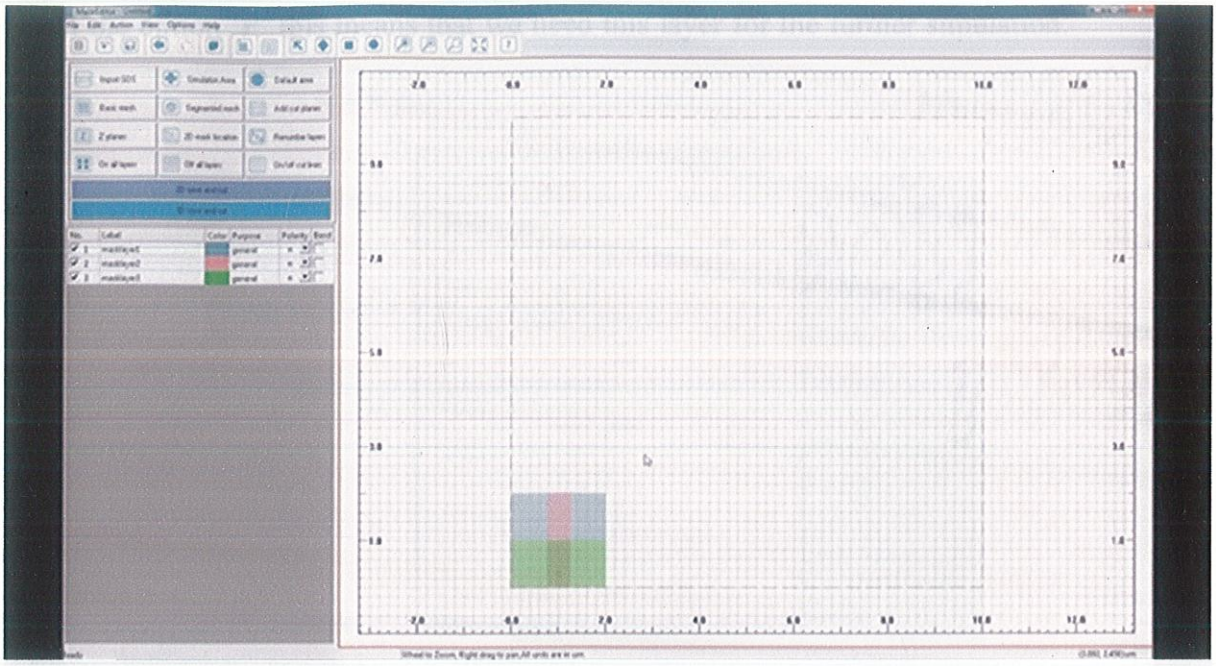
Step 2

Second Mask We Apply Is the Material Mask. In our case Material Mask is not a single Mask but we have a combination of two different materials with two different work functions. We will display the properties of material and work function further in mask properties.

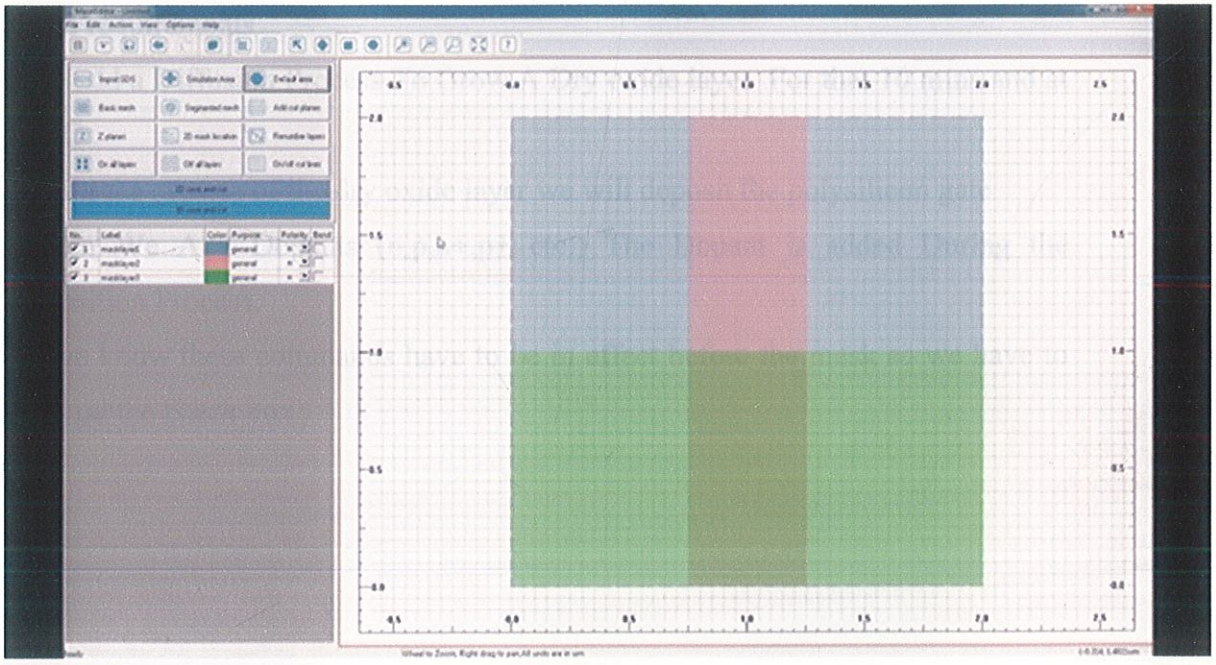


Step 3

Third Mask We Apply is The Source And Drain Implant.

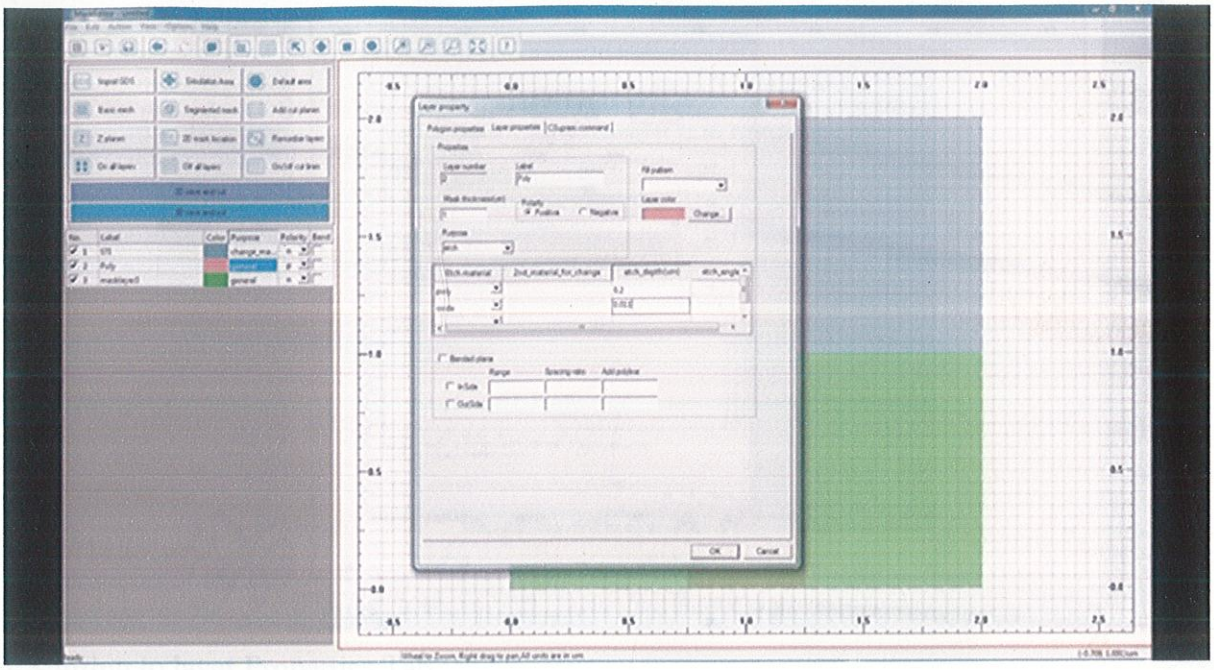


Simulation Area Zoomed IN for the Process Simulation



The purpose of the Mask is to etch away the material we have to etch material we are using in our MOSFETeverywhere except on the mask we have formed so we

select the option 'P' this means that we need this layer for the further simulation.



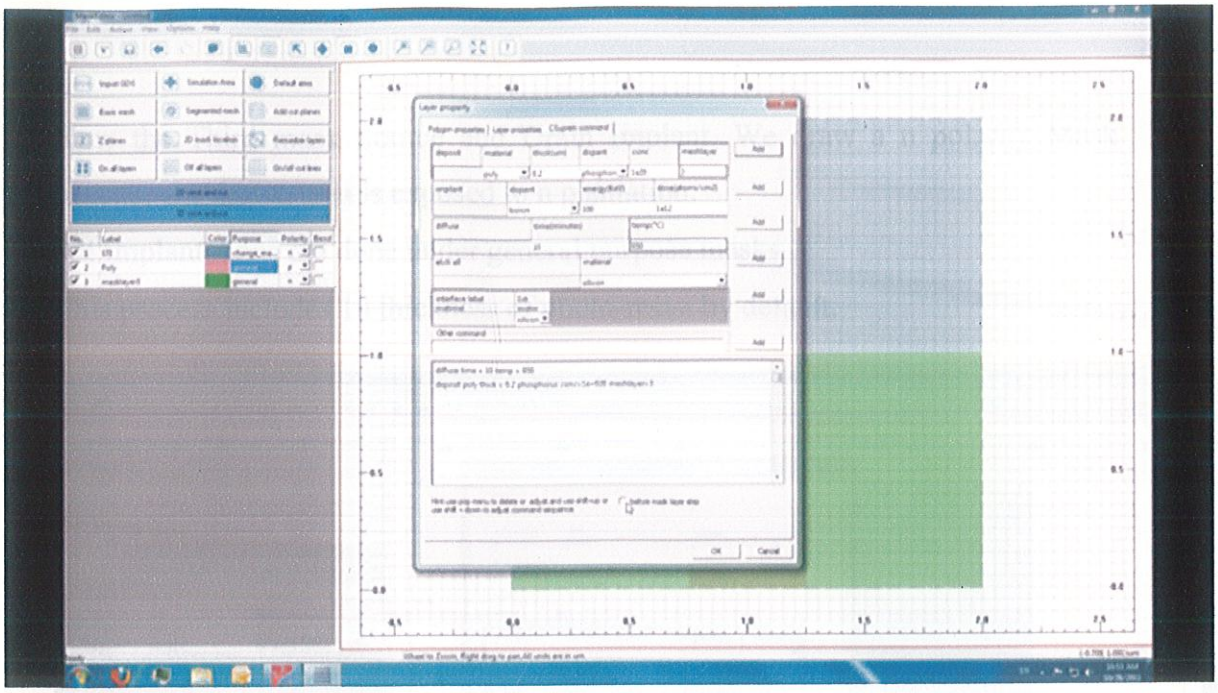
Some requirements

1.To add a Diffusion Process To Grow A Dry oxide layer. For that 10 mins and at 950 C .

2.Afetr the growth of the dry oxide layer we will deposit the polysilicon gate

3.Then We Add Dopants (n,p,n+,p+ etc.) The Dopant is added During the Deposition Process.

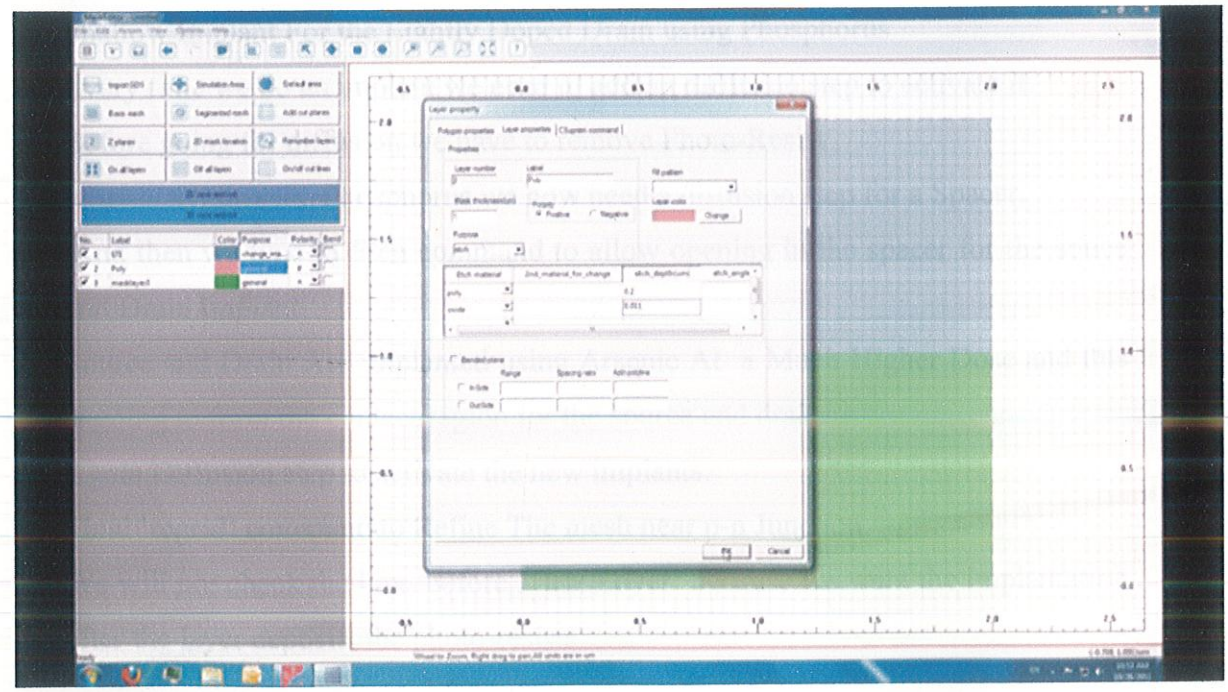
As we know these commands have to be in effect before the mask so we have to click on the check box .



Now Shifting to layer Properties Tab

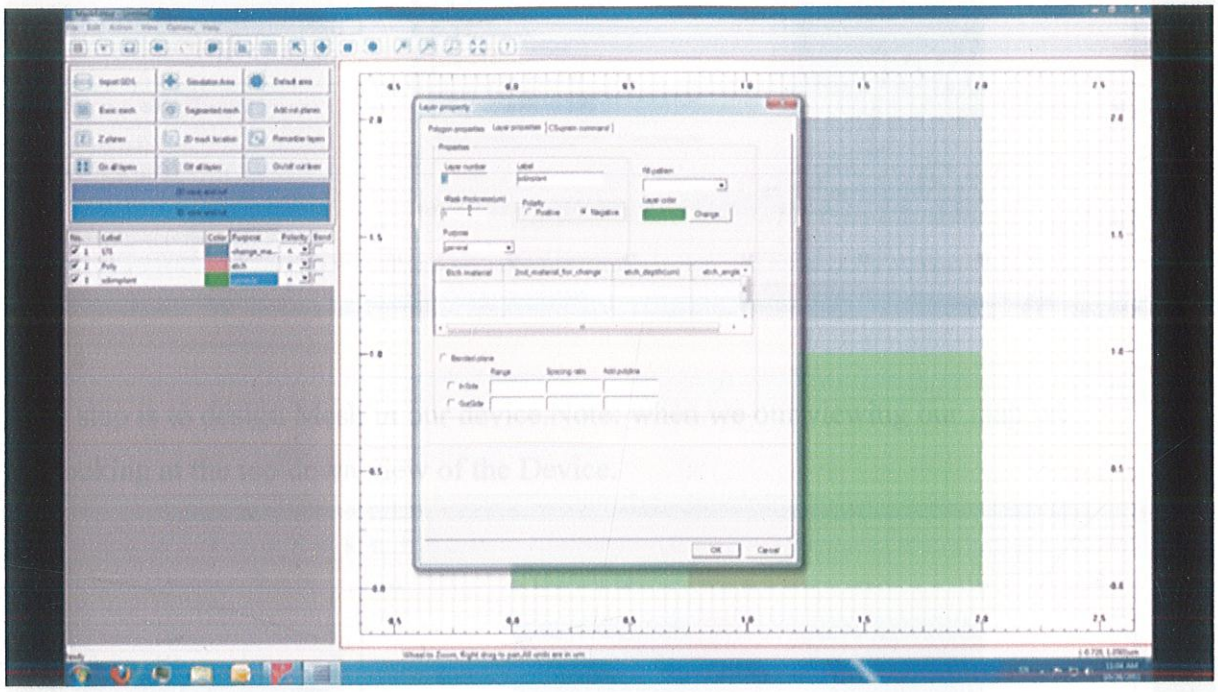
The purpose of the Mask is to etch away material so this process will take effect after the deposition.

- So we have to etch material everywhere except where we have drawn the mask.
- After this we need to do a an oxide etch we will do a over etch so that it is totally removed.



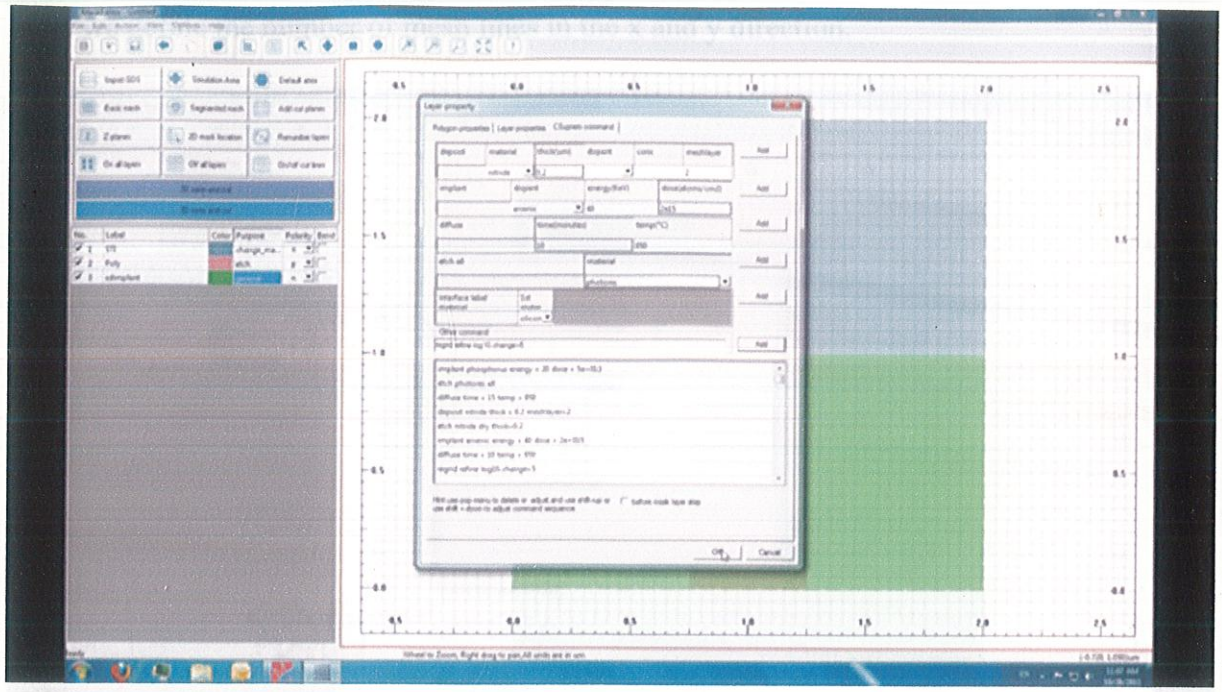
Now the Third mask Source and Drain Implant. We draw a n polarity Mask because the drawn area is exposed to n plantation.

- All Implantations are done under general purpose masks.
- This process includes 1u thickness of photo-resist by default.



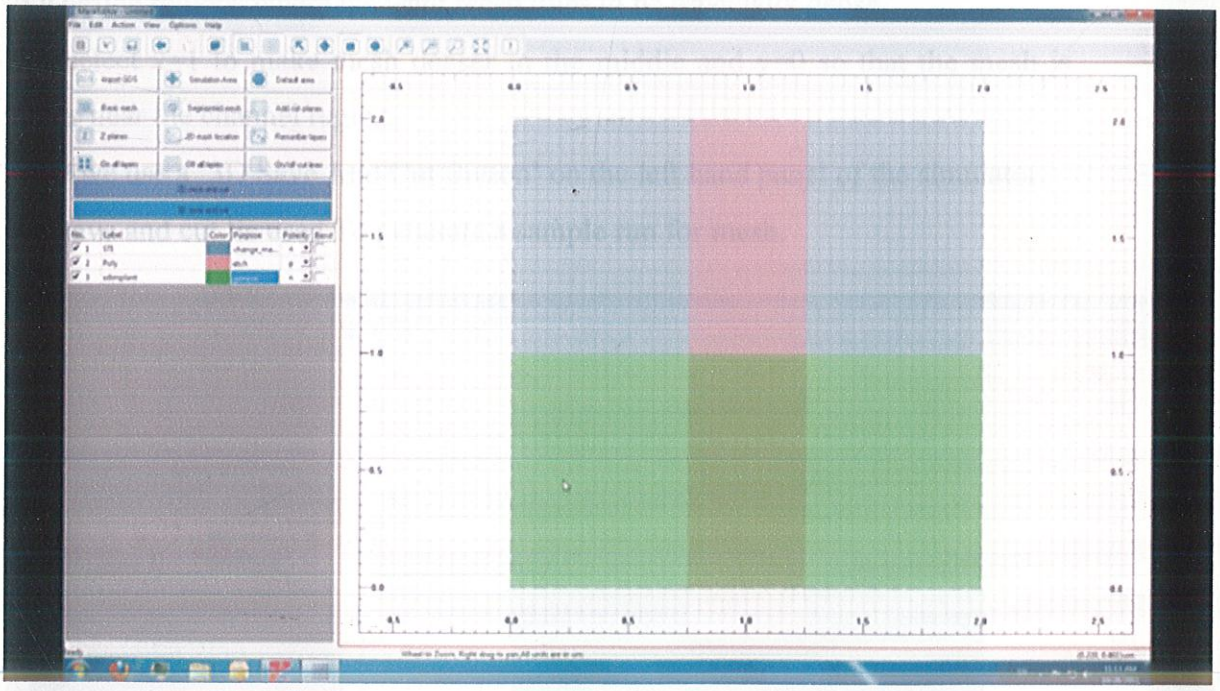
- Implantation is Done in Several Steps

1. Shallow Implant For the Lightly Doped Drain using Phosphorus
2. Every time we do an implant we need to add an diffusion step to activate it.
3. Before going for diffusion we have to remove Photo-Resist .
4. After activating the Phosphorus we now need a diffusion step for a Spacer.
5. And then we type in Etch command to allow opening in the spacer for the souce and Drain Implant.
6. Source and Drain Are implanted using Arsenic At a Much Higher Dose and this is going to form the contact region for the source and drain.
7. Again Diffusion step to activate the new implants.
8. Final 'regrid' command to Refine The mesh near p-n Junction.
9. We will not check the box 'before Mask Layer' because we want the implantation after the layer deposits the photo-resists



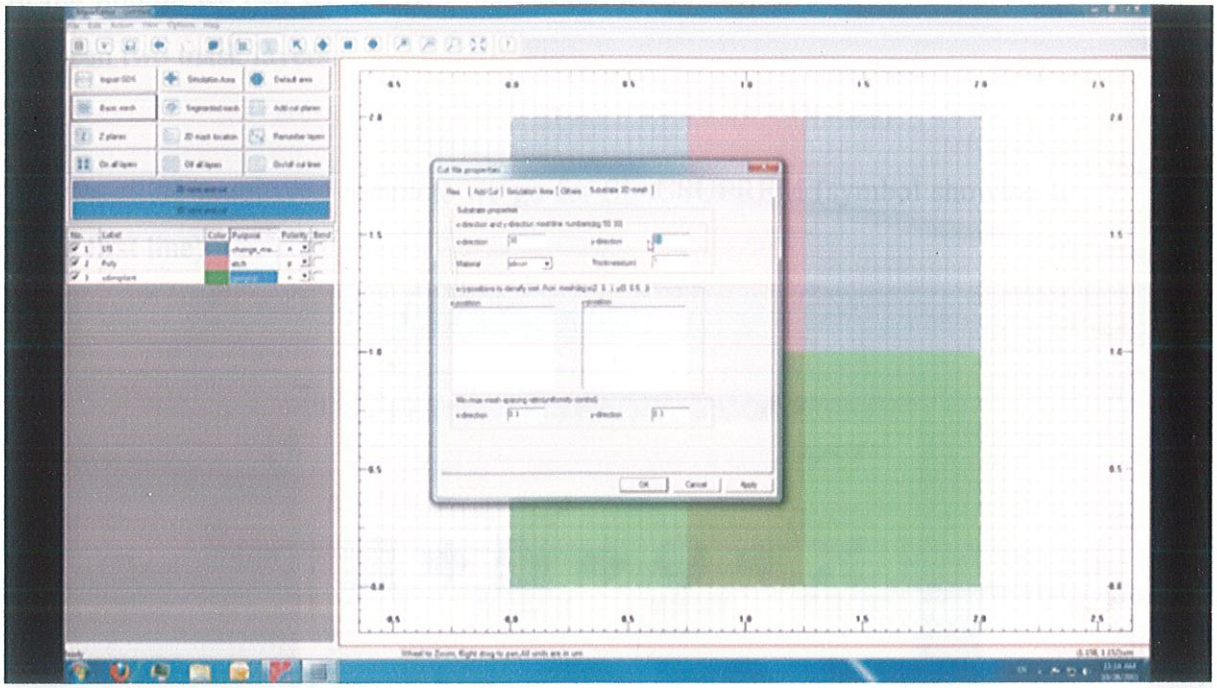
Step 4

Next step is to design Mesh in our device.Note: when we our viewing our map we are looking at the top down view of the Device.

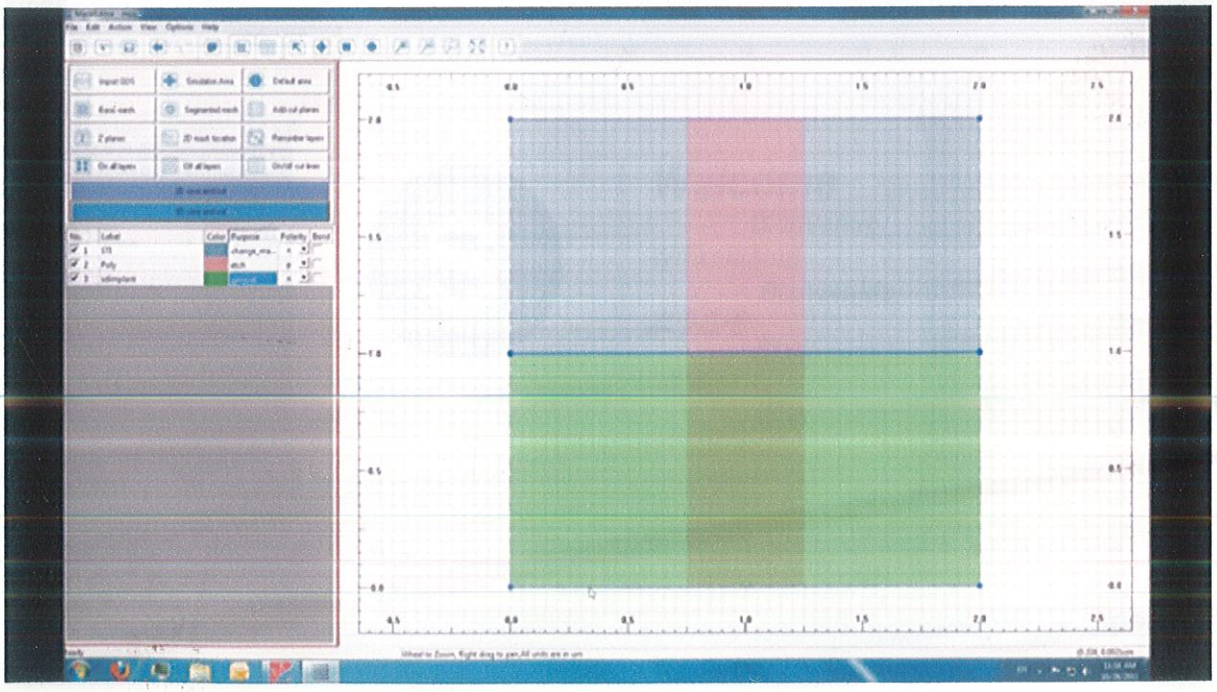


- The horizontal axis corresponds to the x-direction
- The Y direction is perpendicular to the device looking Down.
- The Z direction is in the vertical direction.
- Now we will use the basic mesh button on the top left corner of the screen.
- Now we will define initial x-y mesh in the substrate.

- Here we define the number of mesh lines in the x and y direction.



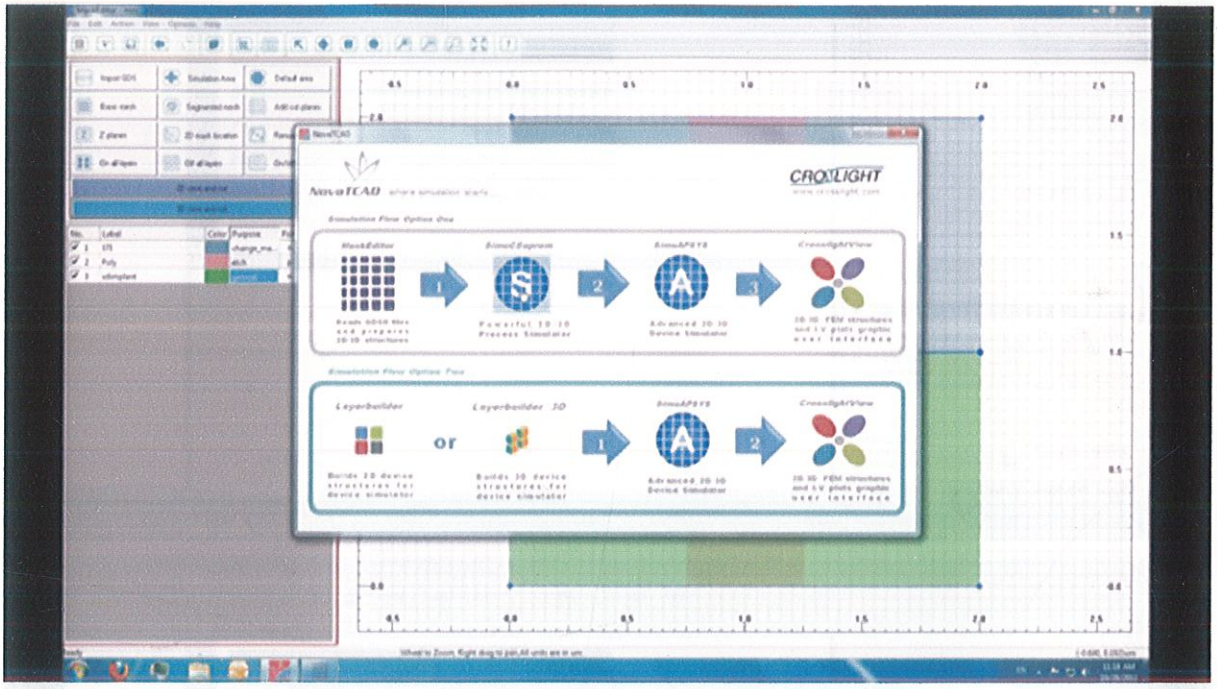
- We define the initial thickness of the substrate.
- We define regions where we want mesh lines to be especially dense.
- We select x=1 to make mesh denser in the middle and y=0 so that the mesh is dense near the channel region.
- Now we use a '3D Save And Cut Button' on the left hand panel of the simulator.
- '3d save and cut 'is used To generate a sample run for mesh.

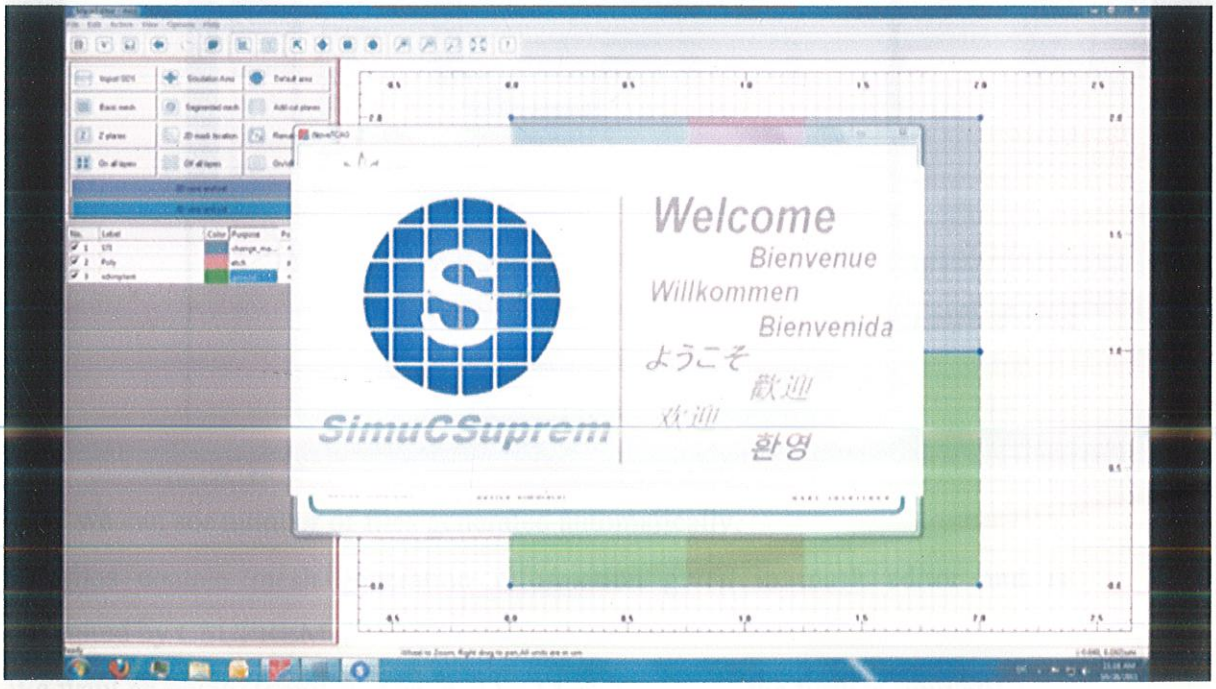


- Four mesh lines in the Z direction
- In the middle we can see the two lines very closely spaced as it is the interface between two mask layers.

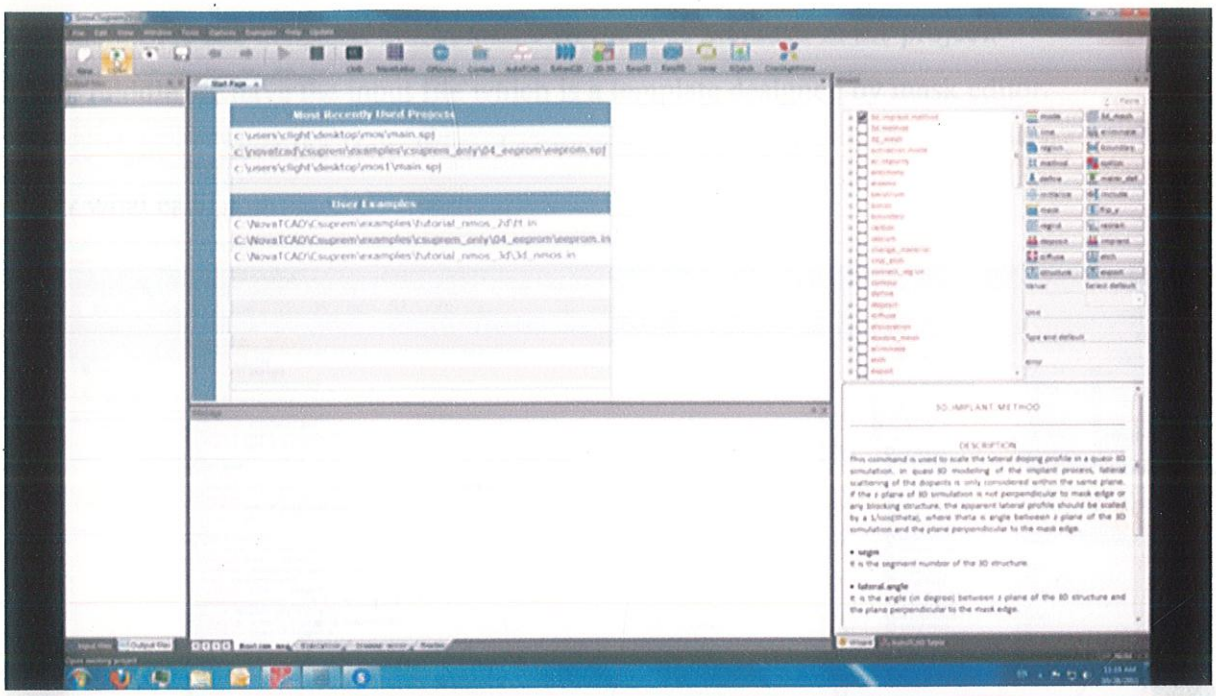
Step 5

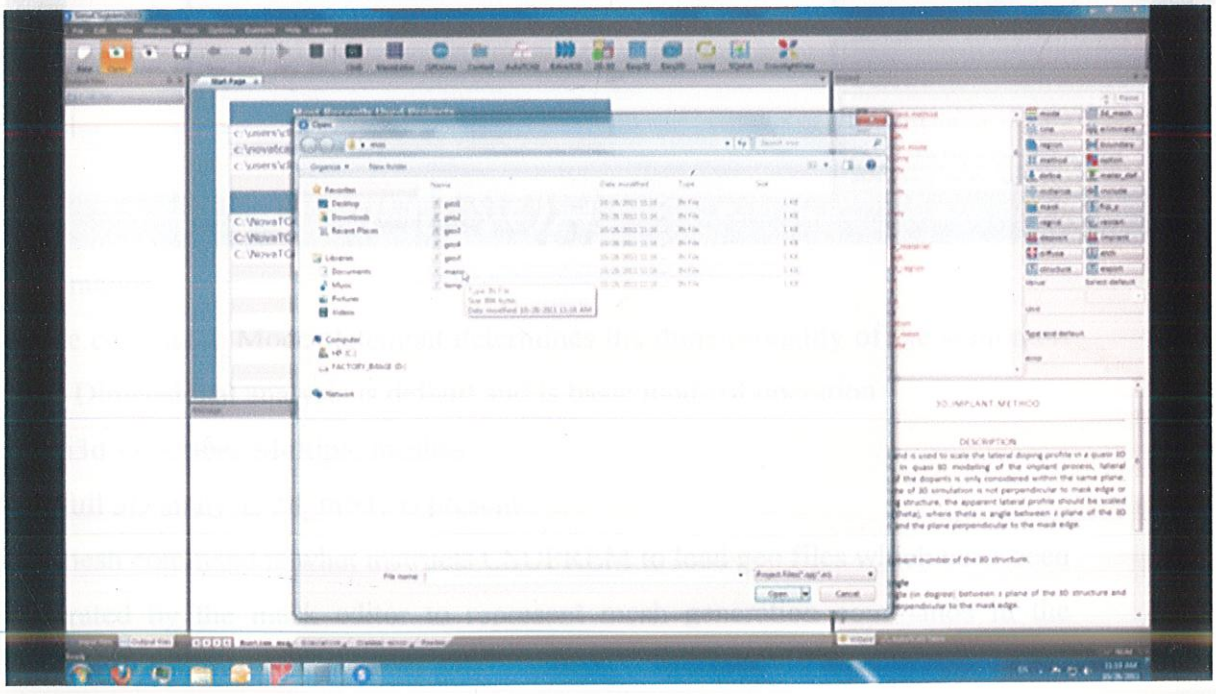
Now masking process is complete we go for SimCSUPREM (symbol showing S in the first line)





Now we open Our Directory





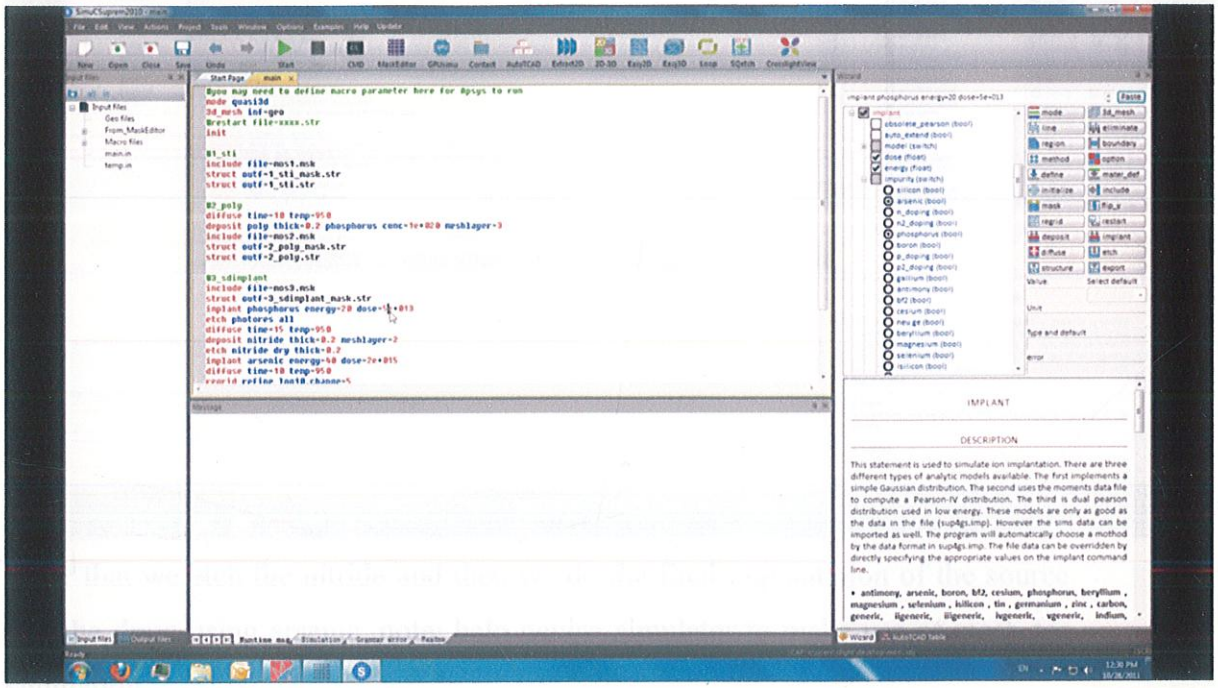
Here we can see number of files generated automatically.

- geo-files contain mesh generation information given in mask editor and is generated by CSUPREM.
- We want an empty template designed by Mask Editor for the further simulation.

Step 6

In the CSUPREM window we have various numbers of tabs

- Left hand Side has the panel that contains all the files included in the project.
- In the middle we have the input file which is a template designed by mask editor.
- On the right we have the Help Wizard as we scroll down the commands it lets us know what each command does.



Commands

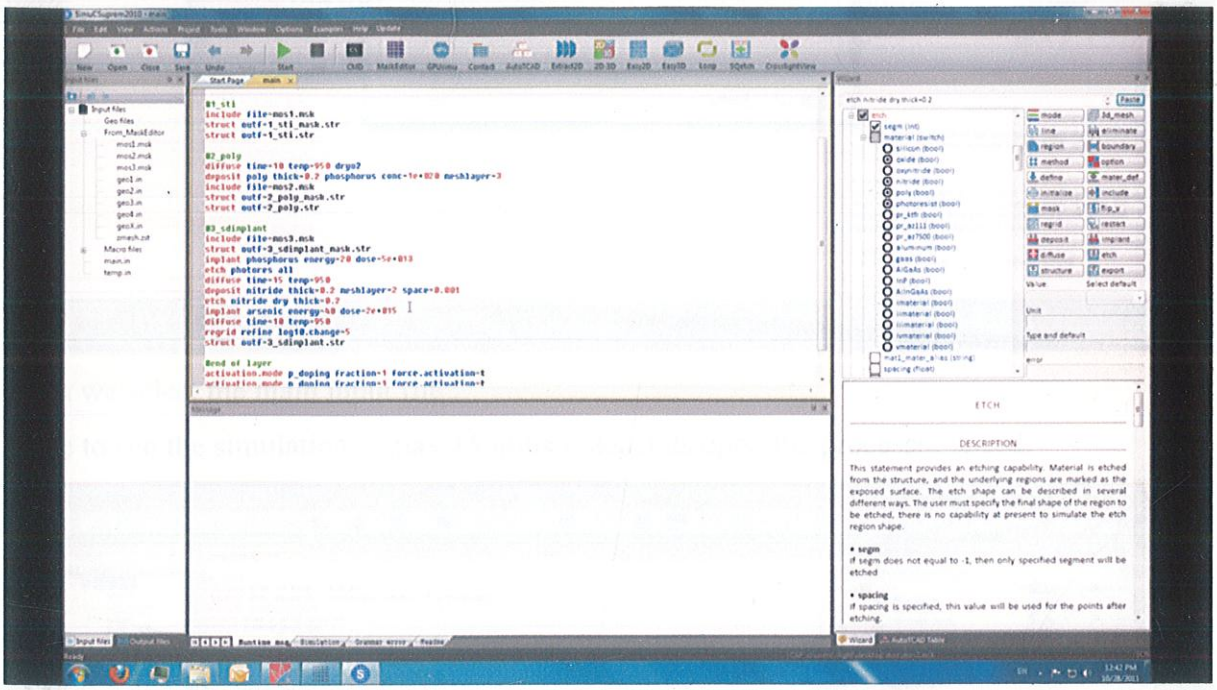
1. Mode command: Mode statement determines the dimensionality of the simulator. Two Dimensional analysis is default and is basic mode of operation.
2. quasi3d-Describes Multiple meshes.
3. For full 3D analysis 3d_mode is present .
4. 3d_mesh command is what instructs CSUPREM to load geo files which have been generated by the mask editor to represent mesh generation commands in the various layers.
5. Init command tells about initial state of the substrate

a. We have express the initial doping of the substrate p-type substrate with a boron concentration of 5e17

b. We have to specify orientation of the crystal i.e. 100 .

Since we have mesh inside the substrate since we are having extra layers on the top of the substrate we apply mesh layer command this dines new defines new horizontal mesh lines for the new layers. Note : dry02 is the command used for growing dry oxide layer .

Note: in order to generate a refined surface we make use of space parameters for making more number of mesh points. Command :space=0.001.

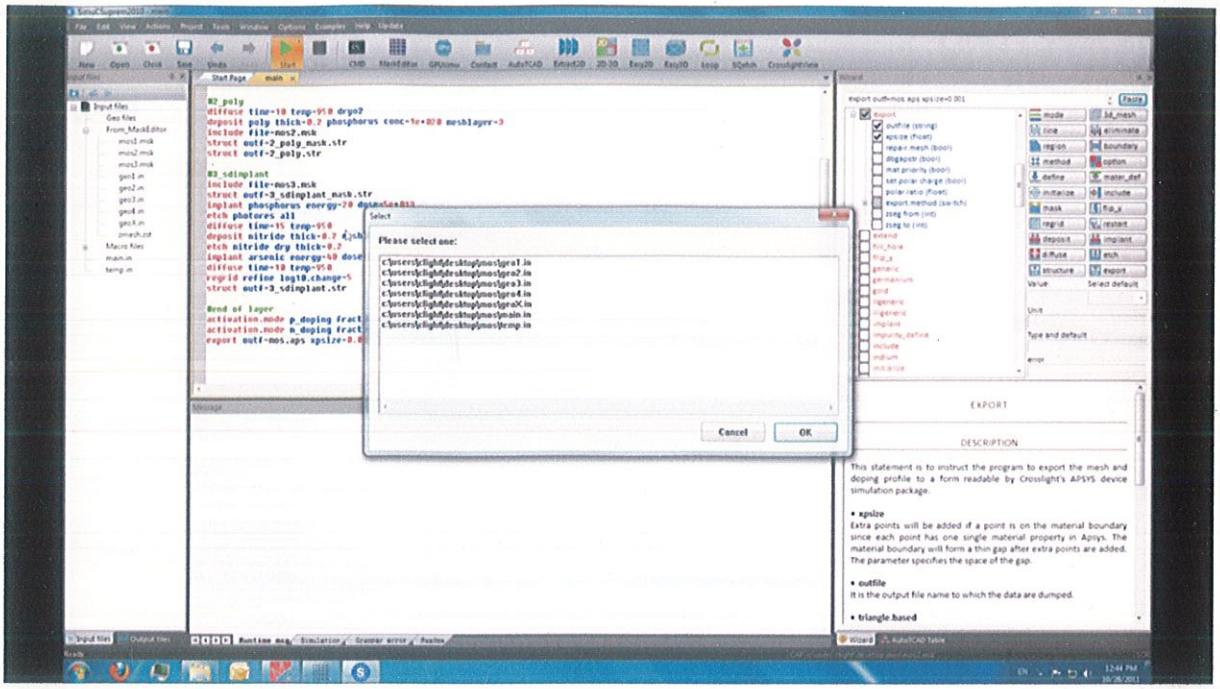


After that we etch the nitride and then we do the final implantation of the source and the drain using arsenic. note: help device simulator to make use of mesh for simulation.

For simulation

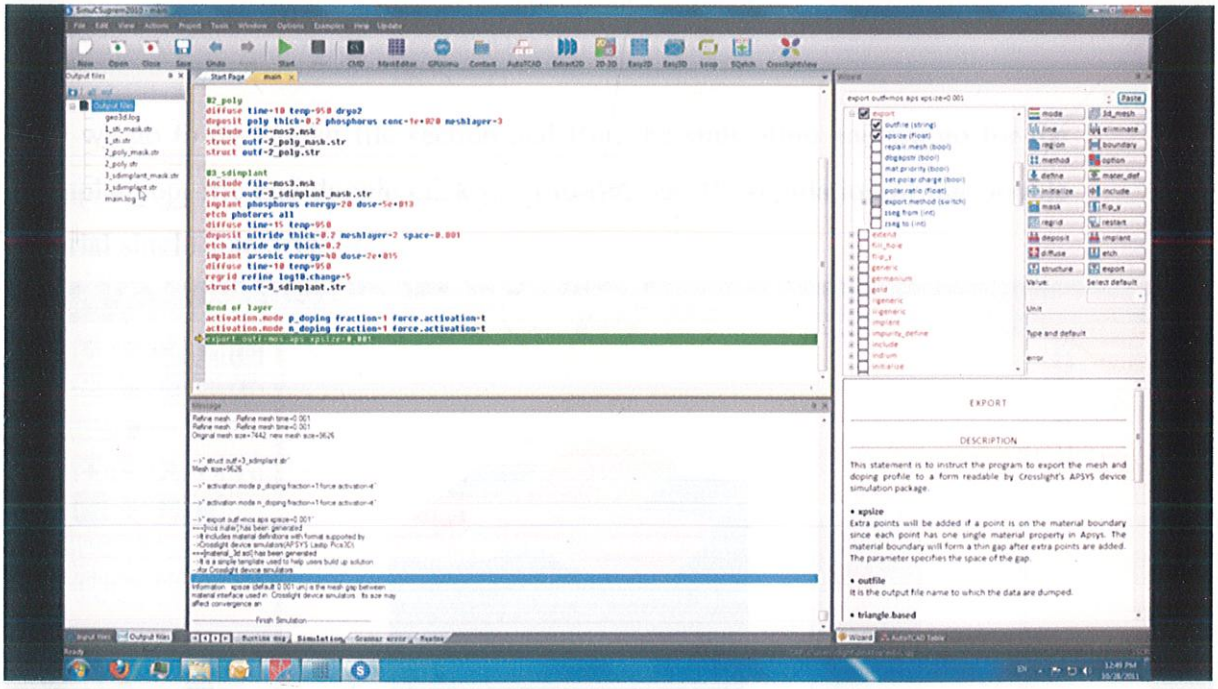
Step 7

Click on the start button on the tool bar below the title bar.

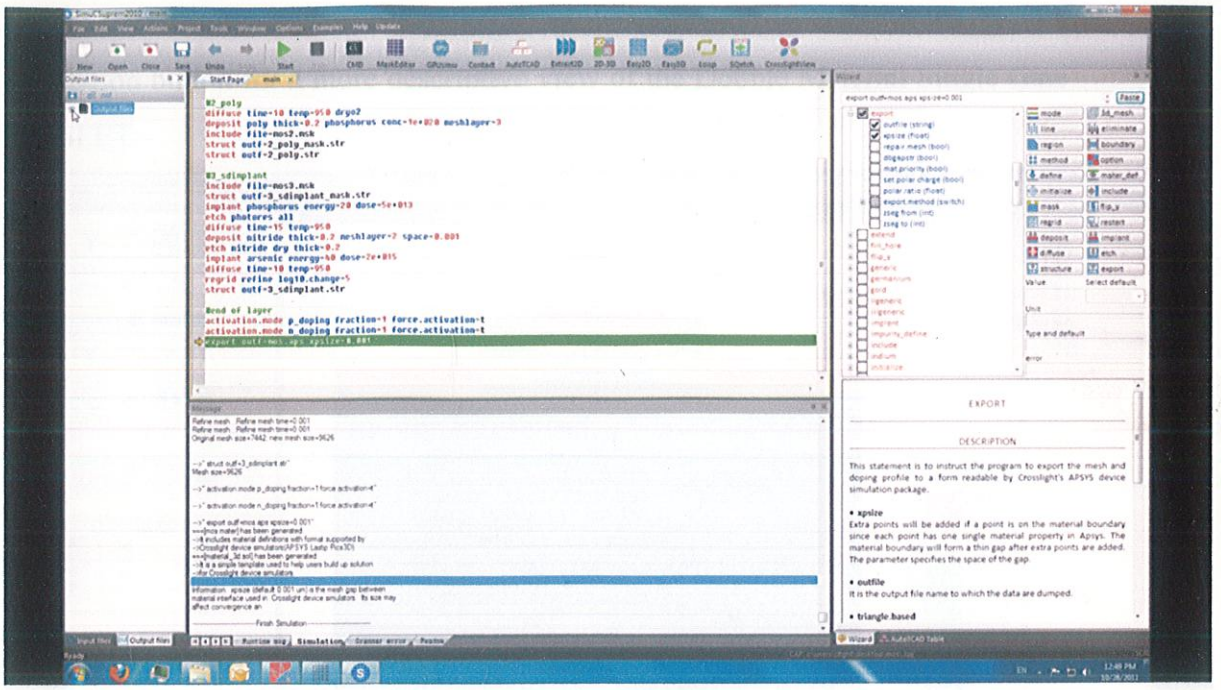


Then we select the main input file .

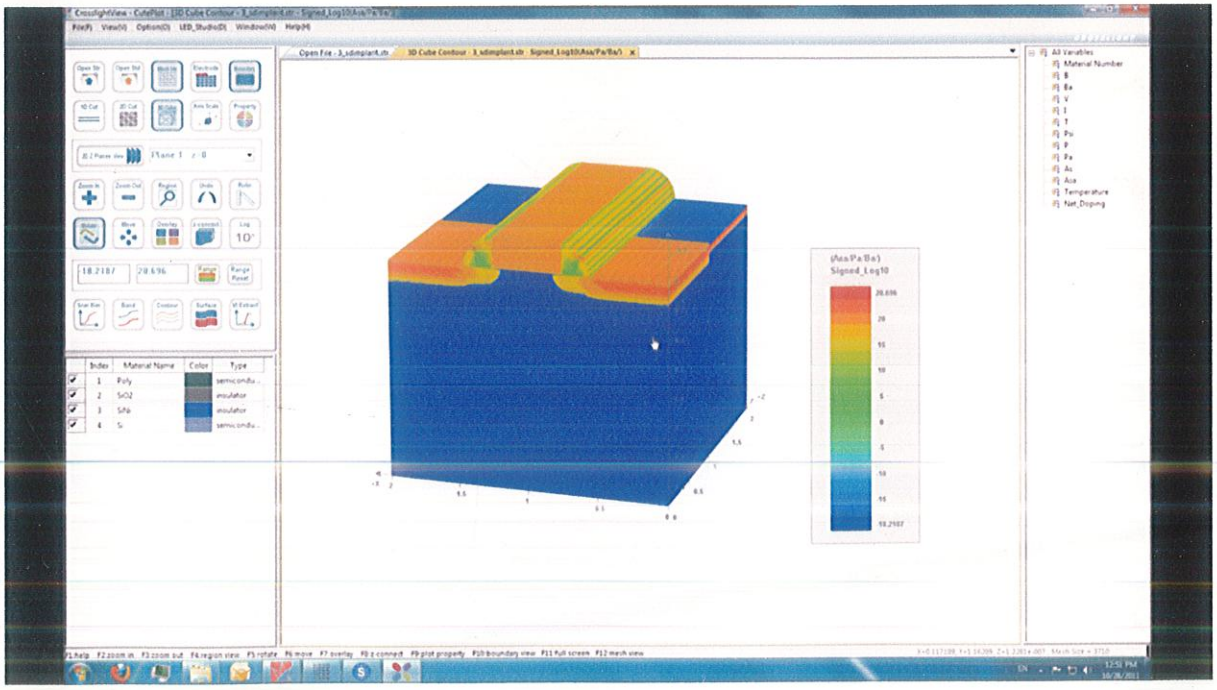
Time to run the simulation is max:15 mins it depends upon the processor speed.



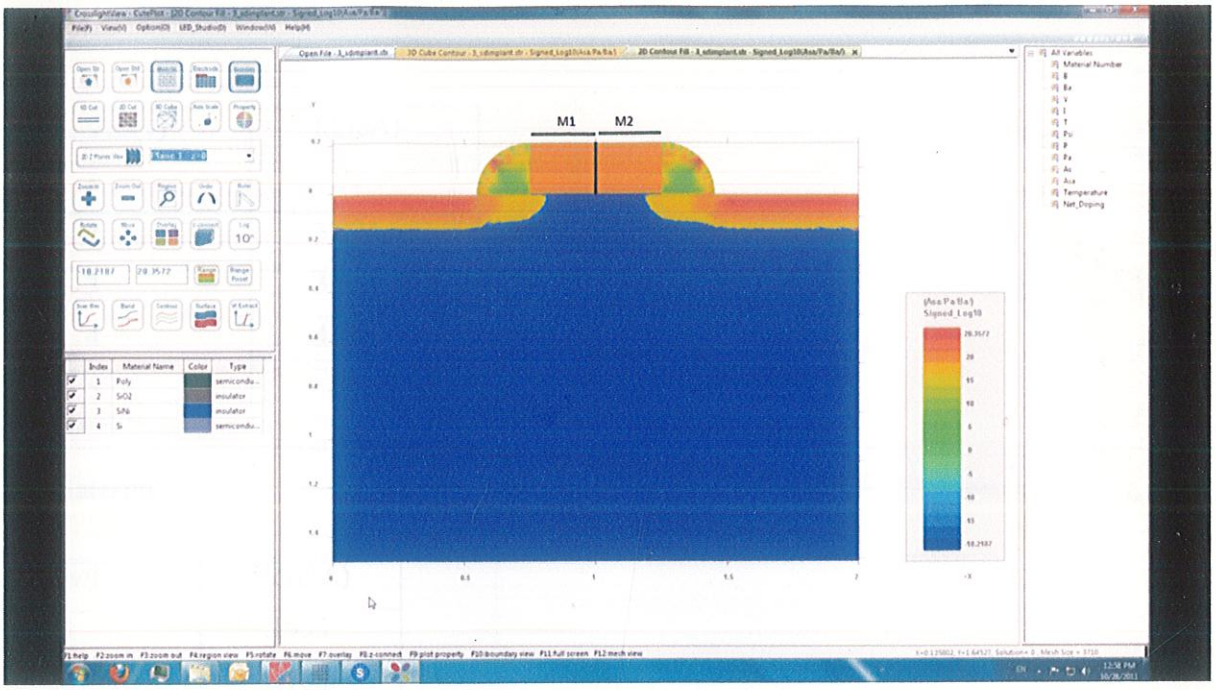
The blue line below shows that the the export command is initiated correctly and now it is saved in form of output file .Note: A message 'Simulation Complete' appears at the bottom of the window.



Now we go to the output file section and Run the simulation and we go for the sdiimplant.opt file and double click on it to run our 3D simulation of our double material single gate MOSFET.



Same as we can see buttons on the left of the window we can click on the 2D simulation button for a more descriptive view of the Double Material Single Gate MOSFET.



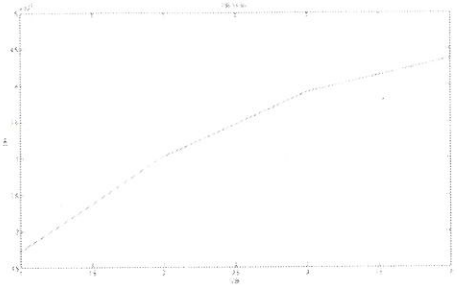
This shows that our DMSG MOSFET is simulated successfully in the simulator i.e. we have successfully done the dry fabrication of the DMSG MOSFET .

TCAD fabrication is just the one step before the original fabrication of the chip. Now we Can use our .cad file and use it to print in 3D

Chapter 6: Results

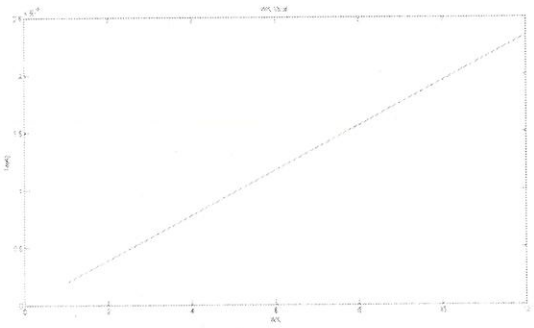
6.1 Results of Single Material MOSFET

Vds(v)	Id(mA)
1	1.72
2	3.024
3	3.906
4	4.368
5	



Single Material

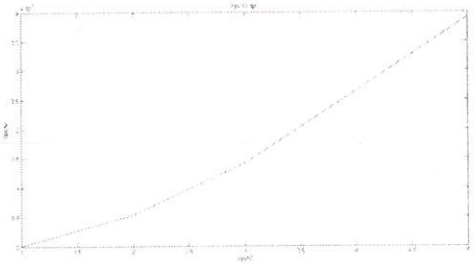
w/l	Id(mA)
1	.1953
3	.3906
4	.7812
8	1.562
12	2.343



Single material

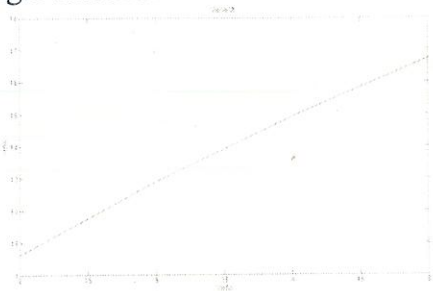
Vgs(v)	Id(mA)
1	.0075
2	.5370
3	1.419
4	2.646
5	3.906

Single material



Vsb(v)	Vt(v)
1	.782
2	1.0618
3	1.2917
4	1.492
5	1.6722

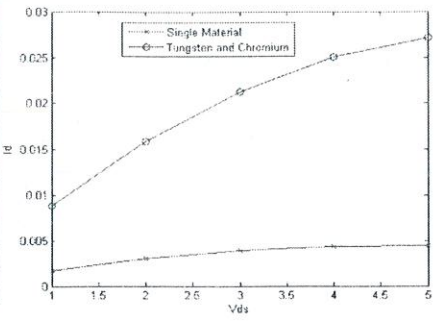
Single material



Results of Double Material MOSFETGate Material Engineering Properties Of Material

Vds(v)	Tungsten+Chromium(Id)
1	8.779
2	15.87
3	21.31
4	25.05
5	27.11

Double Material



Vds(v)	Tungsten+Gold(Id)
1	8.93
2	16.208
3	21.79
4	25.69
5	27.92

Double material

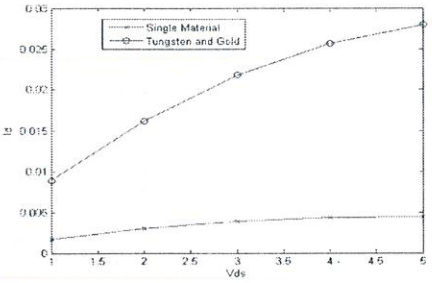
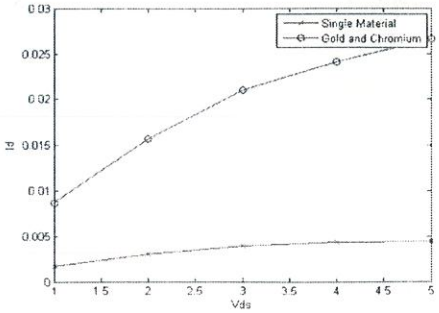


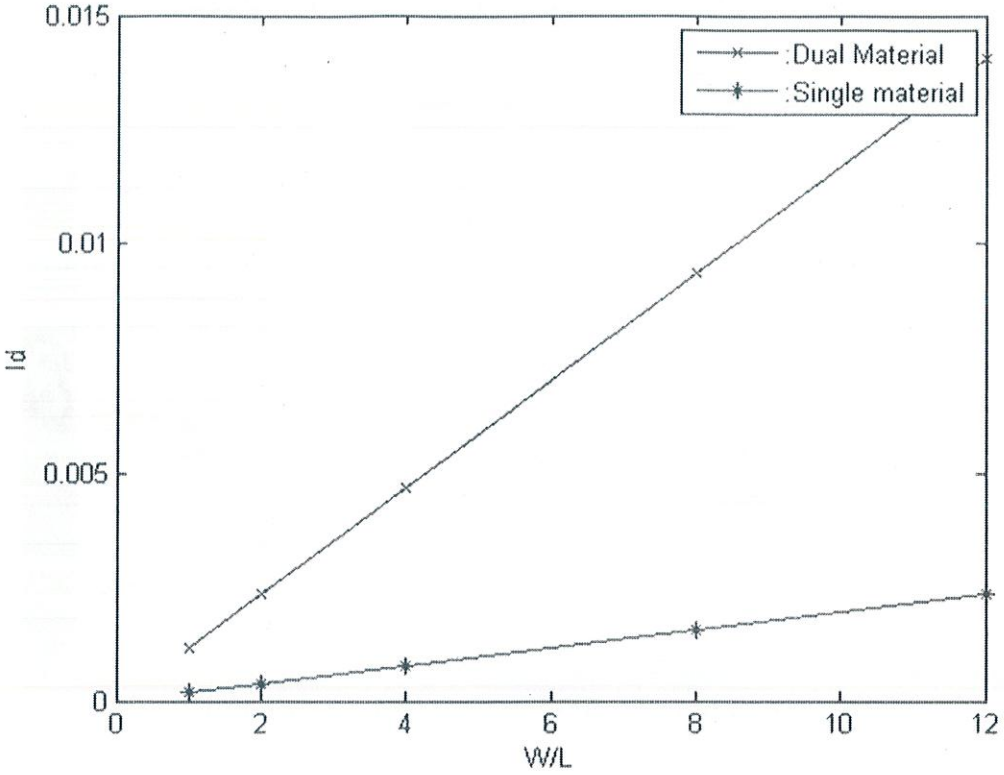
Figure 10:Numerical Simulation Of DMG MOSFET

Vds(v)	Gold+Chromium(Id)
1	8.68
2	15.69
3	21.04
4	24.08
5	26.65

Double material



Results of Double Material MOSFET Vs Single Material



Results of Double Material MOSFET Through Simulation In NOVA TCAD

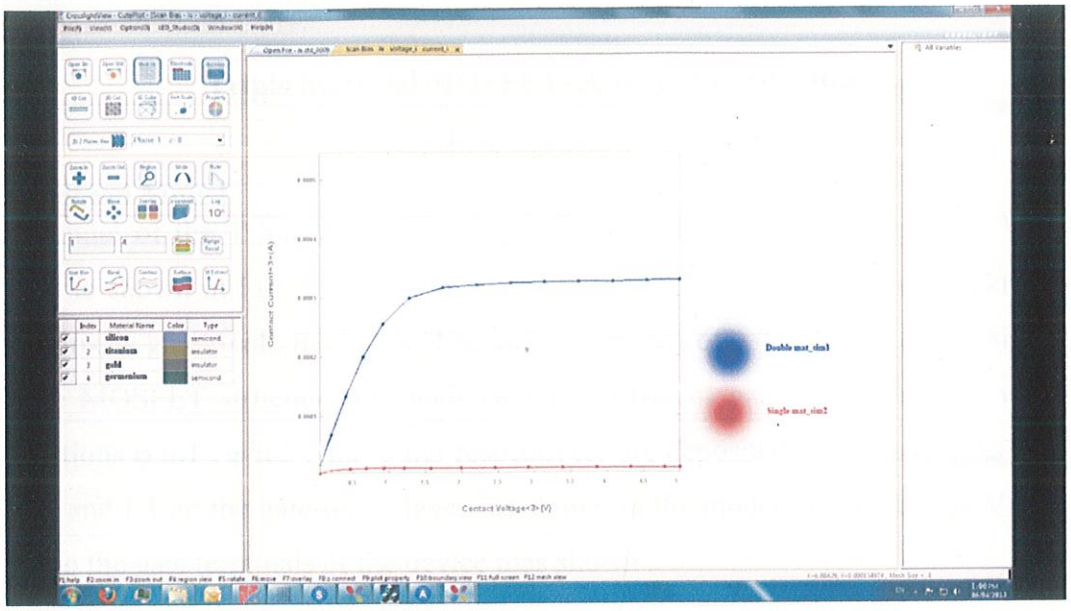
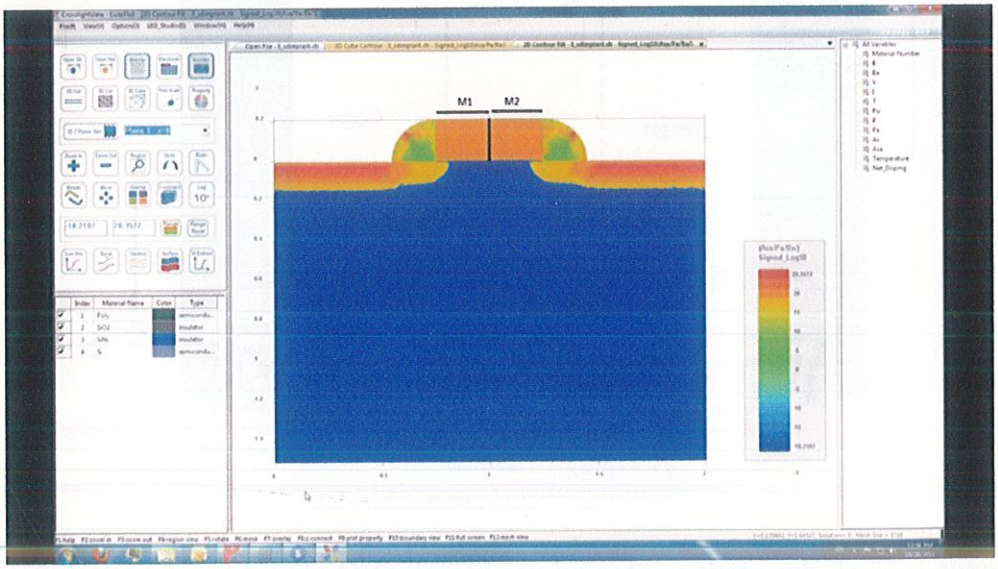


Figure 11:Final Result –DMG MOSFET Vs POLYSILICON GATE MOSFET

Sa D

simulation button for a more descriptive view of the Double Material Single Gate MOSFET.



This shows that our DMSG MOSFET is simulated successfully in the simulator i.e. we have successfully done the dry fabrication of the DMSG MOSFET . TCAD fabrication is just the one step before the original fabrication of the chip. Now we Can use our .cad file and use it to print in 3D .

Now For the Electrical Simulation We took our present Model and Also we compare it with the normal MOSFET model.

Further improvement in DMSG MOSFET:

Triple Material MOSFET- A Brief Introduction

Proposed Model

A model of the Triple Material –Single Gate MOSFET device which we have used is shown in Fig. 1 where L is the gate length , tsi is the channel thickness, and tox is gate-oxide thickness. The gate electrodes of a Triple Material –Single Gate MOSFET structure are made of three different gate materials with work functions φ m1 , φ m2 , and φ m3 respectively are deposited over the lengths L1 , L2 , and L3 on the gate-oxide layers as shown in the model. Same volatge Vgs is fed to the gate terminals of the device mas shown .

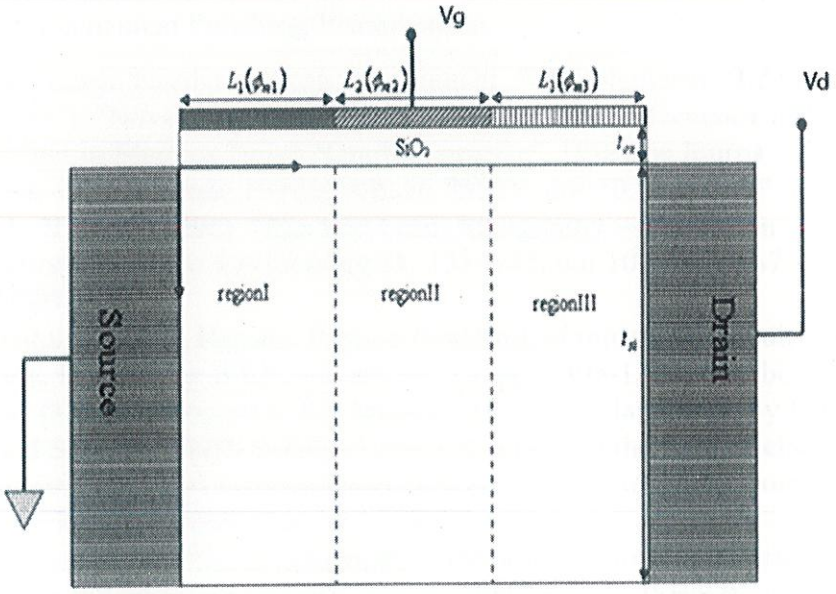


Figure 12:Triple Material Single Gate MOSFET

A Triple Material-Single Gate device can be seen as three sub-devices connected in series, each having its own threshold voltage Vth , and channel length. The drain current for each region are calculated by making use of the charge densities in each part and the variation of Ids with respect to Vds can be obtained using MATLAB.

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