JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT TEST -1 EXAMINATION- 2024

B.Tech-5th Semester (CSE/IT)

COURSE CODE(CREDITS): 3-0-0

MAX. MARKS: 15

COURSE NAME: COMPUTER ORGANIZATION AND ARCHITECTURE (18B11CI514)

COURSE INSTRUCTORS: Vivek Kumar Sehgal, Vipal Kumar, Praveen Modi

MAX. TIME: I Hour

Note: (a) All questions are compulsory.

(b) Marks are indicated against each question in square brackets.

(c) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Explain the general structure of the IAS computer with its schematic Containing:
AC, MQ, MBR, IBR, PC, MAR, IR
[C0-1][3]

2. (a) What is Amdahl's Law? Briefly characterize Amdahl's law.

(b) Consider the execution of a program that results in the execution of 2 million instructions on a 400-MHz processor. The program consists of four major types of instructions. The instruction mix and the CPI for each instruction type are given below, based on the result of a program trace experiment:

Instruction Type	CPI	Instruction Mix (%)
Arithmetic and logic	1	60
Load/store with cache hit	2	18
Branch	4	12
Memory reference with cache miss	8	10

[C0-1,2][2+2]

3. (a) A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45,000	1
Data transfer	32,000	2
Floating point	15,000	2
Control transfer	8000	2

Determine the effective CPI, MIPS rate, and execution time for this program.

(b) Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs:

Instruction Type	Instruction Count (millions)	Cycles per Instruction
Machine A		
Arithmetic and logic	8	1
Load and store	4	3
Branch	2	4
Others	4	3
Machine A		
Arithmetic and logic	10	1
Load and store	8	2
Branch	2	4
Others	4	3

Determine the effective CPI, MIPS rate, and execution time for each machine [C0-2][2+2]

4. (a) For following instructions:

0001 = Load AC from memory	Memory	CPU registers
0010 = Store AC to memory	300 1 9 4 0	3 0 0 PC
0101 = Add to AC from memory	301 5 9 4 1	AC
	302 2 9 4 1	→ 1 9 4 0 IR
	940 0 0 0 3	
	941 0 0 0 2	

What is the size of interfaced memory? And what will the contents of memory locations 940 and 941 be after program execution?

(b) List the different addressing modes of the computer system.

Or

(b) Draw the instruction cycle state diagram

[C0-2][2+2]