Mass Rapid Transit System with Emergency Shutdown System

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CERTIFICATE

This is to certify that the work entitled, "Mass Rapid Transit System With Emergency Shutdown System" submitted by Anshul Bora registered in rolls of university via no. 051079 and Abhishek Srivastava registered in rolls of university via no.051080 in partial fulfillment for the award of degree of Bachelors of Technology in "Electronics and Communication" of Jaypee University of Information Technology has been carried out under my supervision. This work has not been submitted partially or wholly to any other University or Institute for the award of this or any other degree or diploma.

9/5/9

Mr. Rohit Sharma

Project Guide

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LIST OF ABBREVIATIONS

ABBREVIATIONS	
MRTS	Mass Rapid Transit System
IC	Integrated Circuit
DTMF	Dual Tone Multiple Frequency
GSM	Global System for Mobile Communication
CDMA	Code Division Multiple Access
SIM	Subscriber Identity Module
MS	Mobile Station
IMSI	International Mobile Subscriber Identity
IMSI	International Mobile Equipment Identity
BTS	Base Transceiver Station
BSC	Base Station Controller
MSC	Mobile Switching Centre
HLR	Home Location Register
VLR	Visitor Location Register
CMOS	Complementary Metal Oxide Semiconductor
SFR	Special Function Registers
LCD	Liquid Crystal Display
IVRS	Interactive Voice Response System
AC	Alternating Current
DC	Direct Current
RAM	Random-access Memory
ROM	Read-only Memory
GND	Ground
RST	Reset

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ABSTRACT

This project proposes a novel emergency shutdown procedure for Mass Rapid Transit System (MRTS). The emergency shutdown is implement using existing GSM/CSMA line that provide global accessibility and thus replaces the conventional manual emergency shutdown system. Here, we are talking about driverless MRTS. This system is designed for fire situations and other emergencies. The setup required for the above technique to be implemented is not highly complicated. The whole setup consists of simple electronic components and the interfacing between them can be done easily. The utility of the above setup is quite high. In our project we have tried to implement the most primary model of the same.

CHAPTER 1

INTRODUCTION TO MASS RAPID TRANSIT SYSTEM

SECTION 1.1: AIM OF THE PROJECT

The aim of the project is the user mobility by controlling the electrical and electronics devices from a remote place. We have introduced the novel technique of emergency stop in Mass Rapid Transit System using existing GSM/CDMA network and to replace the conventional manual emergency shutdown system. We have tried to implement the most basic model but we can incorporate this system with more add-ons to make it more practical in all respects. Here we have designed a circuit that can be connected to the mobile unit that can handle wireless communication functions like subscriber identity module (SIM).This basic setup or base setup module have to be installed at the place where the user want to control the devices .This base unit must be connected to the power supply. While taking the security part into consideration we here have appreciated and implemented the use of single digital access code which is only available with the authenticated user only. As soon as the user is verified by the system the user gets the pass key to control the appliances means switching them on. This whole process can be implemented by the remote user very easily through the mobile phone.

SECTION 1.2: EMERGENCY SHUTDOWN PROCEDURE FOR MASS RAPID TRANSIT SYSTEM

In our project we have decided to implement the embedded system concept due to easy understanding and less complexity as compared to the others. Here the design process is very simple and has to be implemented by using already available digital networks and the GSM cellular networks. In this project we have tried to change the conventional manual system of emergency shutdown with DTMF control system. This system is more robust and protected and can be easily monitored.

We will be using microcontroller as CPU, the model which we are designing is controlled by the stepper motor. The distance between the two stations is set before with the help of

programming. The project is designed in such a way that it follows certain protocols. These protocols are:

- The MRTS is designed for three stations, named A, B and C.
- The stoppage time is of 5 seconds.
- The time between two consecutive stations is 10 seconds.
- Before arriving and departing at any station the train blows the buzzer.
- These events will be displayed accordingly with the help of 2 line display LCD.
- Forward and backward movement will be indicated with the help of LED.

These protocols are burned in to the microcontroller with the help of assembly codes. Now replacing the conventional emergency stop with DTMF controlled stop where each wagon will be provided with a unique receiver and an emergency number. This unique number will be the one which will act as a receiver of DTMF circuit. Emergency number will act like a valid DTMF tone to this circuit. The circuit will not respond to the invalid tone. Passenger has a choice to connect to the receiver at any instant and may shutdown the system by sending valid DTMF tone.

SECTION 1.3: WHY THIS SYSTEM?

Present metro uses alarm button or emergency intercom to speak to the train operator and follow his instructions and in trains we have mechanical stop systems which has very high complexity and cost. Nevertheless, the new system is designed to work in conjunction with existing system and can be easily installed and old system can be gradually receded. Therefore, its new wireless remote emergency stop system designed to eliminate costly hard-wiring of emergency-stop panic switches. It is the way to reduce unnecessary stops, as every time any passenger uses this system, a log is generated. If such a system is implemented then there will be minimal misuse of this facility. Any misuse can be easily caught and penalized accordingly.

CHAPTER 2

DESCRIPTION OF COMPONENTS

SECTION 2.1: TECHNOLOGIES THAT MUST BE DISCUSSED

Before we start giving the description of the components it is important to discuss some technologies for proper understanding of the project.

DTMF Tones

DTMF tone is a tone consisting of two superimposed frequencies. The individual frequency is chosen such that it is easy to design filters and easy to transmit the tones through a telephone line having a bandwidth of approximately 3.5 KHz. Initially, DTMF tones were meant only to send control signals over the telephone lines. However, recent works have shown that DTMF may be used for data transfer. With standard decoders it is possible to send 10 beeps per second i.e. five bits per second. DTMF standard specifies 50ms tones and 600ms delay between two successive tones.

DTMF Frequencies

Table 2.1: DTMF Frequency Matrix

1209	1336	1477	1633	KHz
1	2	3	A	**697**
4	5	6	B	**770**
7	8	9	C	**852**
*	0	#	D	**941**

Note that the penultimate column of DTMF frequencies is not commonly seen in the telephones we use, but are quite often used in telephone exchanges all over the world. Nowadays, telephones across the world are dialed using DTMF tones, which help configuring the telephone exchanges and route to the destination telephone. A transceiver of 2.7 MHz is normally used to send floating codes. DTMF was designed to be able to send these floating codes using a microphone. Each beep (or digit you dial on the telephone) is composed of two concurrent frequencies super imposed in amplitude. The shift between the two individual frequencies is termed as `twist`. If the twist is equal to

4db, the higher frequency is louder by 4db.If the lower frequency is loud, then the twist is said to be the negative.

GSM

A GSM network is composed of several entities, whose functions and interface are specified. The GSM network can be divided into four parts:

Mobile Station:

The mobile station (MS) consist of the physical equipment, such as the radio transceiver, display, digital processing unit and a smart card called the subscriber identity module (SIM). The SIM provides the personal mobility, so the user can have the access to all the subscribed services irrespective of both the location of the terminal and the use of specific terminal. By inserting the SIM card into another GSM cellular phone, the user is able to receive calls at that phone, make calls from that phone and other services.

The mobile equipment is uniquely identified by the international mobile equipment identity (IMEI). The SIM card contains the international mobile subscriber identity (IMSI), identifying the subscriber, a secret key for authentication, and other user information. The IMSI and IMEI are independent, thereby providing personal mobility. The SIM card may be protected against unauthorized use by a password or personal identity number.

Base Station Subsystem:

The base station subsystem is composed of two parts, the base transceiver station (BTS) and the base station controller (BSC).these communicate across the specified interface, allowing (as in the rest of the system) operation between components made by different suppliers.

The Base Transceiver Station houses the radio transceivers that define a cell and handles the radio link protocols with the Mobile Station. In a large Urban Area, there will

potentially be a large number of BTS deployed. The requirements for a BTS are ruggedness, reliability, portability and minimum cost.

The Base Station Controller manages the radio resources for one or more BTS. It handles radio channel setup, frequency hopping, and handovers, as described below. The BSC is the connection between the mobile and the mobile switching center (MSC). The BSC also translates the 13kbps voice channel used over the radio link to the standard 64 kbps channel used by the Public Switched Telephone Network or ISDN.

Network Subsystem:

Central component of the network subsystem is the Mobile Services Switching Center (MSC). It acts like a normal switching node of the PSTN or ISDN, and in addition provides all the functionality needed to handle a mobile subscriber, such as registration, authentication, location, updating, and handovers and call routing to a roaming subscriber. These services are provided in conjunction with several functional entities which together form the Network Subsystem. The MSC provides the connection to the public fixed network (PSTN or ISDN), and signaling between the functional entities uses the ITUT signaling system Number 7 (SS7), used in ISDN and widely used in current public networks.

The Home Location Register (HLR) and the Visitor Location Register (VLR), together with the MSC, provide the call routing (possibly international) roaming capabilities of GSM. The HLR contains all the administrative information of each subscriber registered in corresponding GSM network along with the current location of the mobile. The current location of the mobile station roaming number (MSRN) which is regular ISDN number used to rout a call to the MSC where the mobile is currently located. There is logically 1 HLR per GSM network, although it may be implemented as a distributed database.

The Visitor Location Register contains selected administrative information from the HLR, necessary for all control and provision for the subscribed services, for each mobile currently located in the geographical area controlled by the VLR. Although each

functional entity can be implemented as an independent unit, most manufacturers of the switching equipment implement one VLR together with one MSC, so that the geographical area controlled by the MSC corresponds to that controlled by the VLR simplifying the signaling required. Note that the MSC contains no information about particular mobile stations-this information is stored in the location registers

Operational subsystem:

The others registers are used for the authentication and security purposes .The equipment identity register is a database that contains a list of all valid mobile equipment, where each mobile is identified by the IMEI. The authentication centre is a protected database that stores the copy of the secret key stored in each SIM card, which is used for authentication and encryption over the radio channel.

SECTION 2.2: CLASSIFICATION OF THE PROJECT

The complete circuit is broadly divided into two parts:

- Remote Control
- Control Unit

Remote control

The remote control unit used in our project is any kind of telephone which can make a call to the control unit installed at the MRTS application. The phone must have a facility to encode DTMF tones and send it to control unit. Nowadays, all phones have the facility of DTMF coding and all networks support sending of these tones. It has become an international standard and is being used all over. DTMF signals can also be generated through dedicated IC's or by using RC networks connected to a microprocessor.

The latter method is bit difficult and complicated to implement, and high accuracy is needed. There is a trade-off between the frequency of the crystal and the time length of a non standard cycle in the implementation of the latter method. Hence this method is used.

Control Unit

The control unit is further divided into 3 sections:

1. DTMF Decoder
2. Microcontroller
3. Power Circuit

DTMF Decoder

In DTMF decoder circuit we use IC8870, which converts the dual tones to corresponding binary outputs (Binary Coded Decimal).

AC register signaling is used in DTMF telephones, here tones rather than make/break pulse are used for dialing, and each dialed digit is uniquely represented by a pair of sine waves tones. These tones (one from low group for row and another from high group for column) are sent to the exchange when a digit is dialed by pushing the key, these tone lies within the speech band of 300 to 3400 Hz, and are chosen so as to minimize the possibility of any valid frequency pair existing in normal speech simultaneously. Actually, this minimization is made possible by forming pairs with one tone from the higher group and the other from the lower of frequencies. A valid DTMF signal is the sum of two tones, one from a lower group (697-940 Hz) and the other from a higher group (1209-1663 Hz). Each group contains four individual tones to represent digits 1 through 9 and 0. Tones in DTMF dialing are so chose that none of the tones is Harmon IC of are other tone. Therefore is no change of distortion caused by harmonics. Each tone is sent as long as the key remains pressed. The DTMF signal contains only one component from each of the high and low group. This significantly simplifies decoding because the composite DTMF signal may be separated with band pass filters into single frequency components, each of which may be handled individually.

The design of a DTMF receiving system can generally be broken down into three functional blocks.

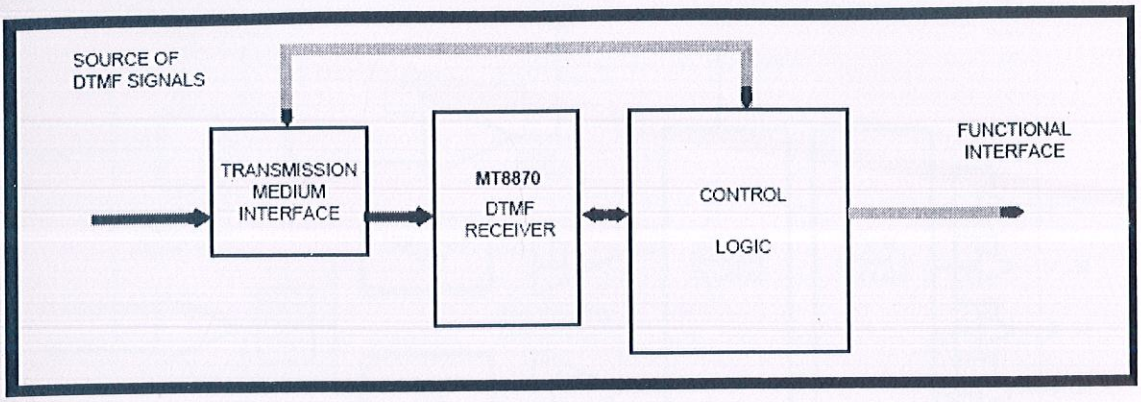


Fig 2.1: Modular Approach to DTMF Receiver Systems

The first consideration is the interface to the transmission medium. This may be as simple as a few passive components to adequately configure the MT8870's input stage or as complex as some form of demodulation, multiplexing or analog switching system. The second functional block is the DTMF receiver itself. This is where the receiving system's parameters can be optimized for the specific signal conditions delivered from the "front end" interface. The third, and perhaps most widely varying function, is the output control logic. This may be as simple as a 4 to 16 line decoder, controlling a specific function for each DTMF code, or as complex as a full blown computer handling system protocols and adaptively varying the tone receiver's parameters to adjust for changing signal conditions.

Several emergency medical service networks currently use DTMF signals to control radio repeaters. Functions are, typically, mobile identification, selection of appropriate repeater links, selection of repeater frequencies, reading of repeater status, and for completing automatic phone patch links.

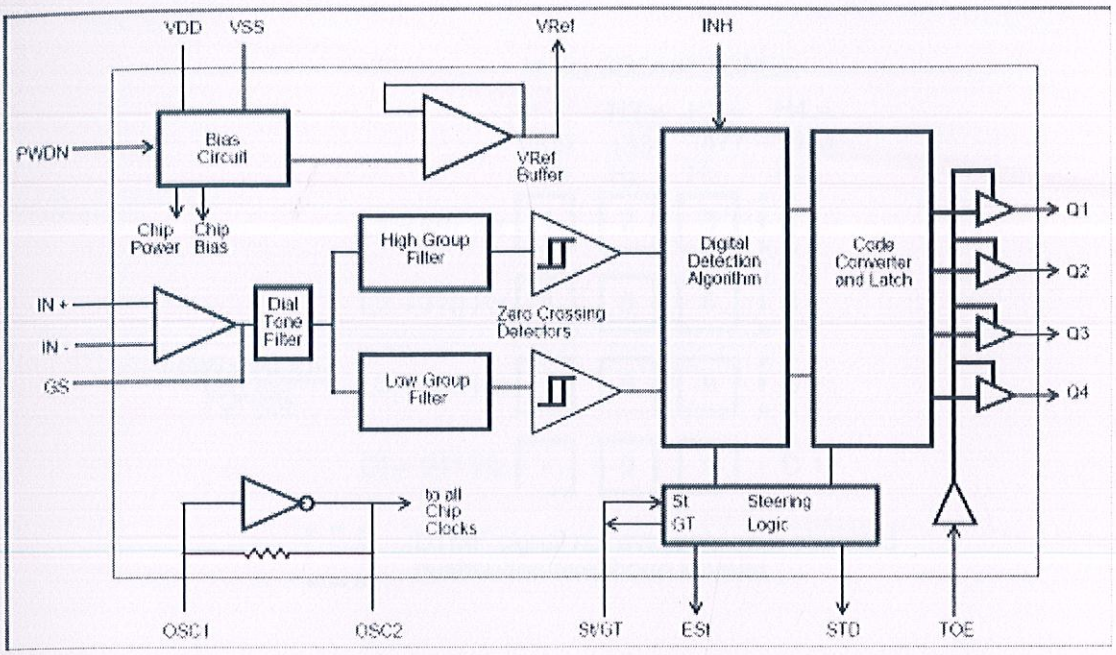


Fig 2.2: MT8870 Functional Block Diagram

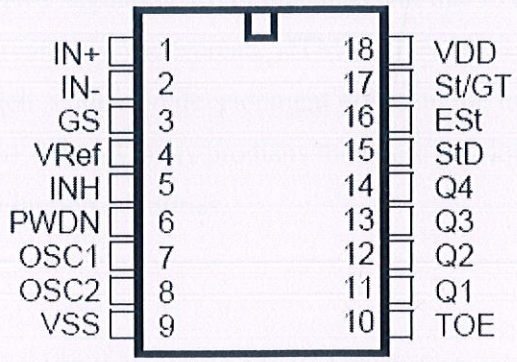


Fig 2.3: Pin Diagram of 8870IC

The DTMF coding scheme ensures that each signal contains one and only one component from each of the high and low groups. This significantly simplifies decoding because the composite DTMF signal may be separated with band pass filters, into its two single frequency components each of which may be handled individually. As a result DTMF coding has proven to provide a flexible signaling scheme of excellent reliability, hence motivating innovative and competitive decoder design.

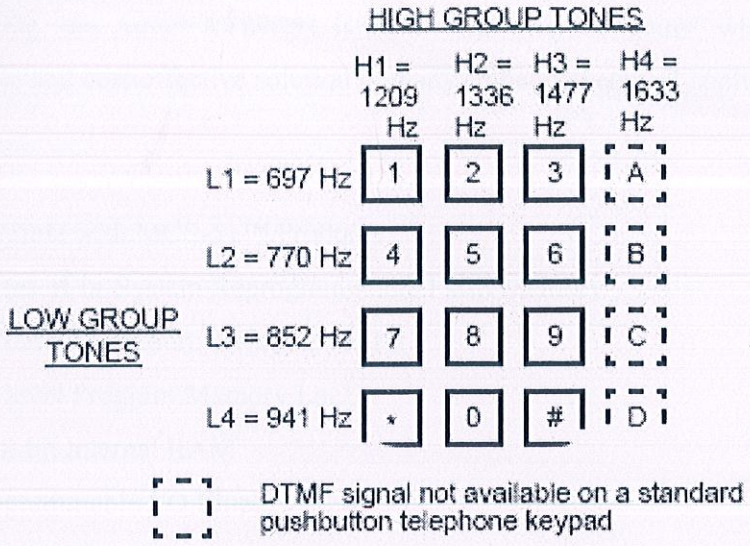


Fig 2.4: The Dual Tone Multiple Frequency (DTMF) keypad.

The applications for DTMF signaling are tremendous and due to innovative technological advances its use is increasingly widespread. DTMF offers highly reliable, cost effective signaling solutions which require no development effort on the user's part. The advent of single chip receivers has allowed many products that were previously not cost effective to be manufactured in production quantities.

Microcontroller

8051 microcontroller has 128 bytes of RAM, 4K bytes of on-chip ROM, two timers, one serial port, and four ports (each 8-bits wide) all on a single chip. The 8051 is an 8-bit processor i.e. the CPU can work on only 8 bits of data at a time. The fixed amount of on-chip ROM, RAM, and number of I/O ports in microcontroller makes them ideal for many applications in which cost and space are critical.

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash programmable and erasable read only memory (PEROM). The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional

nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer, which provides a highly flexible and cost-effective solution to many embedded control applications.

Features:

- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low-power Idle and Power-down Modes

Block Diagram

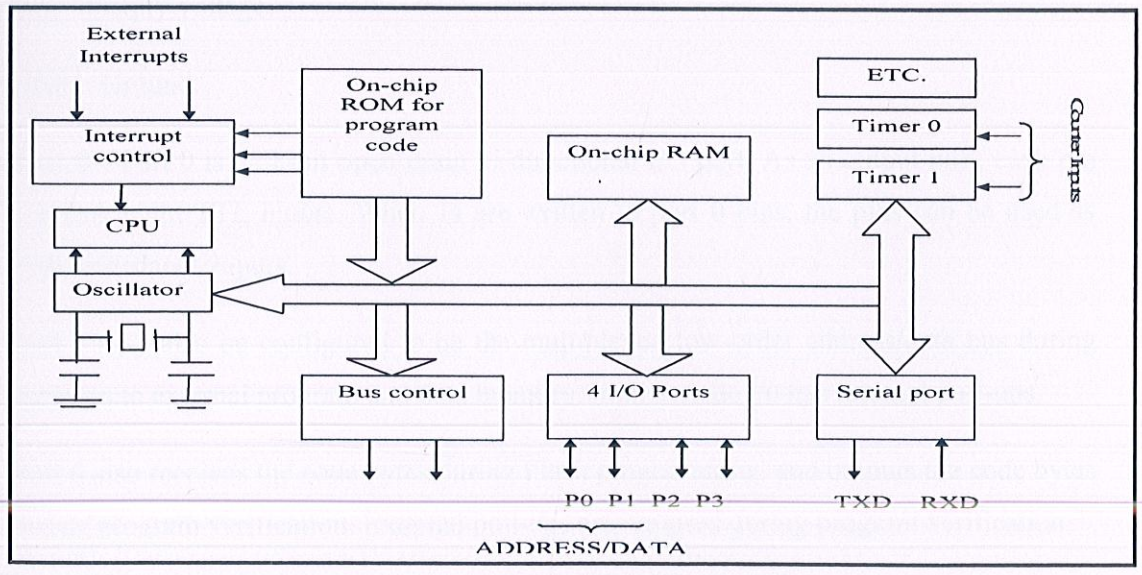


Fig 2.5: Block diagram of microcontroller

Pin Configuration

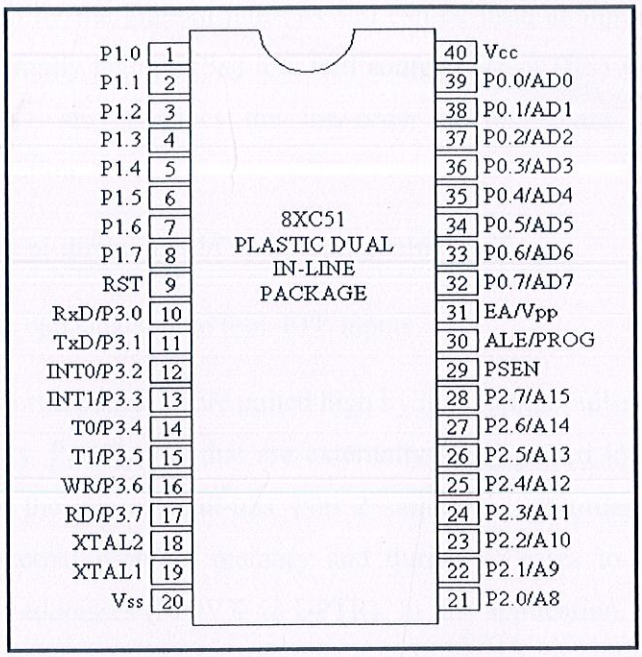


Fig 2.6: Pin configuration

Pin Description

V_{CC} - Supply voltage.

GND - Ground.

Port 0 - Port 0 is an 8-bit open-drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pull-ups are required during program verification

Port 1 - Port 1 is an 8-bit bi-directional I/O port with internal pull-ups.

The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2 - Port 2 is an 8-bit bi-directional I/O port with internal pull-ups.

The Port 2 output buffers can sink/source four TTL inputs.

When 1s are written to Port 2 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that uses 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that uses 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3 - Port 3 is an 8-bit bi-directional I/O port with internal pullups.

The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pullups. Port 3 also serves the functions of various special features of the AT89C51 as listed below:

RST - Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG - Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN - Program Store Enable is the read strobe to external program memory. When the AT89C51 is executing code from external program memory, PSEN is activated twice

Table:2.2: Port 3 of 8051

Port No.	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP - External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.

EA should be strapped to VCC for internal program executions.

This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming, for parts that require 12-volt VPP.

XTAL1 - Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2 - Output from the inverting oscillator amplifier.

The 8051 Registers

The most widely used registers of the 8051 are A (accumulator), B, R0, R1, R2, R3, R4, R5, R6, R7, DPTR (data pointer), and PC (program counter). All of the above registers are 8-bits, except DPTR and the program counter. The 8 bots of a register are shown below from the MSB (most significant bit) D7 to the LSB (least significant bit) D0.

D7	D6	D5	D4	D3	D2	D1	D0

Program Counter

The program counter points to the address of the next instruction to be executed. As the CPU fetches the opcode from the program ROM, the program counter is incremented to point to the next instruction. The PC is 16 bits wide i.e. it can access program addresses 0000 to FFFFH, a total of 64K bytes of code.

Program Status Word (PSW) Register

The PSW contains status bits that reflect the current state of the CPU and is also called flag register. The PSW contains the Carry bit, the Auxiliary Carry bit, the two register bank select bits, the overflow flag bit, a parity bit, and two users' definable status flags.

CY	AC	F0	RS1	RS0	OV	---	P

Table 2.3: Program Status Word Register

Registers	Pins	
CY	PSW.7	Carry flag
AC	PSW.6	Auxiliary carry flag.
---	PSW.5	Available to the user for general purpose
RS1	PSW.4	Register Bank selector bit 1
RS0	PSW.3	Register Bank selector bit 0
OV	PSW.2	Overflow flag
---	PSW.1	User definable bit
p	PSW.0	Parity flag

Table 2.4: Register Banks of 8051

RS1	RS0	Register Bank	Address
0	0	0	00H – 07H
0	1	1	08H – 0FH
1	0	2	10H – 17H
1	1	3	18H – 1FH

CY, the Cary Flag

This flag is set whenever there is a carry out from the D7 bit. This flag bit is affected after an 8-bit addition or subtraction. It can also be set to

1 or 0 directly by an instruction such as "SETB C" and "CLR C" where "SETB C" stands for "set bit carry" and "CLR C" for "clear carry".

AC, the Auxiliary Flag

If there is a carry from D3 to D4 during an ADD or SUB operation, this bit is set; otherwise, it is cleared. This flag is used by instructions that perform BCD (binary coded decimal) arithmetic.

P, the Parity Flag

The parity flag reflects the number of 1s in the A (accumulator) register only. If the A register contains an odd number of 1s, then P=1. Therefore, P=0 if A has an even number of 1s.

OV, the Overflow Flag

This flag is set whenever the result of a signed number operation is too large, causing the high-order bit to overflow into the sign bit.

Ram memory space allocation in the 8051

There are 128 bytes of RAM in the 8051, which are assigned addresses 00 to 7FH. These 128 bytes are divided into three different groups:

1. A total of 32 bytes from locations 00 to 1H hex are set aside for register banks and the stack.
2. A total of 16 bytes from locations 20H to 2FH are set aside for bit-addressable read/write memory.
3. A total of 80 bytes from locations 30H to 7FH are used for read and write storage, or what is normally called a scratch pad. These 80 locations of RAM are widely used for the purpose of storing data and parameters by 8051 programmers.

Register Banks in the 8051

The 32 bytes of RAM which is set aside for the register banks and stack is divided into 4 banks of registers in which each bank has 8 registers, R0 – R7. RAM locations from 0 to 7 are set aside for bank 0 of R0 – R7 where R0 is RAM location 0, R1 is RAM location 1, R2 is location 2, and so on, until memory location 7 which belongs to R7 of bank 0. The second bank of registers R0 – R7 starts at RAM location 08 and goes to location

0FH. The third bank of R0 – R7 starts at memory location 10H and goes to location 17H; and finally RAMS locations 18H to 1FH are set aside for the fourth bank of R0 – R7. The following table shows how the 32 bytes are allocated into 4 banks:

Bank 0	
R7	7
R6	6
R5	5
R4	4
R3	3
R2	2
R1	1
R0	0

Bank 1	
R7	7
R6	6
R5	5
R4	4
R3	3
R2	2
R1	1
R0	0

Bank 2	
R7	7
R6	6
R5	5
R4	4
R3	3
R2	2
R1	1
R0	0

Bank 3	
R7	7
R6	6
R5	5
R4	4
R3	3
R2	2
R1	1
R0	0

Stack in 8051

The stack is a section of RAM used by the CPU to store information temporarily. This information could be data or an address. The CPU needs this storage area since there are only a limited number of registers. The register used to access the stack is called the SP (stack pointer) register. The stack pointer in the 8051 is only 8 bits wide i.e. it can take values of 00 to FFH. When the 8051 is powered up, the SP register contains value 07 which implies that RAM location 08 is the first location being used for the stack by the 8051. The storing of a CPU register in the stack is called a PUSH, and loading the contents of the stack back into a CPU register is called a POP. In other words, a register is pushed onto the stack to save it and popped off the stack to retrieve it.

Pushing onto the stack

In the 8051 the stack pointer (SP) is pointing to the last used location of the stack. As data is pushed onto the stack, the stack pointer (SP) is incremented by one and the contents of the register are saved on the stack. To push the registers onto the stack, RAM addresses are used.

Popping from the stack

Popping the contents of the stack back into a given register is the opposite process of pushing. With every pop, the top byte of the stack is copied to the register specified by the instruction and the stack pointer is decremented once.

Addressing modes

The addressing modes in the microcontroller instruction set are as follows:

1. Direct Addressing

In direct addressing, the operand is specified by an 8-bit address field in the instruction. Only internal RAM and SFRs cab be directly accessed.

2. Indirect Addressing

In indirect addressing, the instruction specifies a register that specifies a register that contains the address of the operand. Both internal and external RAM can be indirectly accessed.

The address register for 8-bit addresses can be either the stack pointer or R0 or R1 of the selected register bank. The address register for 16-bit addresses can be only the 16-bit data pointer register, DPTR.

3. Register Instructions

The register banks, which contain registers R0 through R7, can be accessed by instructions whose opcodes carry a 3-bit register specification. Instructions that access the

registers this way make efficient use of code, since this mode eliminates an address byte. When the instruction is executed, one of the eight registers in the selected bank is accessed. One of four banks is selected at execution time by the two bank select bits in the PSW.

4. Register-specific instructions

Some instructions are specific to a certain register. For example, some instructions always operate on the Accumulator, so no address byte is needed to point to it. In these cases, the opcode itself points to the correct register.

5. Immediate Constants

The value of a constant can follow the opcode in program memory. For example,

MOV A, #100

Load the Accumulator with the decimal number 100. The same number could be specified in hex digits as 64H.

6. Indexed Addressing

Program memory can only be accessed via indexed addressing. This addressing mode is intended for reading look-up labels in program memory. A 16-bit base register (either DPTR or the Program Counter) points to the base of the table, and the accumulator is set up with the table entry number. The address of the table entry in program memory is formed by adding the accumulator data to the base pointer.

Power Circuit (STK6712BMK4)

The STK6712BMK4 is a uni-polar fixed-current chopper type 4-phase stepping motor driver hybrid IC (HIC) which uses a MOSFET power device. The excitation sequence signal is active low.

Features

- This IC has the features of the STK6712BMK3, plus a simultaneous input prevention circuit that protects the IC from any malfunction of the excitation signal.
- Self-excitation design means chopping frequency is determined by motor L and R. Supports chopping at 20 kHz or higher.
- Very low number of external components required.
- Wide operating supply voltage range (VCC1 = 18 to 42V)
- Excitation sequence signal is active low, and is TTL level for direct interfacing to the microcomputer and gate array.
- The uni-polar design enables use as a driver for hybrid, PW, or VR type stepping motors.
- Supports W1-2 phase operation, with a dual V_{ref} pin.

Applications

- Serial printer, line printer, and laser beam printer (LBP) paper feed and carriage motor drivers.
- PPC scanner and LBP paper feed drivers.
- XY plotter pen drivers.
- Industrial robot applications, etc.

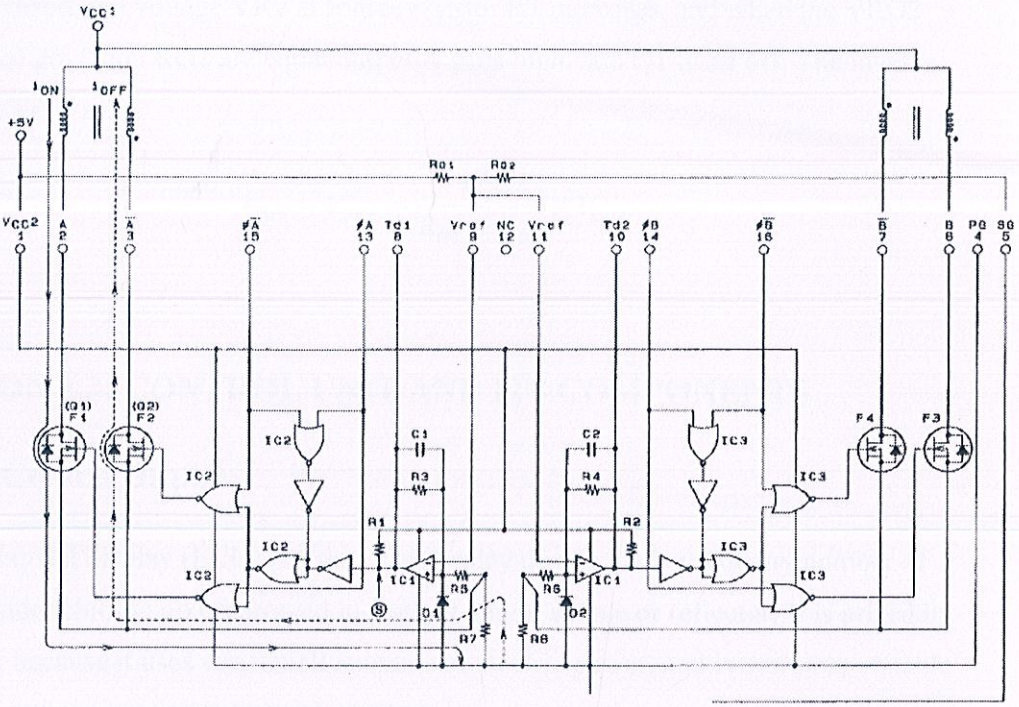


Fig 2.7: STK6712BMK4 Internal Equivalent Circuit

The operation for a 4-phase dual-excitation example is described below.

The STK6712BMK4 equivalent circuit is given in Fig. 1. The circuit consists of the phase drivers, the comparator, the PWM excitation select and the current detect resistance. In Fig. 1 øA is input with low, and øA with high. When Q1 goes on, the +pin of IC1 (comparator) goes low, making IC1 output low also. A winding current iON through Q1 increases as:

$$i_{ON} = \frac{V_{CC1} - V_{SAT}}{R}\left(1 - e^{-\frac{R}{L}t}\right)$$

L: motor conductor winding.

R: sum of winding resistance and current detect resistance.

For this reason, pin voltage VR7 at source resistor R7 increases, and when the VRO2 voltages of pin 8 and RO2 are equal output A goes high, and Q1 turns off. The inverse voltage VTP is as:

$$V_{TP} = V_{ref} = \frac{R_{o2}}{R_{o1} + R_{o2}} \times V_{cc2}$$

SECTION 2.3: CONTROL UNIT AND ITS COMPONENTS

Liquid Crystal Display

A liquid crystal display (LCD) is a thin, flat display device made up of any number of color or monochrome pixels arrayed in front of a light source or reflector. It is prized by engineers because it uses very small amounts of electric power, and is therefore suitable for use in battery-powered electronic devices.

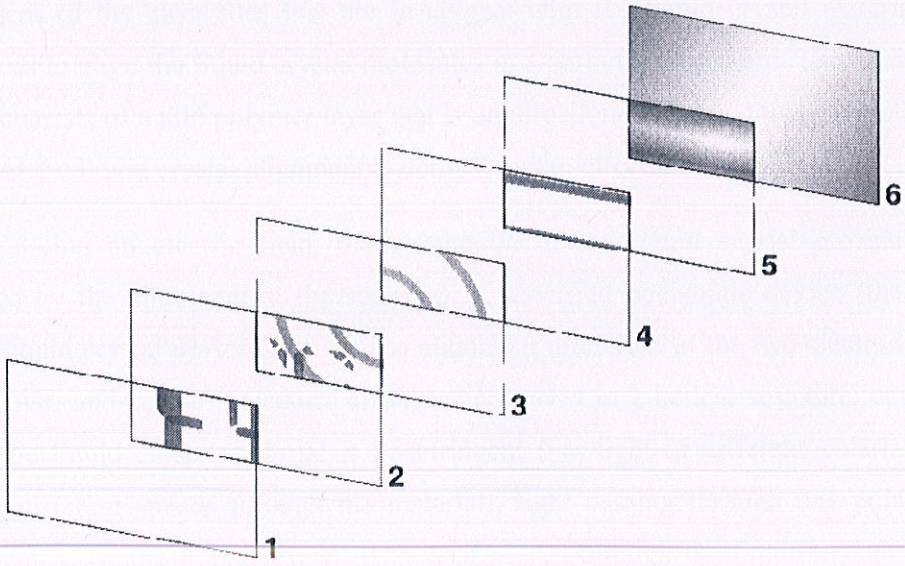


Fig 2.8: Reflective twisted pneumatic liquid crystal display.

1. Vertical filter film to polarize the light as it enters.
2. Glass substrate with ITO electrodes. The shapes of these electrodes will determine the dark shapes that will appear when the LCD is turned on or off. Vertical ridges etched on the surface are smooth.
3. Twisted pneumatic liquid crystals.
4. Glass substrate with common electrode film (ITO) with horizontal ridges to line up with the horizontal filter.
5. Horizontal filter film to block/allow through light.
6. Reflective surface to send light back to viewer

Each pixel of an LCD consists of a layer of liquid crystal molecules aligned between two transparent electrodes, and two polarizing filters, the axes of polarity of which are perpendicular to each other. With no liquid crystal between the polarizing filters, light passing through one filter would be blocked by the other.

The surfaces of the electrodes that are in contact with the liquid crystal material are treated so as to align the liquid crystal molecules in a particular direction. This treatment typically consists of a thin polymer layer that is unidirectionally rubbed using a cloth (the direction of the liquid crystal alignment is defined by the direction of rubbing).

Before applying an electric field, the orientation of the liquid crystal molecules is determined by the alignment at the surfaces. In a twisted pneumatic device (the most common liquid crystal device), the surface alignment directions at the two electrodes are perpendicular, and so the molecules arrange themselves in a helical structure, or twist. Because the liquid crystal material is bi-refringent (i.e. light of different polarizations travels at different speeds through the material), light passing through one polarizing filter is rotated by the liquid crystal helix as it passes through the liquid crystal layer, allowing it to pass through the second polarized filter. Half of the light is absorbed by the first polarizing filter, but otherwise the entire assembly is transparent.

When a voltage is applied across the electrodes, a torque acts to align the liquid crystal molecules parallel to the electric field, distorting the helical structure. This reduces the rotation of the polarization of the incident light, and the device appears gray. If the applied voltage is large enough, the liquid crystal molecules are completely untwisted and the polarization of the incident light is not rotated at all as it passes through the liquid crystal layer. This light will then be polarized perpendicular to the second filter, and thus be completely blocked and the pixel will appear black. By controlling the voltage applied across the liquid crystal layer in each pixel, light can be allowed to pass through in varying amounts, correspondingly illuminating the pixel.

With a twisted pneumatic liquid crystal device it is usual to operate the device between crossed polarizer, such that it appears bright with no applied voltage. With this setup, the dark voltage-on state is uniform. The device can be operated between parallel polarizer, in which case the bright and dark states are reversed (in this configuration, the dark state appears blotchy).

Both the liquid crystal material and the alignment layer material contain ionic compounds. If an electric field of one particular polarity is applied for a long period of time, this ionic material is attracted to the surfaces and degrades the device performance. This is avoided by applying either an alternating current, or by reversing the polarity of the electric field as the device is addressed (the response of the liquid crystal layer is identical, regardless of the polarity of the applied field).

LCD Interfacing

V_{CC}, V_{SS}, and V_{EE}

While V_{CC} and V_{SS} provide +5V and ground, respectively, V_{EE} is used for controlling LCD contrast.

RS, *register select*

There are two important registers inside the LCD. If RS = 0, the instruction command code register is selected, allowing the user to send a command such as clear display,

cursor at home, etc. If RS = 1the data register is selected, allowing the user to send data to be displayed on the LCD.

R/W, *read/write*

R/W input allows the user to write information to the LCD or read information from it. R/W = 1 when reading; R/W = 0 when writing.

E, *enable*

This pin is used by the LCD to latch information presented to its data pins. When data is supplied to data pins, a high-to-low pulse must be applied to this pin in order for the LCD to latch in the data present at the data pins. This pulse must be a minimum of 450 ns wide.

D0 – D7

The 8 – bit data pins, D0 – D7, are used to send information to the LCD or read the contents of the LCD's internal registers. To display letters and numbers, we send ASCII codes for the letters A – Z, a – z, and numbers 0 – 9 to these pins while making RS = 1.

Table 2.5: Pin Descriptions for LCD

Pin	Symbol	I/O	Description
1	VSS	--	Ground
2	VCC	--	+5V power supply
3	VEE	--	Power supply to control contrast
4	RS	1	RS = 0 to select command register, RS = 1 to select data register
5	R/W	1	R/W = 0 for write, R/W = 0 for read
6	E	I/O	Enable
7	DB0	I/O	The 8-bit data bus
8	DB1	I/O	The 8-bit data bus
9	DB2	I/O	The 8-bit data bus
10	DB3	I/O	The 8-bit data bus
11	DB4	I/O	The 8-bit data bus
12	DB5	I/O	The 8-bit data bus
13	DB6	I/O	The 8-bit data bus
14	DB7	I/O	The 8-bit data bus

Table 2.6: LCD Addressing

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Line1 (min)	1	0	0	0	0	0	0	0
Line1 (max)	1	0	1	0	0	1	1	1
Line2 (min)	1	1	0	0	0	0	0	0
Line2 (max)	1	1	1	0	0	1	1	1

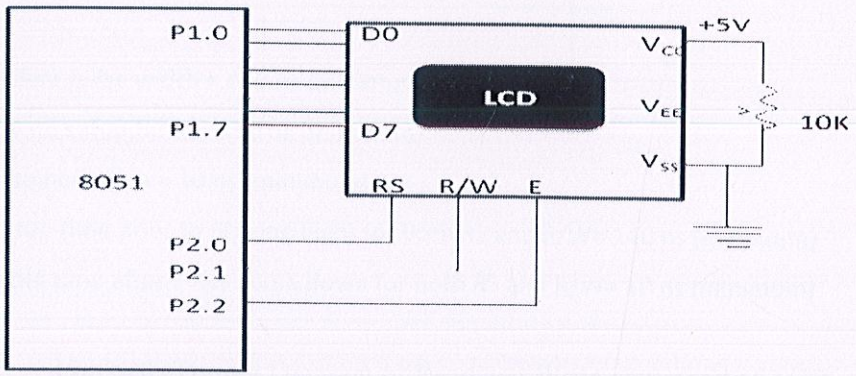
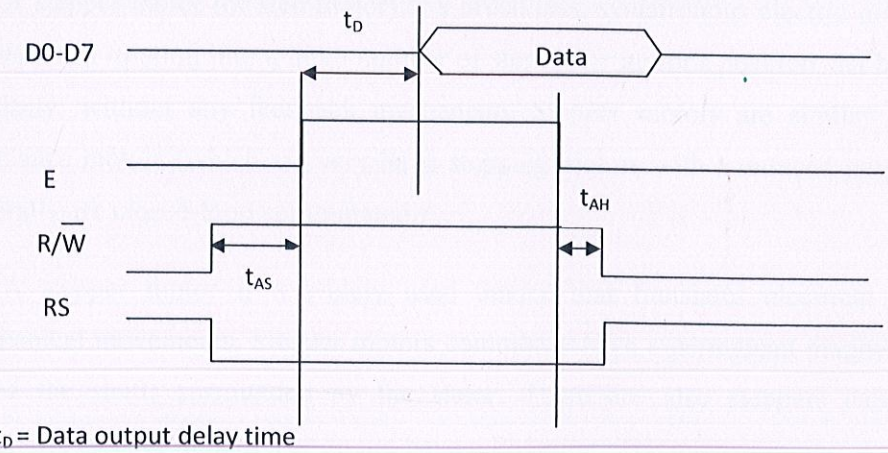


Fig 2.9: LCD Connections



t_D = Data output delay time

t_{AS} = Setup time prior to E(going high) for both RS and R/W= 140 ns (minimum)

t_{AH} = Hold time after E has come down for both RS and R/W= 10 ns (minimum)

Note: Read requires an L-to-H pulse for the E pin.

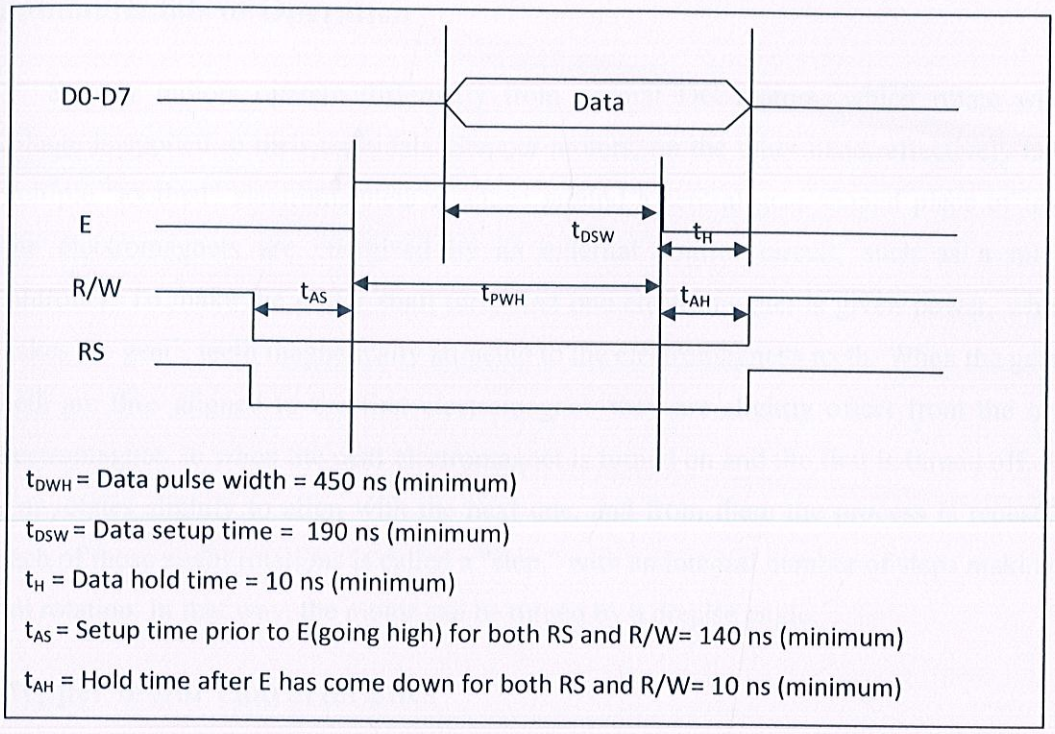


Fig 2.10: Timing Diagram of Read and Write command of LCD

Stepper Motor

A stepper motor (or step motor) is a brush less, synchronous electric motor that can divide a full rotation into a large number of steps. The motor's position can be controlled precisely, without any feedback mechanism. Stepper motors are similar to switched reluctance motors (which are very large stepping motors with a reduced pole count, and generally are closed-loop commutated.)

A stepper motor is a widely used device that translates electrical pulses into mechanical movements. Stepper motors commonly have a permanent magnet rotor (also called the shaft) surrounded by the stator. There are also steppers called variable reluctance stepper motors that do not have a PM rotor. The most common stepper motors have four stator windings that are paired with center-tapped common. This type of stepper motor is commonly referred to as a four-phase or unipolar stepper motor.

Fundamentals of Operation

Stepper motors operate differently from normal DC motors, which rotate when voltage is applied to their terminals. Stepper motors, on the other hand, effectively have multiple "toothed" electromagnets arranged around a central gear-shaped piece of iron. The electromagnets are energized by an external control circuit, such as a micro controller. To make the motor shaft turn, first one electromagnet is given power, which makes the gear's teeth magnetically attracted to the electromagnet's teeth. When the gear's teeth are thus aligned to the first electromagnet, they are slightly offset from the next electromagnet, so when the next electromagnet is turned on and the first is turned off, the gear rotates slightly to align with the next one, and from there the process is repeated. Each of those slight rotations is called a "step," with an integral number of steps making a full rotation. In that way, the motor can be turned by a precise angle.

Stepper motor characteristics

Stepper motors are constant-power devices (power = angular velocity x torque). As motor speed increases, torque decreases. The torque curve may be extended by using current limiting drivers and increasing the driving voltage. Steppers exhibit more vibration than other motor types, as the discrete step tends to snap the rotor from one position to another. This vibration can become very bad at some speeds and can cause the motor to lose torque. The effect can be mitigated by accelerating quickly through the problem speed range, physically damping the system, or using a micro-stepping driver. Motors with a greater number of phases also exhibit smoother operation than those with fewer phases.

Unipolar motors

A unipolar stepper motor has logically two windings per phase, one for each direction of current. Since in this arrangement a magnetic pole can be reversed without switching the direction of current, the commutation circuit can be made very simple (e.g. a single transistor) for each winding. Typically, given a phase, one end of each winding is

made common: giving three leads per phase and six leads for a typical two phase motor. Often, these two phase commons are internally joined, so the motor has only five leads.

A microcontroller or stepper motor controller can be used to activate the drive transistors in the right order, and this ease of operation makes unipolar motors popular with hobbyists; they are probably the cheapest way to get precise angular movements.

A quick way to determine if the stepper motor is working is to short circuit every two pairs and try turning the shaft, whenever a higher than normal resistance is felt, it indicates that the circuit to the particular winding is closed and that the phase is working.

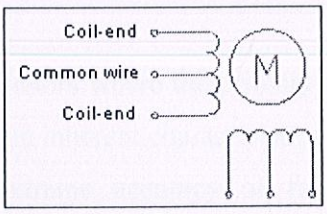


Fig 2.11: Unipolar stepper motor coils

Unipolar stepper motors with six or eight wires may be driven using bipolar drivers by leaving the phase commons disconnected, and driving the two windings of each phase together.

Stepper motor drive circuits

Stepper motor performance is strongly dependent on the drive circuit. Torque curves may be extended to greater speeds if the stator poles can be reversed more quickly, the limiting factor being the winding inductance. To overcome the inductance and switch the windings quickly, one must increase the drive voltage. This leads further to the necessity of limiting the current that these high voltages may otherwise induce.

Applications

Computer-controlled stepper motors are one of the most versatile forms of positioning systems. They are typically digitally controlled as part of an open loop system, and are simpler and more rugged than closed loop servo systems.

Industrial applications are in high speed pick and place equipment and multi-axis machine CNC machines often directly driving lead screws or ball screws. In the field of lasers and optics they are frequently used in precision positioning equipment such as linear actuators, linear stages, rotation stages, goniometry, and mirror mounts. Other uses are in packaging machinery, and positioning of valve pilot stages for fluid control systems.

Commercially, stepper motors are used in floppy disk drives, flatbed scanners, computer printers, plotters and many more devices.

Crystal oscillators

Crystal oscillators are oscillators where the primary frequency determining element is a quartz crystal. Because of the inherent characteristics of the quartz crystal the crystal oscillator may be held to extreme accuracy of frequency stability. Temperature compensation may be applied to crystal oscillators to improve thermal stability of the crystal oscillator.

Crystal oscillators are usually, fixed frequency oscillators where stability and accuracy are the primary considerations. For example it is almost impossible to design a stable and accurate LC oscillator for the upper HF and higher frequencies without resorting to some sort of crystal control. Hence this is the reason for using crystal oscillators.

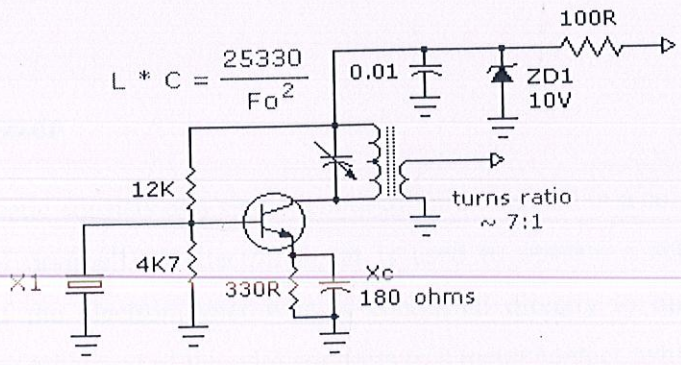


Fig 2.12: Schematic of a crystal oscillator

Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier, which can be configured for use as an on-chip oscillator. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven.

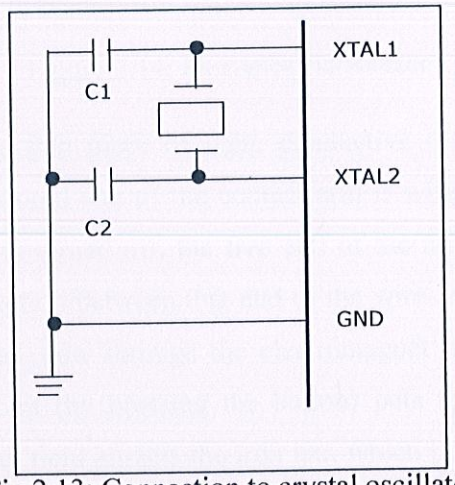


Fig 2.13: Connection to crystal oscillator

Note: C1, C2 = 30 pF +/- 10 pF for Crystals
= 40 pF +/- 10 pF for Ceramic Resonators

There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Piezoelectric Buzzer

An electromagnetic consists of a single length of wire wrapped in a coil. In a buzzer, the simplest sort of doorbell, an electromagnet is used to operate a self-interrupting circuit. One end of the electromagnet wire is connected directly to one end of the electrical circuit. The other end of the wire connects to a metal contact, which is adjacent to a moving contact arm.

Figure 2.14: Piezoelectric Buzzer

The contact arm is a thin piece of light, conductive metal, with a thin iron bar soldered onto it. The anchored end of the contact arm is wired to the electrical circuit. When the electromagnet is turned off, the free end of the arm resets again the contact point. This forms a connection between that end of the wire and the electrical circuit. In other words electricity can flow through the electromagnet when the circuit is closed. Closing the doorbell circuit (by pressing the button) puts this mechanism in motion. Initially, the electromagnet field attracts the iron bar, which pulls the contact arm off the stationery metal contact. This reestablishes the connection between the electromagnet and the circuit, and the current can flow through it again. The magnetic field draws the contact arm up, and the process repeats itself as long as you hold down the buzzer button. In this way, the electromagnet keeps shutting itself on and off.

The buzzing noise you hear is the sound of the rapidly moving arm hitting the magnet and the stationary contact dozen times a second.

CHAPTER 3

HARDWARE AND SOFTWARE

SECTION 3.1: HARDWARE

Component side

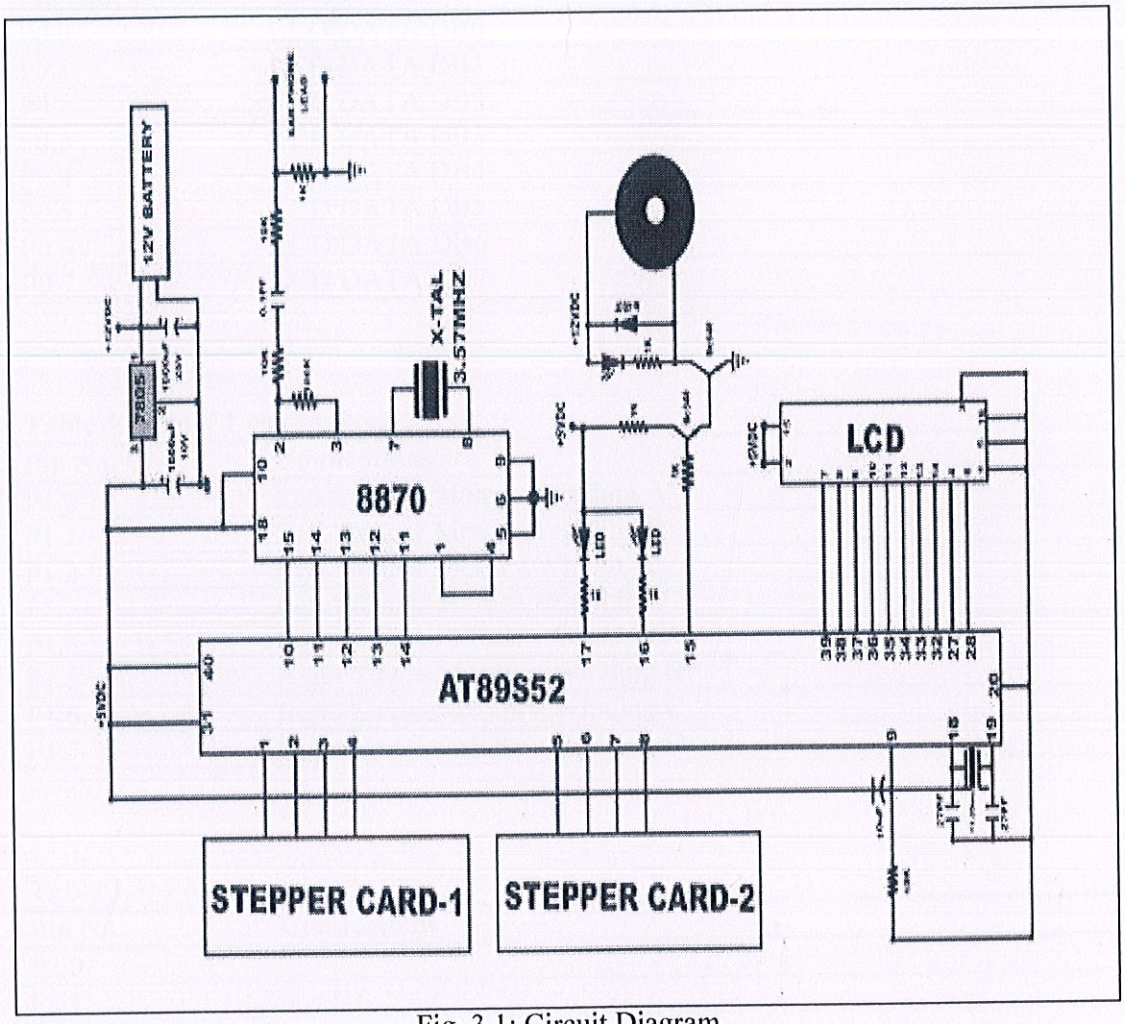


Fig. 3.1: Circuit Diagram

SECTION 3.2: PIN CONNECTIONS OF 89C52

Table 3.1: Port 0 connections

Pin No.	Connections
P0.0	LCD DATA DB0
P0.1	LCD DATA DB1
P0.2	LCD DATA DB2
P0.3	LCD DATA DB3
P0.4	LCD DATA DB4
P0.5	LCD DATA DB5
P0.6	LCD DATA DB6
P0.7	LCD DATA DB7

Table 3.2: Port 1 connections

Pin No.	Connections
P1.0	Left Stepper Motor - Winding A
P1.1	Left Stepper Motor - Winding B
P1.2	Left Stepper Motor - Winding C
P1.3	Left Stepper Motor - Winding D
P1.4	Right Stepper Motor - Winding A
P1.5	Right Stepper Motor - Winding B
P1.6	Right Stepper Motor - Winding C
P1.7	Right Stepper Motor - Winding D

Table 3.3: Port 2 connections

Pin No.	Connections
P2.0	--
P2.1	--
P2.2	--
P2.3	--
P2.4	--
P2.5	--
P2.6	RS, *register select*
P2.7	EN, *enable*

Table 3.4: Port 3 connections

Pin No.	Connections
P3.0	std pin of DTMF decoder. (IC 8870)
P3.1	data_8 of DTMF decoder.
P3.2	data_4 of DTMF decoder.
P3.3	data_2 of DTMF decoder.
P3.4	data_1 of DTMF decoder.
P3.5	buzzer
P3.6	led - left
P3.7	led - right

SECTION 3.3: SOFTWARE

Pseudo code for emergency shutdown procedure in MRTS:

In case of emergency situation, the passenger dials the emergency number; the following checks are performed first:

1. Check for std pin. It should be set to 1.
2. To get input as '1'; data_8 →0, data_4 →0, data_2 →0, data_1 →1.

   This will make the input BCD as 0001.
3. Stop flag should be set to 1.
4. This will halt the system by generating a delay.
5. At this instant, buzzer will blow, LCD will display the emergency situation.
6. System will reboot to normal process in 5 sec.

FLOWCHART FOR THE EMERGENCY SHUTDOWN PROCEDURE IN MRTS

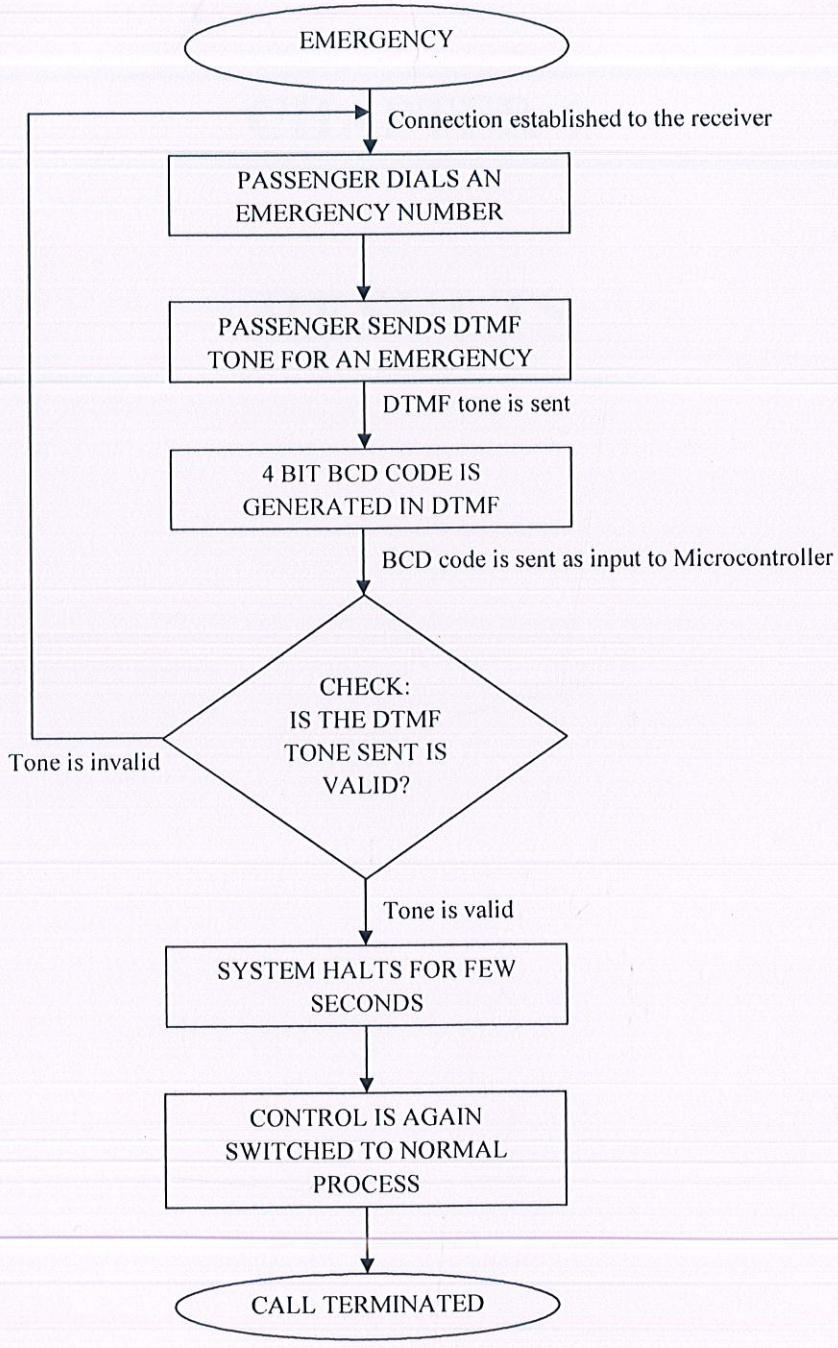


Fig 3.2: Flow chart of emergency shutdown procedure

CHAPTER 4

RESULTS

SECTION 4.1 OPERATING THE UNIT

To operate this unit, first of all concede main wire to the 12 volt battery.

When main wires are connected then LCD display will show a welcome screen. Now connect a hand free to Nokia mobile phone (simple phone), when we connect a hand free to the phone then hands free symbol is to appear on the screen, it means hand free is connected in proper manner.

Now change the setting of the phone.

Change profile in general mode.

Setting--- tone--- keypad sound--- high

Enhancement setting--- automatic answer--- on--- default

Profile general

Once the MRTS, is switched on, it will start following normal protocols as set.

Whenever we will dial the number of the mobile phone connected to the receiver, the call will be automatically connected in 5 seconds. Then the user will send a tone by pressing the required key from his/her mobile.. This will halt the system for 5 seconds. In our model we have used tone '1' as a DTMF tone to be sent for an emergency stop.

SECTION 4.2: SCREENSHOTS OF THE WORKING UNIT

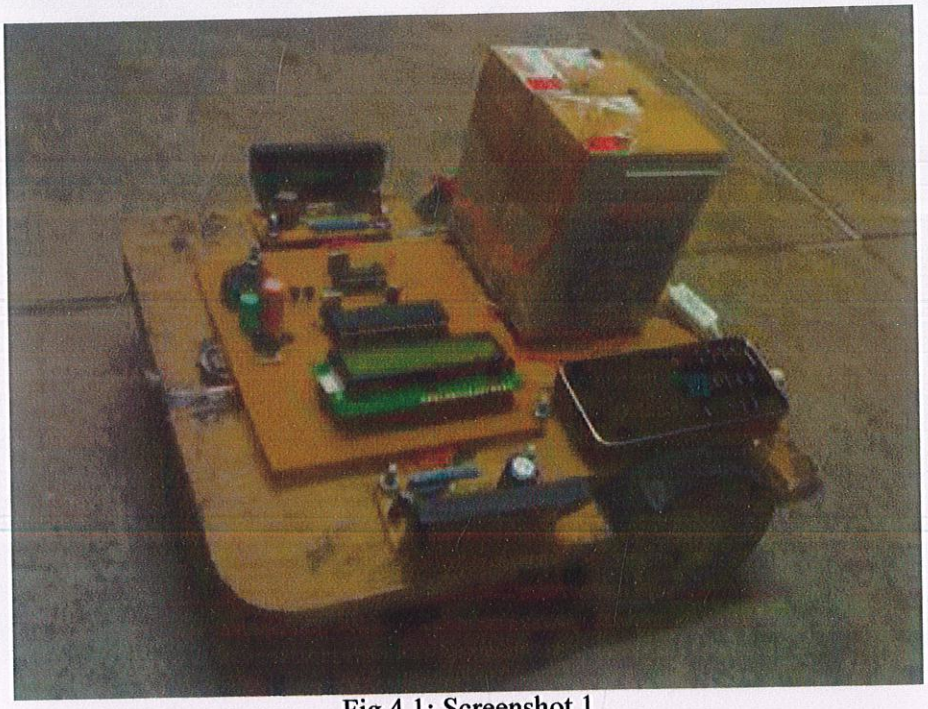


Fig 4.1: Screenshot 1

Fig 4.2: Screenshot 2

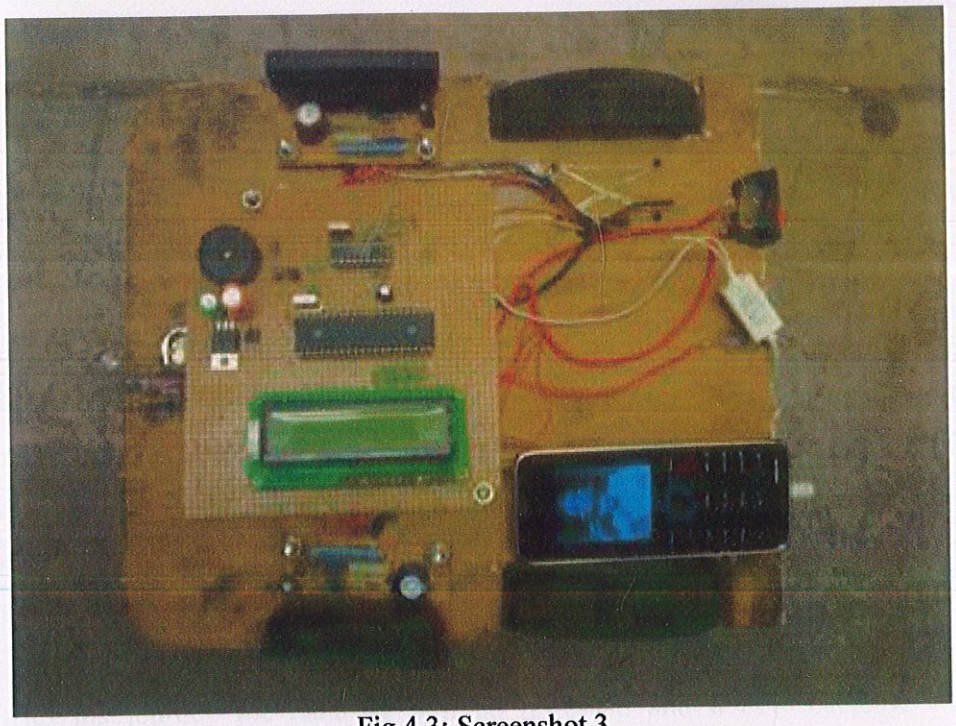


Fig 4.3: Screenshot 3

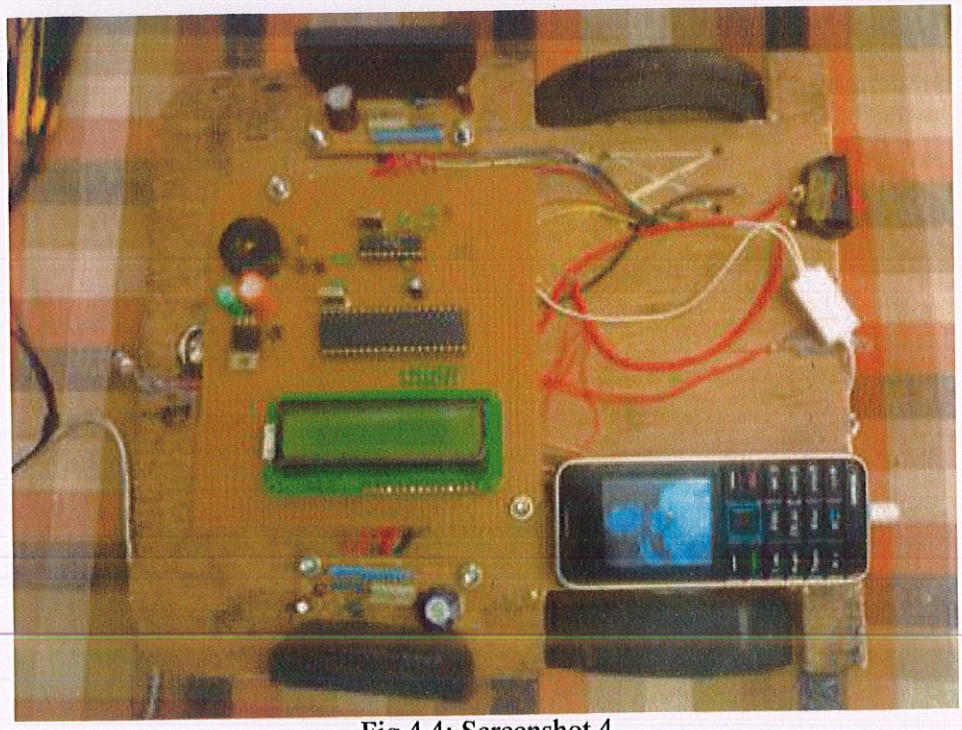


Fig 4.4: Screenshot 4

SECTION 4.3: FUTURE SCOPE

In our project, we have tried to implement the most basic model but we can incorporate this system with more add-ons to make it more practical in all respect. To make it more users friendly we may add 'Interactive Voice Response System' (IVRS) to make it simpler for all kind of users. For the efficient working of this system we may include database for all the passengers. Whenever, the passenger buys the ticket, a ticket reference number is allotted to that passenger. And this number will also be stored in the database. In case of emergency when a passenger connect to the receiver and connection is established successfully he will be asked to give the reference number through IVRS and then he can send emergency number to halt the system. By this a log will be created, whosoever uses this service can be easily traced or monitored. As soon as passenger completes his journey the database will be refreshed and a new database will be generated accordingly.

CONCLUSION

EMERGENCY SHUTDOWN SYSTEM application using DTMF tones in MRTS is one area that seems to have bright future prospects. In today's world where "ease of operation" always remains a primary concern about everything no matter what we are talking about, this system is fast becoming the need of the hour. In the implementation of our project we have seen that this system can be developed even by using simple components and applying basic knowledge of electronic components. Moreover by extending the technology applied we may be able to control all the functions of the wagon by sitting at a distant place and that too in large numbers. Hence proper implementation of the above stated technique will make operation of the transit system much easier and thus this technique is likely to attract more and more improvements in the near future.

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