DESIGN OF A LOW VOLTAGE, HIGH PERFORMANCE CURRENT FEEDBACK OPERATIONAL AMPLIFIER USING CMOS

Project Report submitted in partial fulfilment of the requirement for the degree of

Bachelor of Technology

in

Electronics and Communication Engineering

By

ADITYA BHANSALI - 061011

AYUSH GUPTA 061040

SWATI BHARGAVA 061131

under the Supervision of

Mrs. Shruti Jain

Jaypee University of Information Technology

Waknaghat, Solan - 173 234, Himachal Pradesh

Certificate

This is to certify that the project report entitled "**Design of a Low Voltage, High performance Current Feedback Operational Amplifier using CMOS**", submitted by **Aditya Bhansali, Ayush Gupta and Swati Bhargava** in partial fulfillment for the award of degree of Bachelor of Technology in Electronics and Communication Engineering to Jaypee University of Information Technology, Waknaghat, Solan has been carried out under my supervision.

Signataure

Date: 24th May '2010.

(Mrs. Shruti Jain)

(Lecturer)

Certified that this work has not been submitted partially or fully to any other University or Institute for the award of this or any other degree or diploma.

Signature

1. **(Aditya Bhansali)**
   Roll No.061011

Signature

2. **(Ayush Gupta)**
   Roll No.061040

Signature

3. **(Swati Bhargav)**
   Roll No.061131

ACKNOWLEDGEMENT

We would like to express our gratitude to **Prof. Dr. SUNIL BHOOSHAN, Head of Department, Electronics and Communication** for encouraging and inspiring us. Our deepest and most sincere thanks to **Mrs Shruti Jain , Lecturer, Department of Electronics and Communication,** our guide, who in spite of his busy schedule was able to spare time to help and guide us in doing this project by giving his expert guidance, encouragement and valuable suggestion.

A special thanks to **Mr. Kamlesh** who provided all possible help. His tireless efforts and willingness to clear all our doubts helped us immensely.

We would like to thank our parents for continuously raising our confidence and for their constant support.

(Aditya Bhansali) (Ayush Gupta) (Swati Bhargava)

Date: 24th May '2010.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF ABBREVIATIONS

BJT	Bipolar Junction Transistor.
CCII	Second generation Current Conveyor
CFA	Current Feedback Amplifier.
CFOA	Current Feedback Operational Amplifer.
CMRR	Common Mode Rejection Ratio.
CMOS	Complimentary Metal Oxide Semiconductor.
LHP	Left Half Plane.
MOSFET	Metal Oxide Semiconductor Field Effect Transistor.
NMOS	n-Channel Metal Oxide Semiconductor.
OP-AMP	Operational Amplifier.
OTA	Operational Transconductance Amplifier.
PMOS	p-Channel Metal Oxide Semiconductor.
PSPICE	Personal Computer Simulation Program with Integrated Circuit Emphasis.
RHP	Right Half Plane.
SLCL	Split Length Current mirror Load.
SNR	Signal to Noise Ratio.
VFA	Voltage Feedback Amplifier.
VLSI	Very Large Scale Integrated circuits.
VOA	Voltage mode Operational Amplifier.

ABSTRACT

The operational amplifier is an extremely efficient and versatile device. Its applications span the broad electronic industry filling requirements for signal conditioning, special transfer functions, analog instrumentation, analog computation, and special systems design. The analog assets of simplicity and precision characterize circuits utilizing operational amplifiers. In our project, we are designing a low-voltage CMOS current feedback operational amplifier (CFOA). This realization nearly allows rail-to-rail input/output operations. Also, it provides high driving current capabilities. The CFOA operates at supply voltages of ±0.75 V. The proposed CFOA circuit is thus a versatile building block for low voltage low power applications. PSpice simulation results for the proposed CFOA are given.

INTRODUCTION

An operational amplifier (op-amp) is a direct-coupled high-gain amplifier usually consisting of one or more differential amplifiers. The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for performing mathematical operations. Originally, the term, "Operational Amplifier," was used in the computing field to describe amplifiers that performed various mathematical operations.

Bipolar op-amps (μA 741) are capable of sourcing and syncing large load currents. This is facilitated by emitter follower output stage, which achieves very low output resistance. On the other hand, CMOS operational amplifiers are normally designed for particular applications where in only a few pico-farads of capacitive load are required to be driven. Therefore most of CMOS op-amps do not require a low resistance output stage. When op-amps input terminals are not connected directly to the IC's external terminals, they do not need electrostatic input devices also. CMOS is known for lower power consumption. But this advantage true only for slower amplifiers. As the bandwidth increases, a CMOS op-amp's current increases dramatically. Because of the exponentially increasing current required for CMOS to achieve high speeds, bipolar are typically better suited for high bandwidth applications.

It was found that the application of negative feedback around a high gain DC amplifier would produce a circuit with a precise gain characteristic that depended only on the feedback used. Negative feedback determines a high magnitude of voltage gain and positive feedback facilitates regenerative gain or oscillations. The voltage feedback (VF) operational amplifier is the most common type of op amp. The current feedback (CF) op amp is a trans impedance op amp and so has a different vocabulary associated with it. In a Voltage Feedback op amp, when negative feedback is applied, the action of the op amp is to drive the error voltage to zero; thus the name voltage feedback. In a Current Feedback op amp, when negative feedback is applied, the action of the op amp is to drive the error current to zero; thus the name current feedback. The current feedback amplifier (CFA) has the same ideal closed-loop equations as the voltage feedback amplifier (VFA), but the CFA offers various improvements when compared with the VFA, which are discussed in a later section.

However, despite the required use of feedback in the internal circuitry, the design of operational amplifiers is often presented and completed without a useful control framework. Op-amps require a deliberately designed frequency response to ensure stability and satisfactory transient performance in end user applications. Internally compensated op-amps have a fixed transfer function set by the manufacturer. Externally compensated op-amps allow the end user to select the compensation network that determines the transfer function of the op amp. The two-stage op-amps have traditionally been compensated using the Miller (or Direct) compensation technique. The indirect compensation technique using split-length transistors can also be used to compensate op-amps (as discussed in chapter 3).

In the last section, a novel low voltage CMOS current-feedback operational amplifier is presented. The CFOA is capable of operating under a minimum supply voltage ($|V_{Tp}|+V_{Tn}+V_{DS,sat}$) and with reduced power dissipation. The new circuit includes a class AB output stage exhibiting high current drive capability and good power conversion efficiency. A rail-to-rail input and output voltage operation is also nearly achieved.

CHAPTER 1

OPERATIONAL AMPLIFIER

1.1 INTRODUCTION

An operational amplifier, which is often called an op-amp, is a DC-coupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output. An op-amp produces an output voltage that is typically millions of times larger than the voltage difference between its input terminals [1]. μa 741 is one of the most commonly used bipolar operational amplifiers IC today. Figure 1.1 shows the circuit symbol for an operational amplifier.

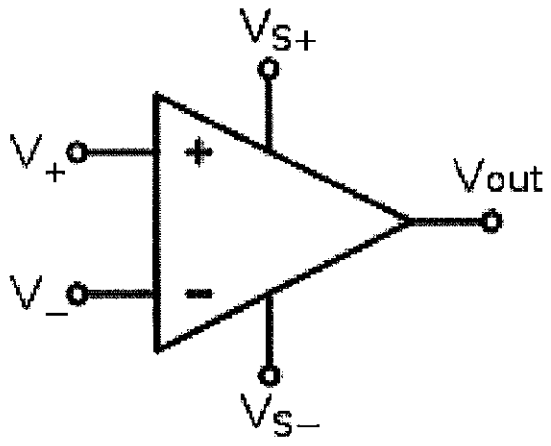


Figure 1.1: The circuit symbol for an op-amp

- V_+ : non-inverting input
- V_- : inverting input
- V_{ought} : output voltage
- V_{S+} : positive supply voltage
- V_{S-} : negative supply voltage

1.2 IDEAL OP-AMP

For any input voltages, an ideal op-amp has the following properties [1]:

- Infinite open-loop gain
- Infinite bandwidth
- Infinite input impedance
- Zero input current
- Zero input offset voltage
- Infinite slew rate and power bandwidth
- Zero output impedance
- Zero noise
- Infinite Common-mode rejection ratio (CMRR)
- Infinite power supply rejection ratio for both power supply rails

Op-amps consist of three basic stages:

1. Differential amplifier – provides low noise amplification, high input impedance, usually a differential output.
2. Voltage amplifier – provides high voltage gain, and usually single-ended output.
3. Output amplifier – provides high current driving capability, low output impedance, current limiting and short circuit protection circuitry.

1.3 WORKING OF μA741

μA741 is one of the most commonly used bipolar op-amp. Figure 1.2 is the internal circuit of μA741.

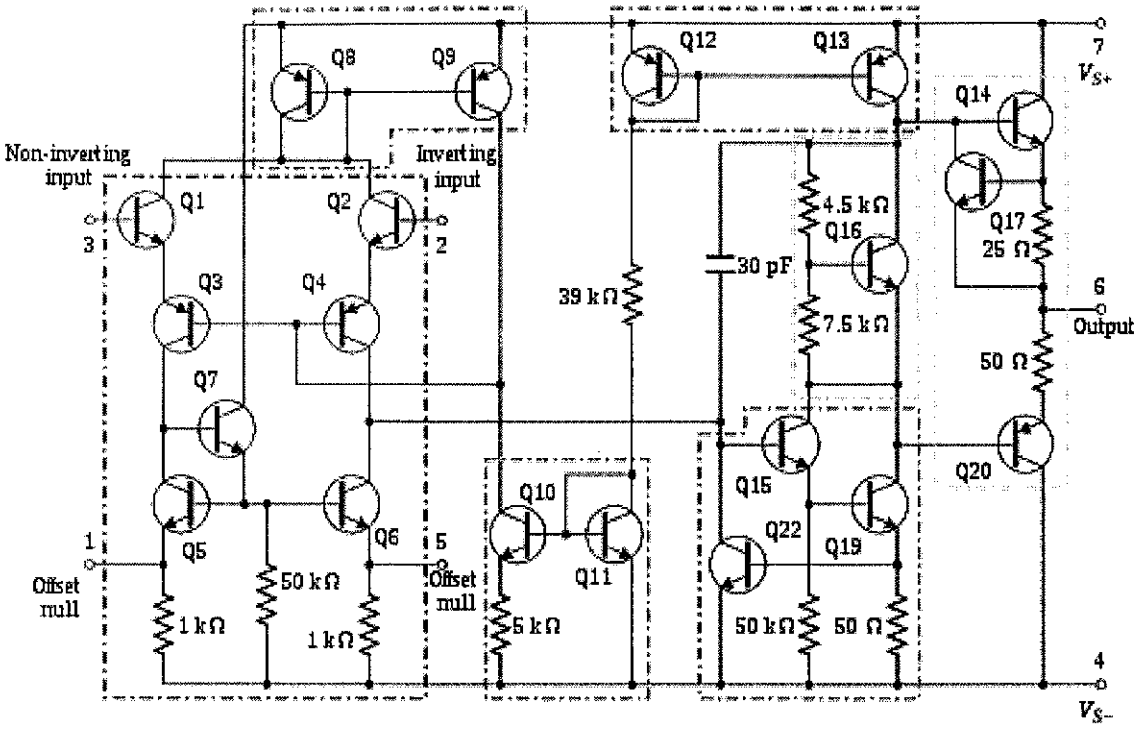


Figure 1.2: Internal circuit of μA741

1.3.1. Input stage

1.3.1.1. Constant-current stabilization system

The input stage DC conditions are stabilized by a high-gain negative feedback system whose main parts are the two current mirrors on the left of the figure 1.2, consisting of *Q*8 *Q*9 and *Q*10 *Q*11. The main purpose of this negative feedback system is to supply the differential input stage with a stable constant current.

The current through the 39 co resistor acts as a current reference for the other bias currents. The voltage across the resistor is equal to the voltage across the supply rails (V_{S+} - V_{S-}) minus two transistor diode drops (i.e., from *Q11* and *Q12*), and so the current has value $I_{ref} = (V_{S+} - V_{S-} - 2V_{be}) / (39k\Omega)$. The current mirror built by *Q10, Q11*, and the *5 kΩ* resistor produces a very small fraction of I_{ref} at the *Q*10 collector. This small constant current through *Q10's* collector supplies the base currents for *Q*3

and $Q4$ as well as the $Q9$ collector current. The $Q8/Q9$ current mirror tries to make $Q9$'s collector current the same as the $Q3$ and $Q4$ collector currents. Thus $Q3$ and $Q4$'s combined base currents will be a small fraction of the already small $Q10$ current.

So, if the input stage current increases for any reason, the $Q8/Q9$ current mirror will draw current away from the bases of $Q3$ and $Q4$, which reduces the input stage current, and vice versa. The feedback loop also isolates the rest of the circuit from common-mode signals by making the base voltage of $Q3/Q4$ follow tightly $2V_{be}$ below the higher of the two input voltages [1].

1.3.1.2. Differential amplifier

Differential amplifier consists of $Q1$ $Q2$ $Q3$ $Q4$ $Q5$ $Q6$ and $Q7$ transistors. $Q1$ and $Q2$ are input emitter followers and together with the common base pair $Q3$ and $Q4$ form the differential input stage. In addition, $Q3$ and $Q4$ also act as level shifters and provide voltage gain to drive the class A amplifier. They also help to increase the reverse V_{be} rating on the input transistors. The differential amplifier formed by $Q1$–$Q4$ drives a current mirror active load formed by transistors $Q5$–$Q7$.$Q7$ increases the accuracy of the current mirror by decreasing the amount of signal current required from $Q3$ to drive the bases of $Q5$ and $Q6$. The signal current of $Q3$ is the input to the current mirror while the output of the mirror (the collector of $Q6$) is connected to the collector of $Q4$. Here, the signal currents of $Q3$ and $Q4$ are summed. For differential input signals, the signal currents of $Q3$ and $Q4$ are equal and opposite. Thus, the sum is twice the individual signal currents. This completes the differential to single ended conversion. The open circuit signal voltage appearing at this point is given by the product of the summed signal currents and the paralleled collector resistances of $Q4$ and $Q6$. Since the collectors of $Q4$ and $Q6$ appear as high resistances to the signal current, the open circuit voltage gain of this stage is very high. It should be noted that the base current at the inputs is not zero and the effective (differential) input impedance of a μA741 is about 2 MΩ.

The "offset null" pins may be used to place external resistors in parallel with the two 1 kΩ resistors (typically in the form of the two ends of a potentiometer) to adjust the balancing of the $Q5/Q6$ current mirror and thus indirectly control the output of the op-amp when zero signal is applied between the inputs [1].

1.3.2. Class A gain stage

Class A gain stage consists of $Q15$ $Q19$ $Q22$ configured in the form of class A amplifier. The top-right current mirror $Q12/Q13$ supplies this stage by a constant current load, via the collector of $Q13$ that is largely independent of the output voltage. The stage consists of two NPN transistors in a Darlington configuration and uses the output side of a current mirror as its collector load to achieve high gain. The 30 pF capacitor provides frequency selective negative feedback around the class A gain stage as a means of frequency compensation to stabilise the amplifier in feedback configurations. This technique is called Miller compensation and functions in a similar manner to an op-amp integrator circuit. It is also known as 'dominant pole compensation' because it introduces a dominant pole (one which masks the effects of other poles) into the open loop frequency response. This pole can be as low as 10 Hz in a μA741 amplifier and it introduces a −3 dB loss into the open loop response at this frequency. This internal compensation is provided to achieve unconditional stability of the amplifier in negative feedback configurations where the feedback network is non-reactive and the closed loop gain is unity or higher. Hence, the use of the operational amplifier is simplified because no external compensation is required for unity gain stability; amplifiers without this internal compensation may require external compensation or closed loop gains significantly higher than unity [1].

1.3.3. Output stage

$Q16$ acts as a voltage level shifter or rubber diode (i.e., a V_{BE} multiplier); a type of voltage source. In the circuit as shown, $Q16$ provides a constant voltage drop between its collector and emitter regardless of the current through the circuit. If the base current to the transistor is assumed to be zero, and the voltage between base and emitter (and across the 7.5 kΩ resistor) is 0.625 V (a typical value for a BJT in the active region), then the current through the 4.5 kΩ resistor will be the same as that through the 7.5 kΩ, and will produce a voltage of 0.375 V across it. This keeps the voltage across the transistor, and the two resistors at 0.625 + 0.375 = 1 V. This serves to bias the two output transistors slightly into conduction reducing crossover distortion.

The output stage is a Class AB push-pull emitter follower ($Q14$, $Q20$) amplifier with the bias set by the V_{be} multiplier voltage source $Q16$ and its base resistors. This

stage is effectively driven by the collectors of $Q13$ and $Q19$. Variations in the bias with temperature, or between parts with the same type number, are common so crossover distortion and quiescent current may be subject to significant variation. The output range of the amplifier is about one volt less than the supply voltage, owing in part to V_{be} of the output transistors $Q14$ and $Q20$. The 25Ω resistor in the output stage acts as a current sense to provide the output current-limiting function which limits the current in the emitter follower $Q14$ to about 25mA for the μA741. Current limiting for the negative output is done by sensing the voltage across $Q19$'s emitter resistor and using this to reduce the drive into $Q15$'s base. Later versions of this amplifier schematic may show a slightly different method of output current limiting. The output resistance is not zero, as it would be in an ideal op-amp, but with negative feedback it approaches zero at low frequencies [1].

1.4. CONFIGURATIONS OF μA741

There are two types of configuration of μA741:

1. Inverting mode
2. Non-Inverting mode

1.4.1. Inverting Mode

The positive end of the input voltage V_{in} is connected through a resistor R_1 to the inverting input pin (-) on the op-amp (the negative end of V_{in} is connected to ground) shown in Figure 1.3. The non-inverting input pin (+) is connected to ground [2].

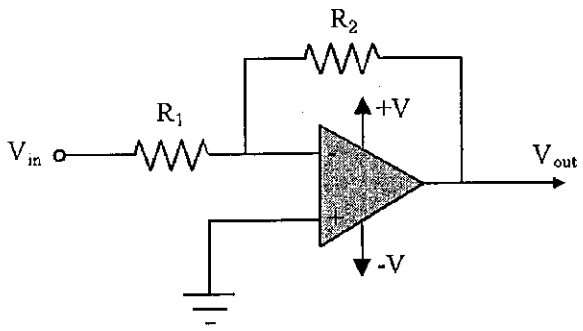


Figure 1.3: Inverting Amplifier.

The **gain** A_f of an amplifier is defined as the ratio of the output to input voltages.

$$A_f = \frac{V_{out}}{V_{in}}$$

When the input voltage is a DC signal, V_{out} and V_{in} in the above equation represent the actual values of the two voltages. When the input is a sinusoidal AC signal, the output will also be a sinusoidal AC signal. In this case, V_{out} and V_{in} represent the magnitudes of the input and output signals.

For the above circuit, we can assume that the same current flows through both resistors because of the extremely high input impedance and that the voltage at the inverting pin is nearly the same as ground (virtual short). Thus

$$V_{out} = -\frac{R_2}{R_1} V_{in}$$

so that the gain is:

$$A_f = -\frac{R_f}{R_1}$$

When the input and output are sinusoidal AC signals, the negative sign in the above equation indicates a 180-degree phase shift between the output and input.

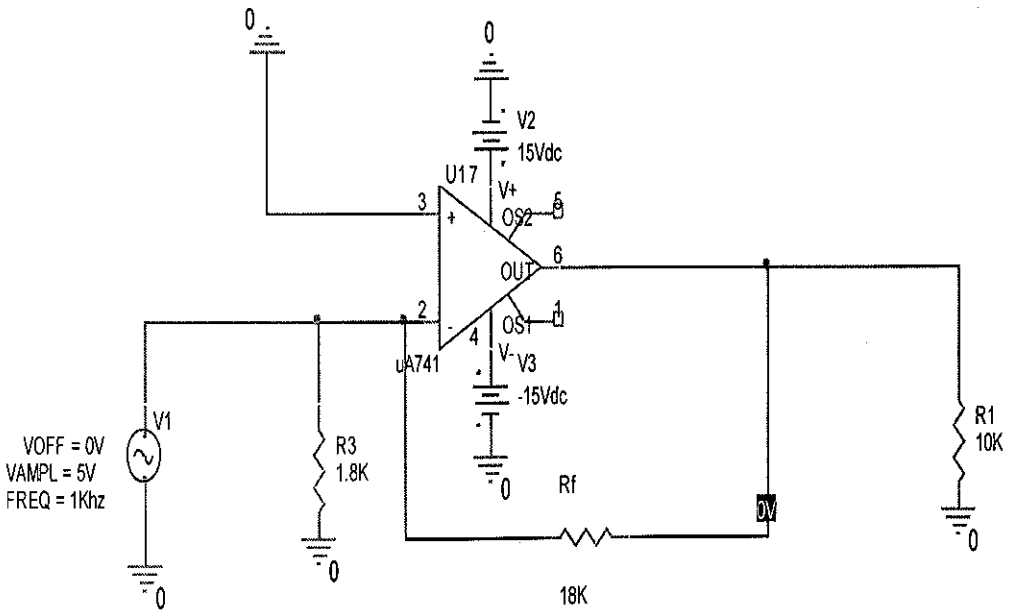


Figure 1.4 : µA741 in inverting configuration

Simulation result:

As can be seen in the Pspice simulation on OrCad Capture given below (Figure 1.5), when an input of 5V, 1kHz is applied to the circuit (Figure 1.4) the output is inverted and amplified.

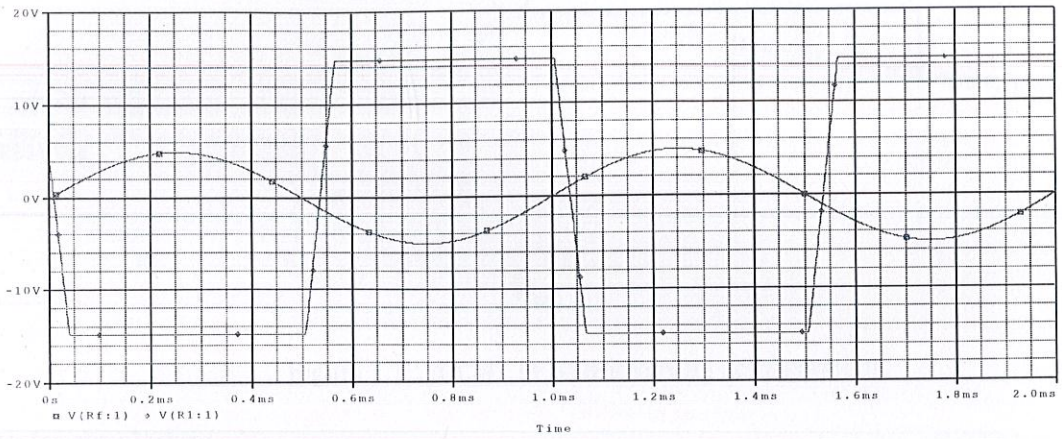


Figure 1.5 : Pspice simulation for μA741 in inverting configuration

1.4.2 Non-inverting Mode

The circuit below shows a simple design for a **non-inverting amplifier**. The input voltage V_{in} is applied directly to the non-inverting terminal of the op-amp shown in Figure 1.6. Negative feedback is provided by the two external resistors R_1 and R_2 which form a voltage divider and apply a fixed fraction of the output voltage to the inverting input terminal of the op-amp [2].

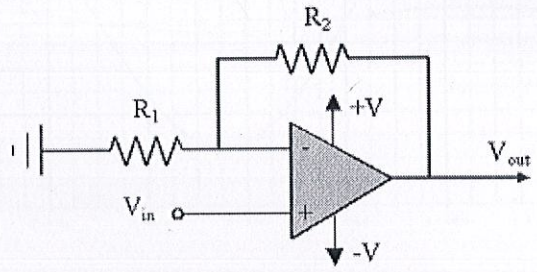


Figure 1.6: Non inverting Amplifier

The gain of the amplifier is determined by the external resistors R_1 and R_2 according to the equation:

$$A_f = 1 + \frac{R_2}{R_1}$$

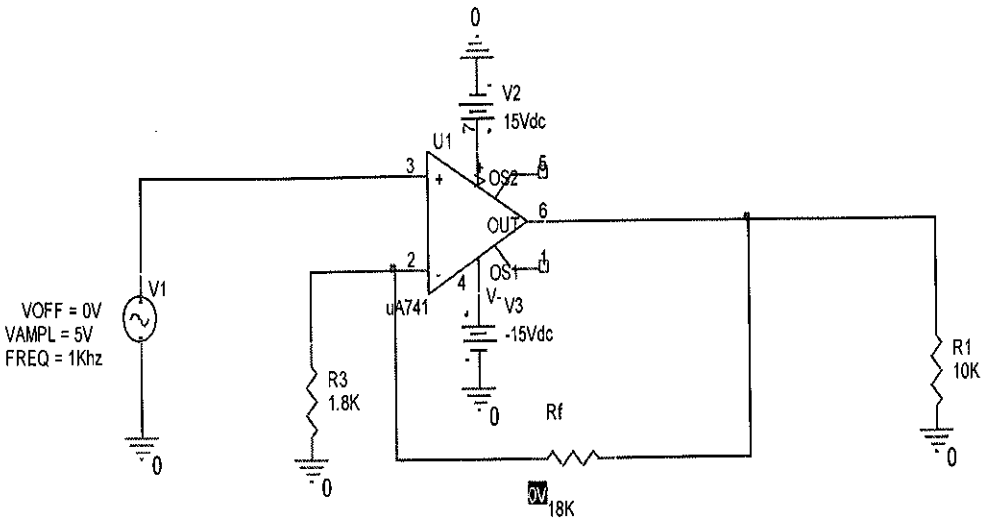


Figure 1.7 : μA741 in Non-inverting configuration

Pspice simulation:

The results of Pspice simulation using OrCad Capture (Figure 1.8) shows that when an input of 5V, 1 kHz is applied to the circuit (Figure 1.7) the output is not inverted, but amplified.

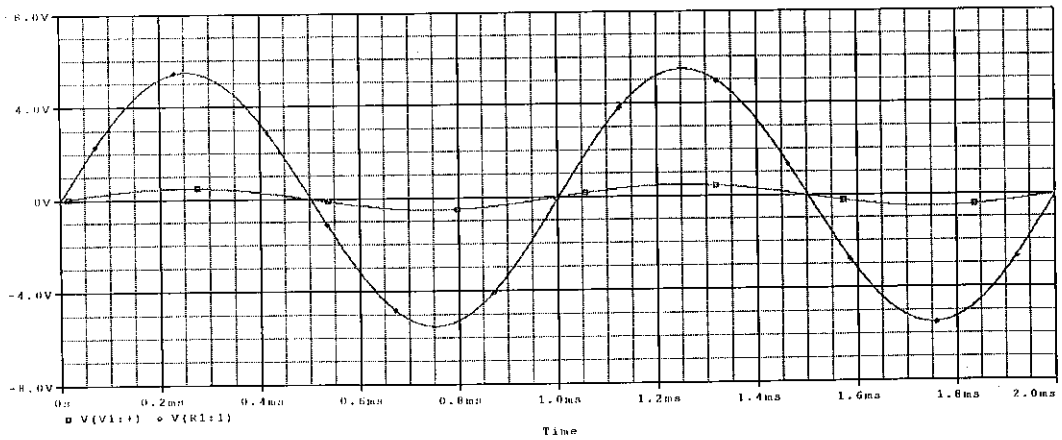


Figure 1.8: Pspice simulation for μA741 in non-inverting configuration

CHAPTER 2

FEEDBACKS IN OPERATIONAL AMPLIFIERS

2.1. INTRODUCTION

There are two types of feedback in op amps:

1. Voltage Feedback
2. Current Feedback

The voltage feedback operational amplifier (VFA) is the most common type of op amp. The less well known current feedback op-amp (CFA). The CFA op amp is a trans impedance op-amp and so has a different vocabulary associated with it.

In a Voltage Feedback op amp, when negative feedback is applied, the action of the op amp is to drive the error voltage to zero; thus the name voltage feedback. Where as in a Current Feedback op amp, when negative feedback is applied, the action of the op-amp is to drive the error current to zero; thus the name current feedback.

2.2. ADVANTAGES OF CFA OVER VFA

The current feedback amplifier (CFA) has the same ideal closed-loop equations as the voltage feedback amplifier (VFA), but the CFA offers three improvements when compared with the VFA. Generally, CFA's cost less per megahertz of bandwidth, and they don't have the constant gain-bandwidth or slew rate limitations of the VFA. As a result, the CFA's open-loop gain doesn't roll off until much higher frequencies. That typically makes the CFA the amplifier of choice for high-frequency op-amp circuits. On top of that, the input circuit of the CFA supplies current to the output under transient conditions, and this extra current increases the slew rate. In fact, the CFA often is the best circuit available with its cost-effective combination of high gain, high performance, and low I_{CC}. Substituting a CFA for a VFA in the design or production stages will result in better performance and lower cost.

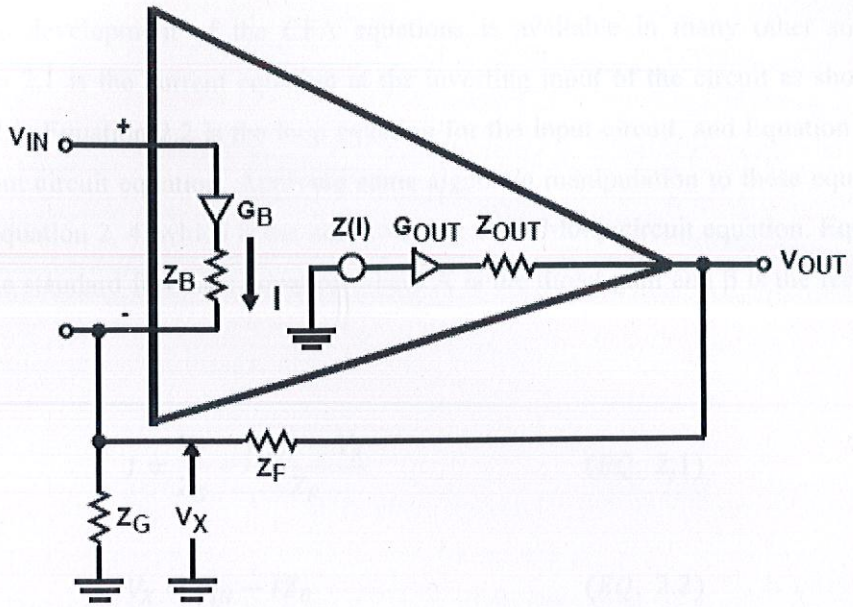


Figure 2.1: Model of Current Feedback op-amp (CFA)

In a CFA model, it can be seen that the non-inverting input is connected to the input of a unity gain, which usually takes the form of sophisticated emitter follower circuit, and is modelled by G_B and Z_B . Because the non-inverting input is actually the input of a buffer, it's a high-impedance input. Also, because this buffer's output connects to the inverting input, CFAs have lower inverting-input impedance, Z_B. The inverting-input impedance will be very low (as low as 10Ω). Therefore, the open-loop inverting input impedance is about equal to (Z_G+ Z_B), which ranges from 1kΩ to 10Ω. G_B possesses a bandwidth greater than the remainder of the amplifier, coupled with a gain that is very close to one, so it is neglected in the calculations. On the other hand, Z_B is a function of frequency and has a secondary effect on stability, so it must be included in the calculations. The current *I*, flowing through the inverting input generates a voltage that is equal to the current times the trans impedance, *Z*. This voltage is modelled by the output voltage source, *Z(I)*. This voltage becomes the output voltage after passing through the output buffer, which is modelled by G_{OUT} and Z_{OUT}. Again, G_{OUT} will be neglected for the same reasons that G_B was neglected. Z_{OUT} is a function of frequency and can have an effect at higher frequencies under capacitive-load conditions, but it will be neglected because these effects are easily calculated and are minimal under normal loading.

An abbreviated development of the non-inverting circuit equations is given here; the complete development of the CFA equations is available in many other sources. Equation 2.1 is the current equation at the inverting input of the circuit as shown in Figure 2.1. Equation 2.2 is the loop equation for the input circuit, and Equation 2.3 is the output circuit equation. Applying some algebraic manipulation to these equations yields Equation 2. 4, which is the non-inverting closed-loop circuit equation. Equation 2.5 is the standard feedback equation where A is the direct gain and β is the feedback factor.

$$I = \frac{V_X}{Z_G} - \frac{V_{OUT} - V_X}{Z_F} \qquad (EQ.\ 2.1)$$

$$V_X = V_{IN} - IZ_B \qquad (EQ.\ 2.2)$$

$$V_{OUT} = IZ \qquad (EQ.\ 2.3)$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{Z(1+\frac{Z_F}{Z_G})}{Z_F(1+Z_B/Z_F||Z_G)}}{1+\dfrac{Z}{Z_F(1+Z_B/Z_F||Z_G)}} \qquad (EQ.\ 2.4)$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1+A\beta} \qquad (EQ.\ 2.5)$$

If A is so large that the product $A\beta$ is much greater than one, then the ideal closed-loop gain is equal to $1/\beta$. Also, the stability of Equation 2.5 is determined by its denominator, or, in other words, by $A\beta$. As the trans impedance, Z, in Equation 4 approaches infinity, the ideal closed-loop gain becomes $G = 1 + Z_F/Z_G$, which is identical to the VFA non-inverting ideal closed-loop gain. This presents a paradox: If the ideal closed-loop gains are identical, then how does the CFA become independent from the constant-gain-bandwidth limitation of the VFA? If the input buffer were perfect, the quantity Z_B in Equation 2.4 would be zero, and Equation 2.4 becomes Equation 2.6 as shown. A close inspection of Equation 2.6 indicates that the CFA has the same ideal closed-loop gain as the trans impedance gets very large, but Z_G is eliminated from the denominator when Z_B is zero. The stability is determined by the

denominator, and the denominator is independent of Z_G. Thus, the stability is independent of the closed-loop gain, and the constant-gain-bandwidth limitation doesn't exist.

The equation for the inverting configuration is developed with the same techniques used to develop the non-inverting equation and is given as Equation 2.7. Notice that the denominators of Equations 2.4 and Equation 2.7 are identical. This is because stability depends solely on the loop gain, $A\beta$, given in Equation 2.8, and not on the placement of the inputs.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{Z(1+\frac{Z_F}{Z_G})}{Z_F}}{1+\frac{Z}{Z_F}} \qquad (EQ.\ 2.6)$$

The CFA can easily replace the VFA in most high-frequency applications with better performance and lower cost. There are just a few salient points to be aware of during the replacement, remember that the CFA must have a feedback resistor, thus a CFA can't be substituted directly for a VFA in unity-gain applications in which the output is shorted to the inverting input ($R_F = 0$).

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{Z}{Z_F(1+Z_B/Z_F||Z_G)}}{1+\frac{Z}{Z_F(1+Z_B/Z_F||Z_G)}} \qquad (EQ.\ 2.7)$$

$$A\beta = \frac{Z}{Z_F(1+Z_B/Z_F||Z_G)} \qquad (EQ.2.8)$$

CHAPTER 3

LOW VOLTAGE AND HIGH PERFORMANCE TECHNIQUES

3.1. HIGH SPEED CMOS OP-AMP DESIGN TECHNIQUE USING NEGATIVE MILLER CAPACITANCE

With developments in deep sub micrometer CMOS processes, the available dynamic range in Operational Amplifiers is reduced due to lower power supply voltages. This loss in dynamic range tightens the noise budget. A larger load capacitor should therefore be used to reduce the circuit noise, and hence increase the Signal-to-Noise Ratio (SNR), which in turn decreases the bandwidth of the amplifier. With ever increasing data rates, many mixed-signal applications, however, require fast settling Op-Amps. Op-Amp design has therefore become exceedingly difficult for broadband circuits while maintaining adequate SNR performance. Techniques for increasing the bandwidth of CMOS Op-Amps are needed to accommodate high speed operation with low noise performance. In this section, a high-speed CMOS Op-Amp design technique is described. The Op-Amp is comprised of an Operational trans conductance Amplifier (OTA) and a buffer, where the OTA is compensated with a capacitor connected between the input and output of the buffer. This arrangement simultaneously improves the unity gain frequency (the bandwidth) and phase margin of the Op-Amp. In a conventional circuit, these two parameters are inversely related to each other (i.e., an increase in one parameter produces a decrease in the other parameter), imposing a tradeoff between speed and stability.

A standard method for designing CMOS Op-Amps is to utilize an OTA followed by an output buffer, as shown in Figure 3.1. Note that all internal nodes in the OTA are low impedance nodes, except for the input and output nodes. A buffer is, therefore, used to isolate the OTA from the load. In Op-Amp applications, the load may be resistive, capacitive, or a combination, whereas OTAs typically drive relatively small capacitive loads. Since the load is connected at the output of the Op-Amp, which is a low impedance node, the load capacitance has little effect on the phase margin of the amplifier. The OTA should, therefore, be internally compensated; otherwise the overall amplifier would exhibit poor stability. In conventional Op-Amps, the OTA is

compensated with a capacitor C_C connected from the output of the OTA to ground.

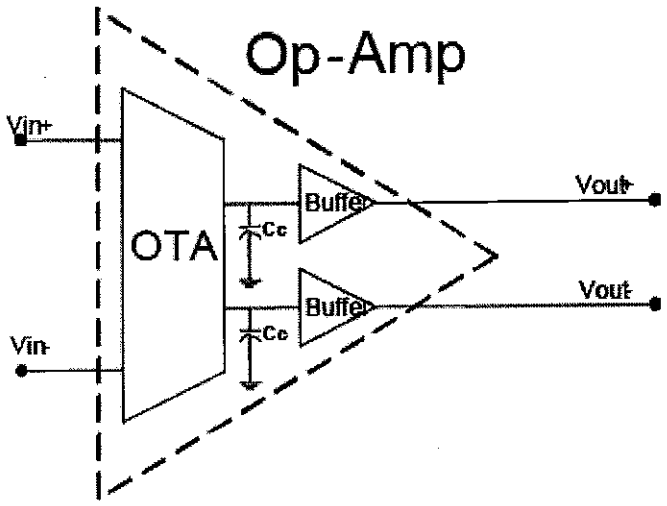


Figure 3.1: Conventional op-amp circuit structure

The high speed Op-Amp method in this section is illustrated in Figure 3.2. Unlike a conventional circuit structure, the OTA is compensated using a Miller capacitance connected between the input and output of the buffer. Assuming that the Op-Amp drives a parallel combination of a capacitor C_L and a resistor R_L, the effective capacitance seen at the input and output of the buffer is

$$C_{eff,in} = C_C(1 - A) \; and \; C_{eff,out} = C_C(1 - 1/A) \qquad EQ.3.1$$

In (EQ. 3.1), A represents the gain of the buffer. Note that since the gain of the buffer is always smaller than one, the effective capacitance seen at the output of the Op-Amp is smaller than the original load capacitance. This effect pushes the first non-dominant pole (i.e., the pole closest to the origin after the dominant pole) to a higher frequency. The location of the dominant pole, however, remains unaltered (to a first order approximation). This argument suggests that in the proposed compensation scheme (see Figure 3.2), both the unity gain frequency and phase margin are improved as compared to a conventional circuit structure. To avoid a negative effective capacitance at the output of the Op-Amp, however, the compensation capacitance must satisfy the following relation,

$$C_C < C_L\left(\frac{A}{1 - A}\right) \qquad EQ.3.2$$

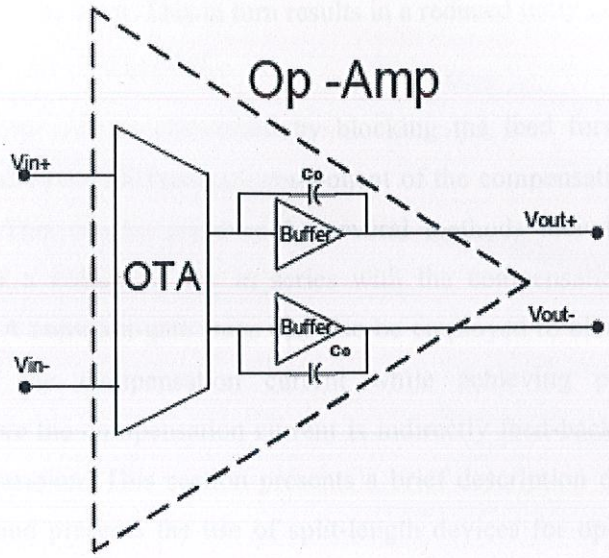


Figure 3.2: High speed Op-amp circuit structure

Note that Miller capacitance compensation is extensively used intro-stage Op-Amps and other applications. Generally speaking, in these applications, the Miller capacitance is connected around an amplifier with a negative high gain (*i.e.*, A<<-1). The reason for this negative gain is to establish negative feedback. In the approach presented above, the gain of the buffer is positive (but smaller than one). As long as the gain is smaller than one, the positive feedback does not necessarily result in a completely unstable system.

3.2. INDIRECT COMPENSATION TECHNIQUE FOR LOW-VOLTAGE CMOS OP-AMPS

3.2.1. INTRODUCTION

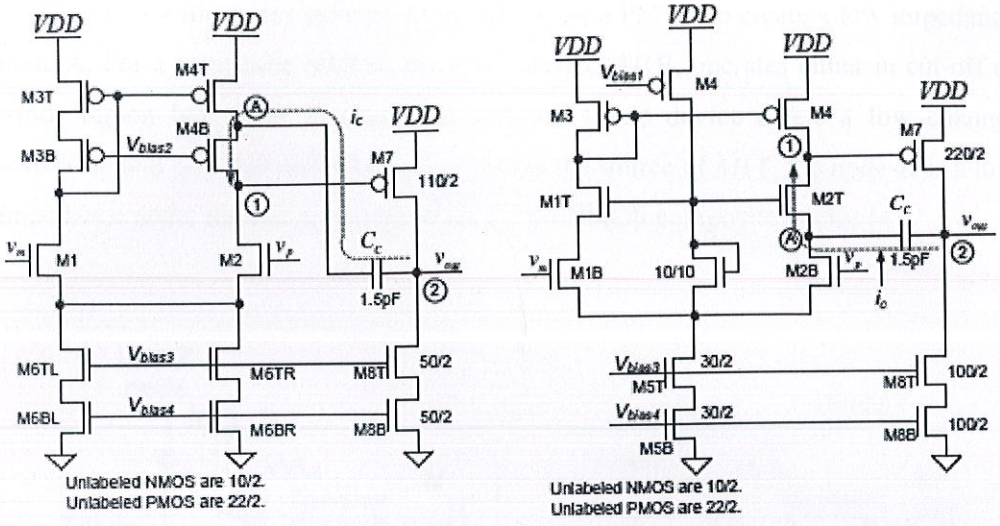
Two-stage op-amps have been the amplifier topologies of choice in analog system design due to their simple frequency compensation and relaxed stability criterions. The two-stage op-amps have traditionally been compensated using the Miller (or Direct) compensation technique. Miller compensation achieves dominant pole compensation by pole splitting due to capacitance multiplication effect. However, the compensation capacitance (C_C) connected between the outputs of the first and second gain stages, leads to a right-half plane (RHP) zero. The RHP zero, located at $z_{n1} = g_{m2}/C_c$ in the s-plane, pulls down the phase margin of the op-amp and requires a larger capacitance

to compensate the op-amp. This in turn results in a reduced unity gain frequency of the op-amp given by $f_{un} = g_{m1}/2\pi C_c$. .

The RHP zero can be eliminated by blocking the feed forward compensation current, while allowing the feedback component of the compensation current to attain pole splitting. This can be achieved by several methods including a zero nulling resistor (R_Z) or a voltage buffer in series with the compensation capacitor in the feedback path. A common-gate stage can also be employed to block the feed forward component of the compensation current while achieving pole-splitting. Such techniques where the compensation current is indirectly feed-back are categorized as indirect compensation. This section presents a brief description of indirect feedback compensation and presents the use of split-length devices for op-amp compensation while operating at low-V_{DD}.

3.2.2. INDIRECT FEEDBACK COMPENSATION OF OP-AMPS

The class of amplifier compensation in which the compensation current is fed back indirectly from the output to the internal high impedance node is defined as Indirect Feedback Frequency Compensation or simply, indirect compensation. Here, the compensation capacitor is connected to an internal low impedance node in the first stage, which allows indirect feedback of the compensation current from the output node to the internal high-impedance node i.e. the output of the first stage. The dominant pole location for the indirect compensated op-amp is same as in Miller compensation. However, instead of a RHP zero we now have a LHP zero located at $z_1 = g_m/(C_C + C_A)$, where is the trans conductance of the common-gate device and C_A is the capacitance attached to the low-impedance node A. The non-dominant pole location is given by $p_2 = -g_{m2}/(C_1 C_L)$. Also there exists a third parasitic pole arising due to the loading of the low impedance node-A.



(a) Cascoded current mirror load (b) Cascoded differential pair

Figure 3.3: Indirect compensated two-stage op-amps using cascode common gate device.

The compensation capacitor, Cc, in each of the op-amps is connected to the the low impedance node A. We can discern that when using indirect compensation, the second pole, p_2, is pushed further away from the dominant pole, p_1, by a factor of approximately C_C/C_1. Hence, pole splitting can be achieved with a lower value of the compensation capacitor C_C and/or with a lower value of g_{m2}.

This results in a significantly higher unity-gain frequency attainable by the op-amp. Also the LHP zero adds to the phase in the vicinity of the unity gain frequency, fun, and improves the phase margin. Figure 3.3 shows two-stage op-amp topologies where indirect compensation is achieved by using the "embedded' common-gate device in the cascode structure.

3.2.3. INDIRECT COMPENSATION USING SPLIT-LENGTH COMPOSITE TRANSISTORS

Indirect-compensated two-stage op-amps can be designed by employing the internal low impedance nodes available in a cascode topology to feedback the compensation current. However, with continual scaling of supply voltage (V_{DD}) cascoding may no longer be an option in the sub-100nm CMOS processes. A suitable technique for low V_{DD} design which employs a split-length composite transistor for indirect compensation is analyzed in this section.

Figure 3.4 illustrates splitting of an NMOS or a PMOS to create a low impedance node-A. For a composite NMOS, the lower device, $M1B$, operates either in cut-off or triode region but never in saturation. Since a triode device offers a low channel resistance and also that node-A is connected to the source of $M1T$, the node-A is a low impedance node. Similar argument holds for the PMOS composite device [4].

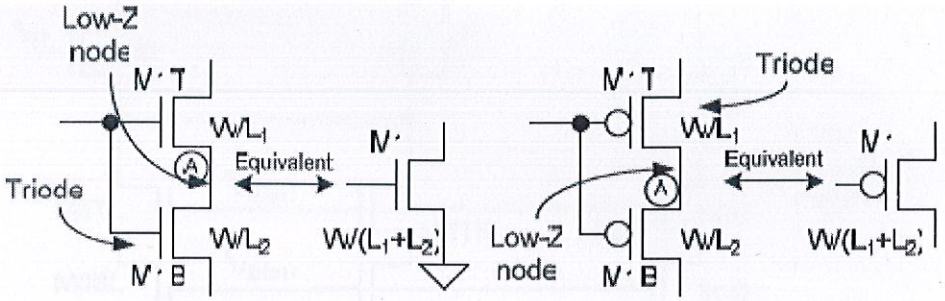


Figure 3.4: Illustration of the split-length composite NMOS and PMOS devices

Split length current mirror load (SLCL)

Figure 3.5 exhibits a two-stage op-amp with a split-length current mirror load (SLCL) topology. The compensation capacitor is connected to the internal low impedance node-A to achieve indirect compensation.

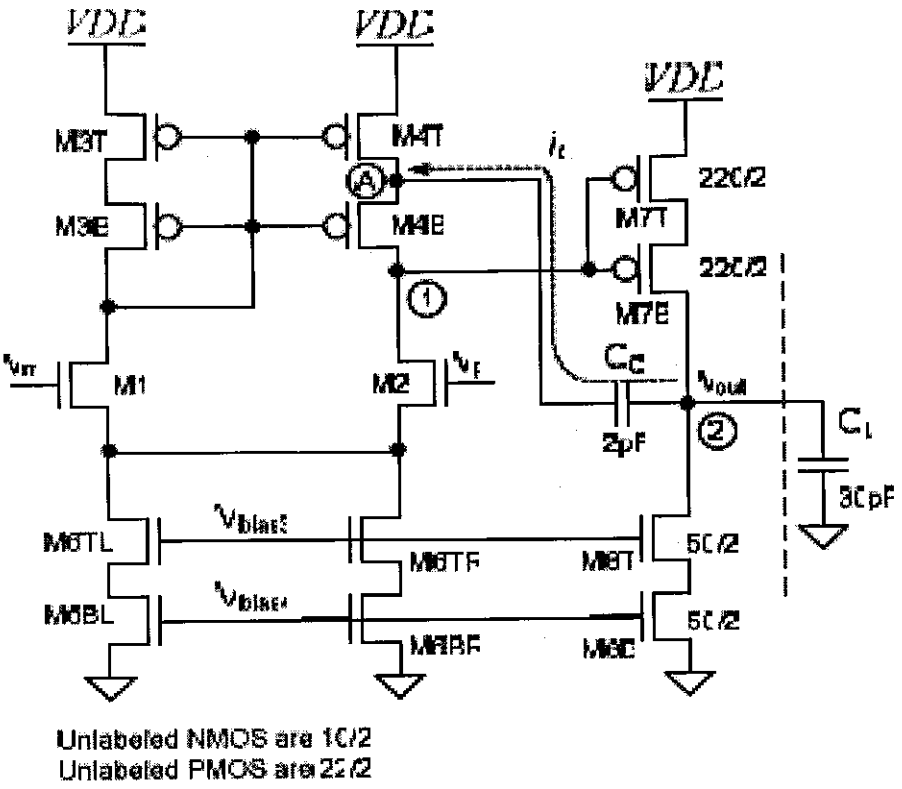


Figure 3.5: A two-stage op-amp with indirect feedback compensation using split-length load composite devices.

In order to simplify the small signal analysis of this op-amp topology, few assumptions have been made. The trans conductance of each of the split PMOS devices is denoted as g_{mp}. The resistance, R_A, can be approximated to be equal to the channel resistance of the trioded PMOS, which is close to $1/g_{mp}$. Also, here if the current mirror load is designed with the same g_m as the diff-pair, we have $g_{mp}= \sqrt{2}\, g_{m1}$. The simplified small-signal model for SLCL op-amp is shown in figure 3.6.

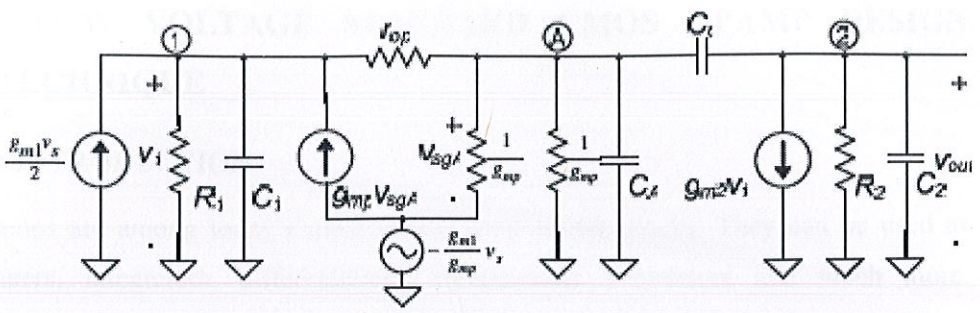


Figure 3.6: Small signal model for analysis of the two-stage op-amp employing split length load devices

On applying nodal analysis on the small signal model shown in figure 3.6, we obtain a dc gain of $-g_{m1}R_1\ g_{m2}\ R_2$ and a unity gain frequency equal to

$$f_{un} = \frac{g_{m1}}{2\pi(2C_C)}$$

The dominant pole is given as

$$p_1 \approx -\frac{1}{2g_{m2}R_2R_1C_C}$$

The LHP zero is located at

$$z_1 \approx -\frac{4g_{mp}}{3(C_C + C_A)} = -\frac{4\sqrt{2\ g_{m1}}}{3(C_C + C_A)} \approx \frac{8\sqrt{2}}{3}\omega_{un}$$

The non dominant poles are approximated

$$p_2 \approx \frac{g_{m2}\ C_C}{2C_CC_L}$$

$$p_3 \approx -[g_{mp}/C_C||C_C + 1/(R_1||r_{op})C_1]$$

3.3. LOW VOLTAGE STANDARD CMOS OPAMP DESIGN TECHNIQUE

3.3.1 INTRODUCTION

Op-amps are among today's most widely used circuit blocks. They can be used as summers, integrators, differentiators, comparators, attenuators and much more. Defined generally, an Op-amp is a high-gain differential input amplifier. Designers have been trying to integrate these versatile circuit blocks into the rest of their circuitry since the mid-1960s. The mA709 was the first Op-amp designed on an integrated circuit.

In an effort to reduce cost and space and improve performance, designers are integrating more and more circuit blocks, both analog and digital, onto a single chip. In order to reduce power dissipation, it is advantageous, at least for digital circuit blocks, to implement these "mixed-signal" chips in a standard CMOS process. In a further effort to reduce power dissipation in digital circuit blocks, it is advantageous to reduce the supply voltage V_{DD}. For a standard CMOS inverter, power dissipation may be expressed as

$$P_{avg} = C_{load} \times V_{DD^2} \times f_{clk}$$

In an effort to increase the intrinsic gain of CMOS devices, the trend in the MOSFET design industry is to shrink the gate oxide thickness, T_{ox}. Unfortunately, as T_{ox} is reduced, the MOSFET device's tolerance for high voltage levels at the gate is also reduced. This means that, for reliability purposes, it is advantageous to reduce the maximum voltage supply V_{DD}.

This trend in reducing the supply voltage means that analog designers face challenges such as reduced input common mode range, output swing and linearity. Part of the problem is that V_{TO} does not scale in a linear fashion with the reduction in minimum device length. V_{TO} is given by the following expression:

$$V_{TO} = V_{fb} + 2\phi_f + (4eE_r N_a \phi_f)^{\frac{1}{2}} \frac{1}{C_{ox}}$$

Most of the values in equation 2.2 remain relatively constant as minimum process lengths and supply voltage are scaled down. Therefore, a decrease in V_{TO} can usually

only be brought about by a decrease in Na or by an increase in C_{ox}. Unfortunately for the designer, V_{TO} does not tend to decrease at the same rate as V_{DD}.

Some fabrications do offer low V_{TO} processes specially suited for analog blocks. However, they tend to cost more than standard CMOS processes. It is therefore desirable to use low voltage design techniques, in order to be able to implement analog circuit blocks using standard CMOS processes [5].

3.3.2 LOW VOLTAGE OPAMP SOLUTIONS

3.3.2.1 FOLDED CASCODE OPAMP

The typical differential pair, shown in figure3.7, normally consists of 2 transistors connected in a common source amplifier configuration. The differential gain of this amplifier is given by:

$$A = -gm_{1,2}R_{out}$$

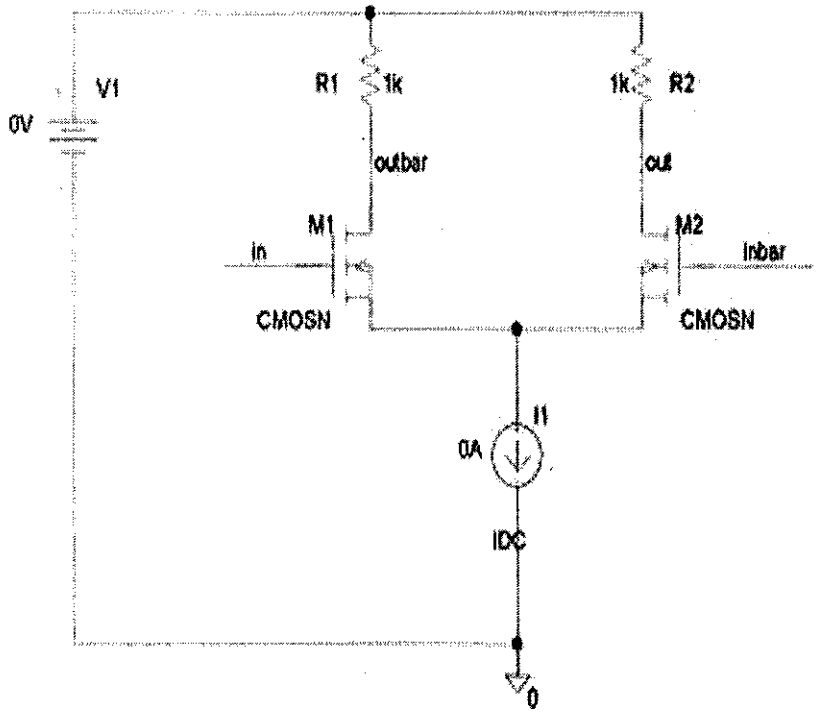


Figure: 3.7 Standard NMOS Diffpair

In an effort to increase the gain of this differential pair, it can be connected in cascade with a common gate amplifier, as shown in figure 3.8. This is known as a cascode configuration. Its differential gain is given by:

$$A_{cascode} = A_{commonsource} \times A_{commongate}$$

$$A_{cascode} = -gm_{1,2}r_{0(1,2)} \times gm_{3,4}r_{0(3,4)}$$

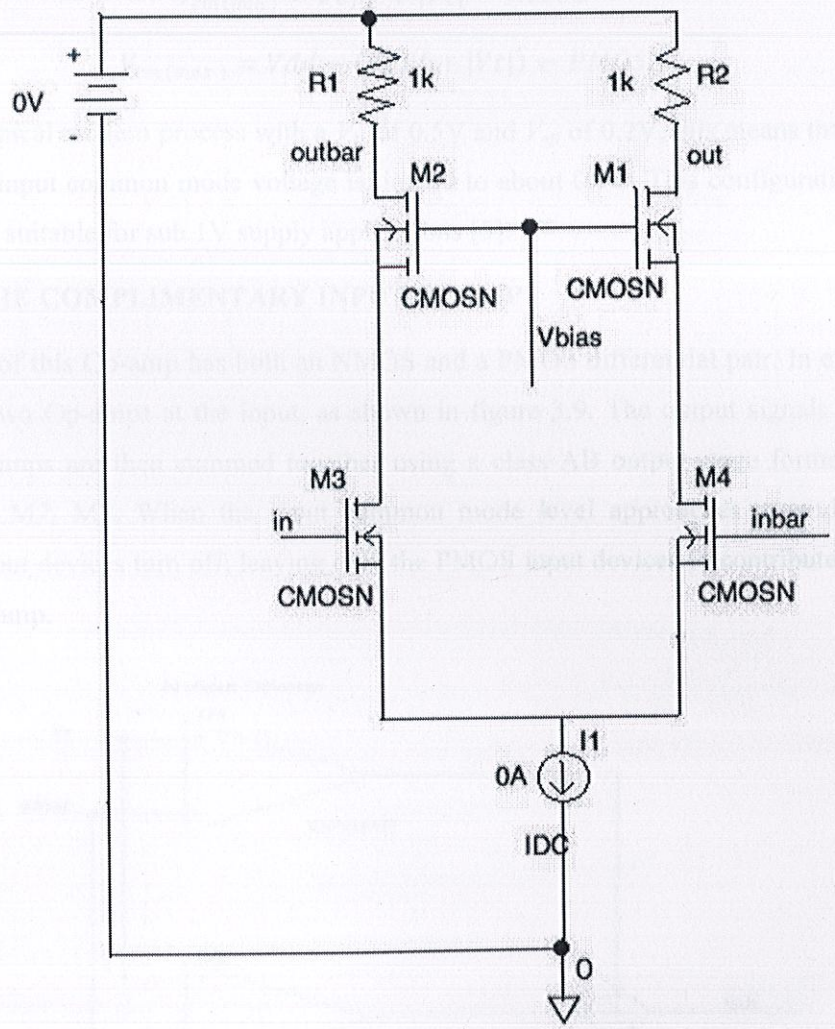


Fig 3.8 Cascode Differential Amplifier

This very large gain comes at a price. The extra transistors *M*3, *M*4 require an extra V_{eff} from the total supply headroom budget. If however *M*3, *M*4 are chosen as

PMOS devices and placed in the folded cascode configuration, then at the cost of some extra current, this configuration takes up the same amount of voltage headroom as that of the simple differential pair shown in figure 1.

In the case of an NMOS input differential pair, the input transistors must have a bias high enough so that the tail current source transistor remains in the active region. In the case of a PMOS input differential pair, the input must be biased low enough so that the tail current source transistor remains in the active region. In other words,

$$V_{cm(\min)} = Veff + |Vt| \leftarrow NMOS$$

$$V_{cm(max)} = Vdd - (Veff + |Vt|) \leftarrow PMOS$$

Given a typical modern process with a V_{Tn} of 0.5V and V_{eff} of 0.2V, this means that the minimum input common mode voltage is limited to about 0.7V. This configuration is clearly not suitable for sub 1V supply applications [5].

3.3.2.2. THE COMPLIMENTARY INPUT OPAMP

The input of this Op-amp has both an NMOS and a PMOS differential pair. In effect, there are two Op-amps at the input, as shown in figure 3.9. The output signals from these Op-amps are then summed together using a class-AB output stage formed by transistors M7, M8. When the input common mode level approaches ground, the NMOS input devices turn off; leaving only the PMOS input devices to contribute gain to the Op-amp.

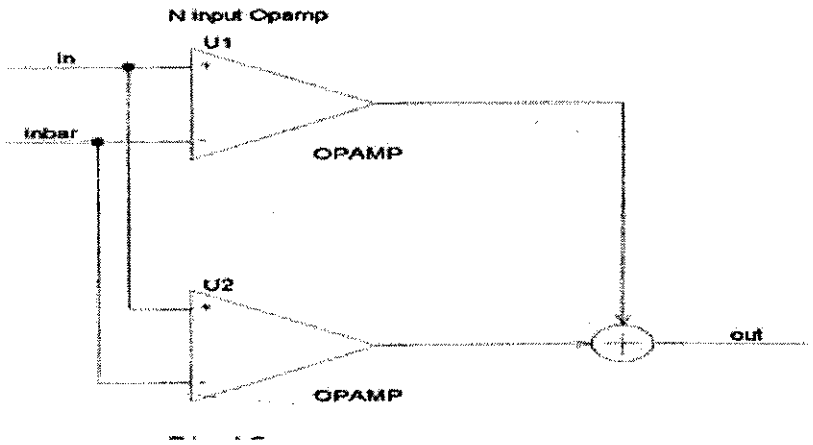


Fig 3.9 Complimentary Differential Pair block Diagram

When the input common mode level approaches V_{DD}, the PMOS devices turn off, leaving only the NMOS devices to contribute gain to the Op-amp. Unfortunately, the complementary input configuration may contain an undesirable "dead-zone" in the input common mode range. In this "dead-zone", the DC bias level is too high for the PMOS input, but not high enough for an NMOS input. The designer must ensure that there is sufficient overlap of $V_{cm(in)}$ where both the PMOS and NMOS differential pairs are active.

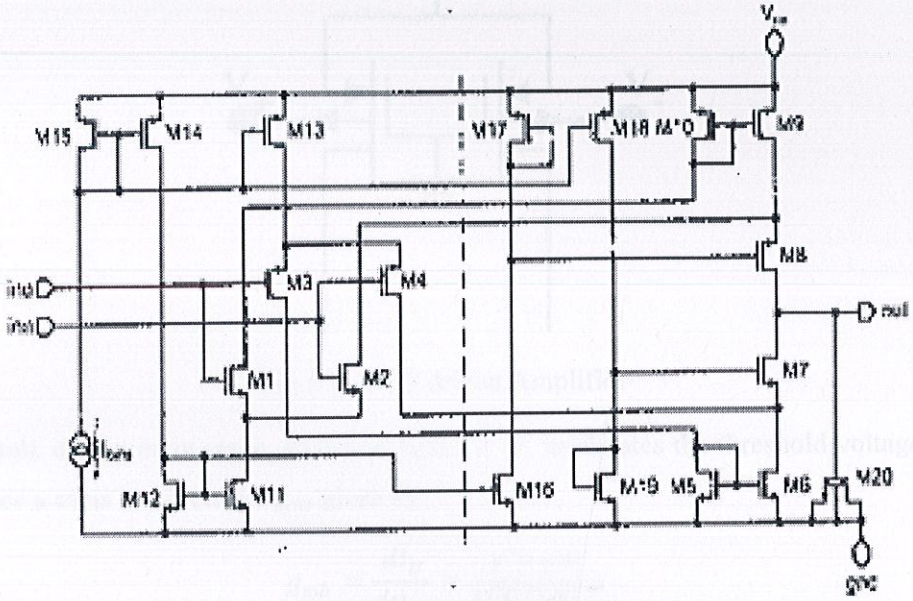


Fig 3.10 Complimentary Differential Input Scheme

For example, using a typical modern process where V_{Tn} = 0.5V, and V_{Tp} = -0.7V, and the current sources are biased to have a V_{eff} = 0.2V, equation gives us;

$$V_{cm\,(min\ N)} = 0.7 \leftarrow \text{LimitedbyNMOSdiffpair}$$

$$V_{cm\,(max\ P)} = V_{DD} - 0.9 \leftarrow \text{LimitedbyPMOSdiffpair}$$

With a 1V supply, this would leave a "dead-zone" between 0.1V and 0.7V. Clearly, the complementary input stage is also not ideal for ultra-low supply voltages [5].

3.3.2.3 THE BULK DRIVEN AMPLIFIER

In the past, analog designers have often taken for granted that a MOSFET transistor is actually a four terminal device. The Bulk terminal is usually ignored and simply

connected to ground or V_{DD}, or tied to the source terminal. Recently, however, it has been discovered that the Bulk terminal may be used as a small signal input in a completely novel family of amplifiers that are very well suited to an ultra-low supply environment.

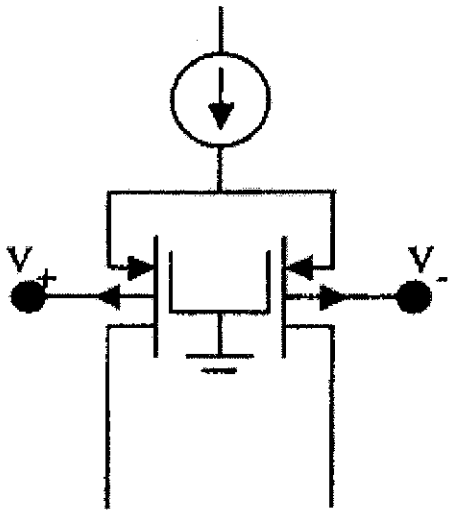


Fig 3.11 Bulk driven Amplifier

The Bulk driven input stage, shown in figure 3.11, modulates the threshold voltage to produce a trans conductance g_{mb} given by:

$$g_{mb} = \frac{di_D}{dv_{BS}} = \frac{\gamma \times gm}{\sqrt[2]{2\phi - V_{BS}}}$$

It can be shown that the gain of a Bulk driven amplifier can actually exceed that of a standard common source input differential stage when:

$$V_{BS} \geq 2\phi - 0.25\gamma^2$$

A rail-to-rail input and output Op-amp, with only a 1V supply, this Op-amp has 48.8dB gain and a 1.3 MHz unity gain frequency. This design demonstrates that Bulk driven input stages are well suited for ultra-low voltage Op-amps.

Unfortunately, the favourable properties of the Bulk driven input stage do not come without their drawbacks. Increasing the input common mode voltage VBS, whether for the purposes of increasing the gain of the Op-amp, or simply to attain rail-to-rail input common mode, comes at the price of power dissipation.

The drain current of an active MOSFET transistor is given by:

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(Vgs - V_T)^2(1 + \lambda Vds)$$

When the VT term is expanded to account for the Body effect, the equation becomes:

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_{TO} - \sqrt[\gamma]{2\phi - V_{BS}} + \sqrt[\gamma]{2\phi}\right)^2(1 + \lambda Vds)$$

Equation shows that, as VBS increases, the V_{eff} term also increases, producing a larger drain current. Another drawback of this type of input stage is that as the bias voltage to the bulk changes, the size of the depletion region between the Bulk and substrate changes. This means that the input capacitance will now be dependent on the input Bulk bias [5].

CHAPTER 4

CMOS OPERATIONAL-AMPLIFIER

4.1. General Op-amp Block Diagram

The basic block diagram of an op-amp is shown below in figure 4.1. Input is fed to the first stage that is the differential stage then we have the inverting and at the end we have the last stage that is the buffer stage.

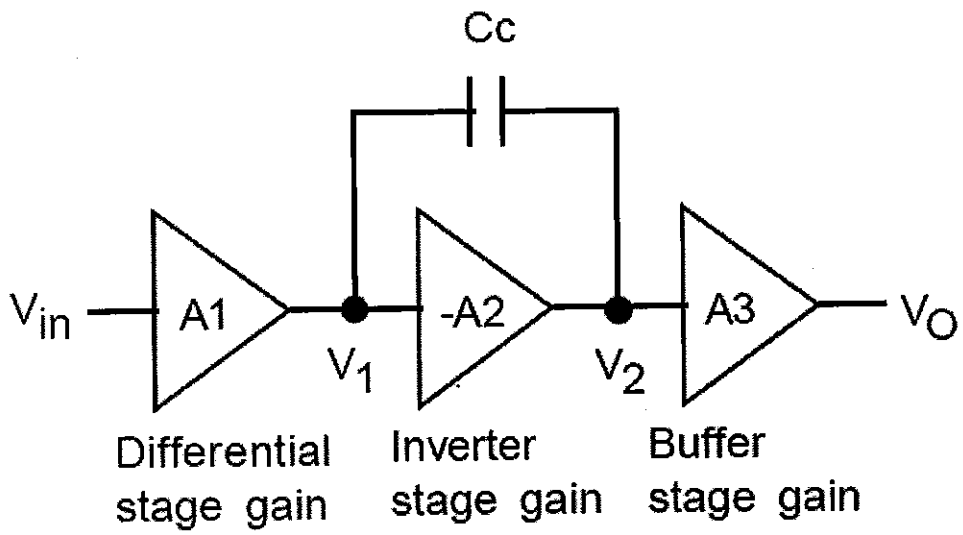


Figure 4.1: General block diagram of an op-amp.

The second stage needs to have a negative gain because of the feedback capacitor. With a positive gain an oscillator or unstable system will be implemented instead. The last stage is a buffer to convert the high output impedance of the inverter stage to low output impedance. This is needed in developing a good op-amp. Ideal op-amp requires $r_{in} = \infty$ and $r_o = 0$ [7].

The Effect of Compensation Capacitance *C*c.

At the input side,

$$\frac{V_1 - V_2}{I_1} = \frac{1}{sC_c} \; ; \; \frac{V_1 + AV_1}{I_1} = \frac{1}{sC_c} \; ; \; \frac{V_1(1+A)}{I_1} = \frac{1}{sC_c} \; ; \; \frac{V_1}{I_1} = \frac{1}{sC_c(1+A)}$$

This is known as the miller capacitance. The feedback capacitance value appears at the input side of the gain stage with a value magnified by *(1+A)*.

At the output side

$$\frac{V_2-V_1}{I_2}=\frac{1}{sC_c};\ \frac{V_2+\frac{V_2}{A}}{I_1}=\frac{1}{sC_c};\ \frac{V_2(1+\frac{1}{A})}{I_1}=\frac{1}{sC_c};\ \frac{V_1}{I_1}=\frac{1}{sC_c(1+\frac{1}{A})}=\frac{1}{sC_c};\ \text{when A>>1}$$

Due to Miller effect, the load of the first stage is effectively the compensation capacitance Cc magnified by $(1+A_2)$

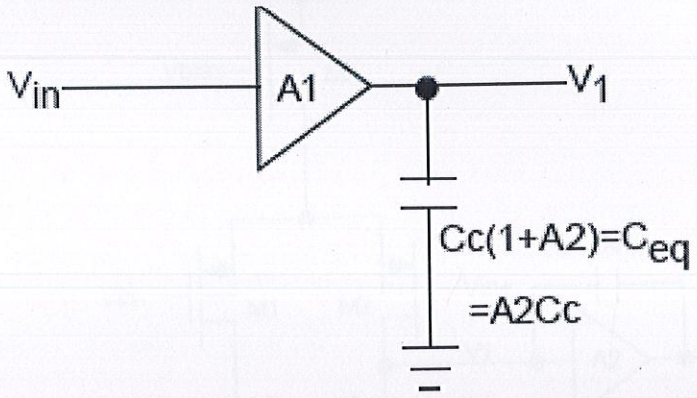


Figure 4.2: The Miller Capacitance Loading The First Stage.

The gain

$$\frac{V_2-V_1}{I_2}=\frac{1}{sC_c};\ \frac{V_2+\frac{V_2}{A}}{I_1}=\frac{1}{sC_c};\ \frac{V_2(1+\frac{1}{A})}{I_1}=\frac{1}{sC_c};\ \frac{V_1}{I_1}=\frac{1}{sC_c(1+\frac{1}{A})}=\frac{1}{sC_c};\ \text{when A>>1}$$

where:

$$Z_{o1}\approx rds2||rds4||\left(\frac{1}{sC_{eq}}\right)\approx\frac{1}{sC_{eq}}=\frac{1}{s(1+A2)C_C}\approx\frac{1}{sA2C_C}$$

The voltage gain of the op-amp, assuming the output buffer has unity gain (A3=1),

$$A_v(s)=\frac{V_o}{V_{in}}=A3A2A1=A3A2\left(\frac{g_{m2}}{sAC_C}\right)=A3\frac{g_{m2}}{sC_C}=\frac{g_{m2}}{sC_C}$$

The unity gain bandwidth, ω_{GB} is the radian frequency when the gain is 1. That is,

$$|A_v(s)|=|A_v(j\omega_{GB})|=|g_{m2}/(j\omega_{GB}C_C)|=1$$

Solving for ω_{GB},

$$\omega_{GB} = g_{m2}/C_C$$

4.2. Slew Rate Determination

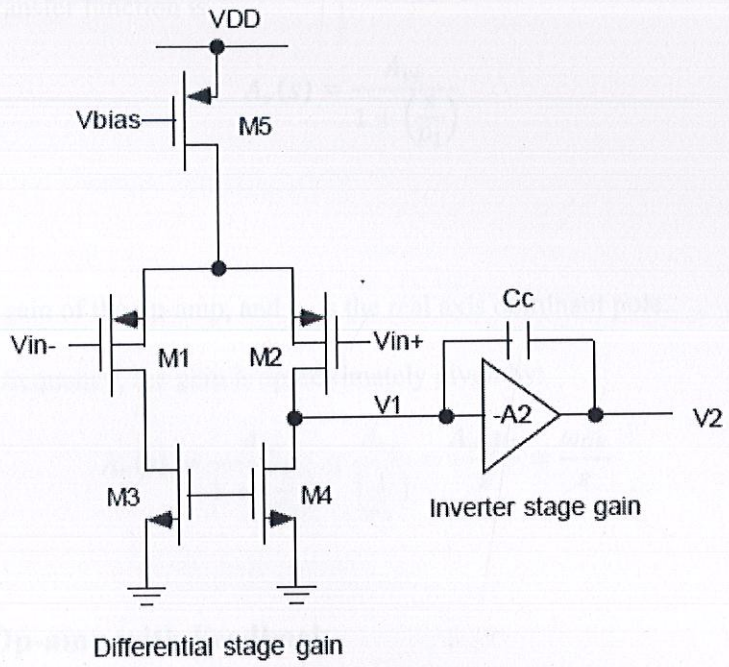


Figure 4.3: The Differential Stage Gain of op-amp

Slew rate is the maximum rate at which the output changes when input signals are large. When v_{in}+ >>0 (v_{in}-<<0) is large positive (negative), M1 is on and M2 is off. Hence $I_{SD1} = I_{SD5}$, since $I_{SD2} = 0$. The current flows through M3 which is then mirrored to M4, therefore $I_{SD1} = I_{DS3} = I_{DS4} = I_{SD5}$. The current in the compensation capacitor can only flows through *M*4, since *M*2 is off and the input impedance of the second stage A2 is ∞. That is $I_{Cc} = I_{DS4} = I_{SD5}$.

On the other hand, when v_{in}+<<0 (v_{in}->>0) is large negative (positive), *M*1 is off and *M*2 is on. Hence, $I_{SD1} = 0$ which flows through *M3* and mirrored to *M*4, therefore $I_{DS3}=I_{DS4}=0$. That is, current source I_{SD5} flows through *M*2, then to *Cc* directly, since M4 is off. In both cases, the maximum current that flows through *Cc* is I_{SD5}. The output voltage of the op-amp is approximately equal to V_2, since $A3 \cong 1$ [6].

$$SR = \frac{d(V_o)}{dt} = \frac{d(\frac{q}{C_C})}{dt} = \frac{I_{SD5}}{C_C} = \frac{2I_{SD1}}{C_C}$$

4.3. Op-Amp First Order Model

The objective of compensation is to make the op-amp to behave as a single pole in the frequency of interest. That is, at least within the unity gain bandwidth frequency, ω_{GB}. The desired transfer function is

$$A_v(s) = \frac{A_{vo}}{1 + \left(\frac{s}{p_1}\right)}$$

where:

A_{VO} is the dc gain of the op-amp, and p_1 is the real axis dominant pole.

At mid-band frequency, the gain is approximately given by:

$$A_v(s) = \frac{A_{vo}}{1 + \left(\frac{s}{p_1}\right)} \cong \frac{A_{vo}}{\left(\frac{s}{p_1}\right)} = \frac{A_{vo}p_1}{s} = \frac{\omega_{GB}}{s}$$

4.4. An Op-amp with Feedback

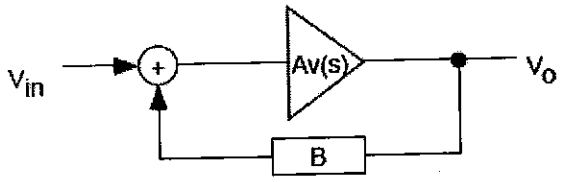


Figure 4.4: Ideal Feedback Configuration.

$$V_o = A_v V_{in} - \beta A_v V_o$$
$$V_o(1 + \beta A_v) = A_v V_{in}$$

Hence, the closed loop response is given by:

$$A_{CL}(s) = \frac{A_v(s)}{1 + \beta A_v(s)} = \frac{\omega_{GB}/s}{1 + \beta\omega_{GB}/s} = (\frac{1}{\beta})\frac{1}{1 + (\frac{s}{\beta\omega_{GB}})}$$

Where, (1/β) is the dc gain of the closed loop system. $LG(s) = \beta A_v(s)$ is the loop gain. The frequency when the closed gain is 3 Db down occurs when the LG becomes unity. That is,

$$|LG(s)| = \left|\beta \frac{\omega_{GB}}{j\omega_{-3db}}\right| = 1$$

That is,

$$\omega_{-3db} = \beta\omega_{GB} = \omega_{GB} \; ; \; \beta=1$$

4.5. Op-amp Design Specification

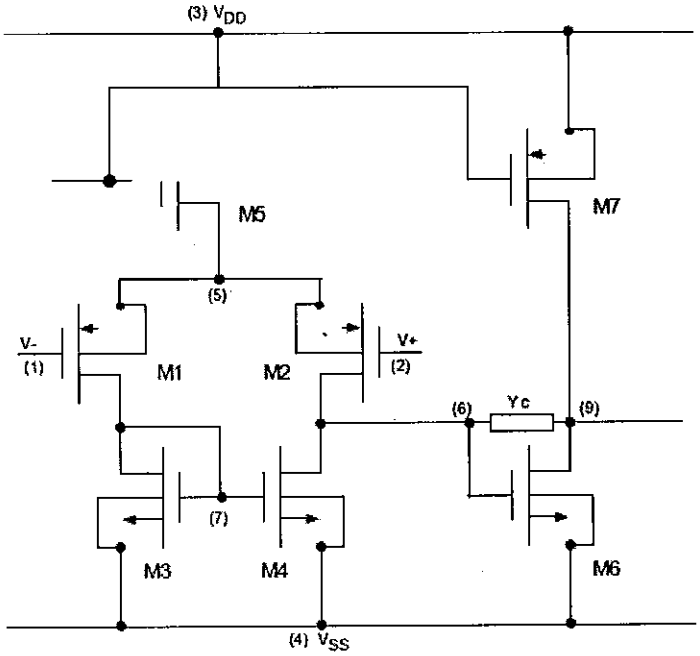


Figure 4.5: Schematic Diagram of Unbuffered Opamp

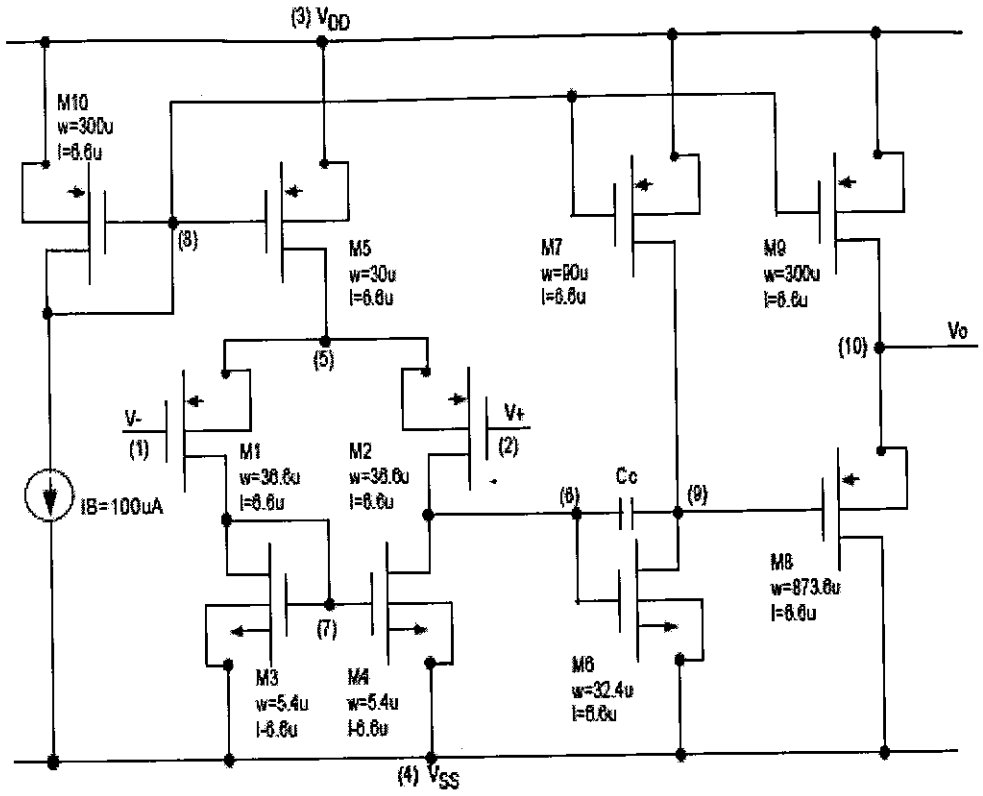


Figure 4.6: Op-amp Design Specification

Now we will calculate W/L ratios for each NMOS and PMOS for the above circuit [6]

a. CIRCUIT parameters: V_{DD} = +5V, Vss =-5V, Ao ≥ 15,000, GB = 2π(5MHz),

SR = 10V /μS, Ro ≤ 1.46k,-4.5 ≤ CMR ≤ 3, PM > 60°

b. SPICE Parameters: K_n = 40uA/V , K_p = 15uA/V, λ=0.02

(1) Determine I_{D5} from the SR specification.

Let Cc = 1pF

$$SR = \frac{I_{SD5}}{C_C} \ ;$$

$$I_{SD5} = (SR)(C_C) = (10E-6)(1E-12) = 10\mu A \ ;$$

$$V_{SD5(SAT)} = V_{SD5} - |V_{TPO}| = V_{DD} - V_{bias} - |V_{TPO}| = 5 - 3.5 - |-1| = 0.5 \ ;$$

$$(W/L)_5 = \frac{2I_{SD5}}{K_P V_{SD5(SAT)}^2} = \frac{2(10E-6)}{(15E-6)(0.5)^2} = 5.333\ ;$$

$$I_{SD1} = I_{SD2} = \frac{I_{SD5}}{2} = (10\mu A)/2 = 5\,\mu A\ ;$$

$$R_O = \frac{1}{g_{m8}} = \sqrt{\frac{1}{2\beta_8 I_{SD8}}} = \sqrt{\frac{1}{2K_P\left(\frac{W}{L}\right)_8 I_{SD8}}}$$

Solving for $(W/L)_8$, assuming I_{SD8} = 100 μA and Pspice parameter K_P = 15uA/V^2

$$\left(\frac{W}{L}\right)_8 = \frac{1}{2K_P R_O^2 I_{SD8}} = \frac{1}{2(15E-6)(1.46E+3)^2(100E-6)} = 156$$

(2) Determine $(W/L)_1$ from the ω_{GB} and positive CMR specifications.

From ω_{GB} specification,

$$\omega = (1E-12)(2\pi 5E6) = 31.4umho$$

$$(\frac{W}{L})_1 = \frac{(g_{m1})^2}{2K_P I_{SD1}} = \frac{[31.4E-6]^2}{2(15E-6)(5E-6)} = 6.57$$

From the positive CMR specification,

$$V_{G1(\max.)} = V_{DD} - V_{DS(SAT)} - V_{SG1}$$

$$V_{SG1} = V_{DD} - V_{SDS(SAT)} - V_{G1(max.)}$$

From the gate bias, V_{bias}, V_{SDS} can be determined.

$$V_{SG1} = V_{DD} - V_{SDS(SAT)} - V_{G1(max.)} = 5 - 0.5 - 3 = 1.5$$

$$V_{SD1(SAT)} = V_{SG1} - |V_{TPO}| = 1.5 - |-1| = 0.5$$

$$(\frac{W}{L})_1 = \frac{2I_{SD1}}{K_P V_{SD1(SAT)}^2} = \frac{2(5E-6)}{(15E-6)(0.5)^2} = 2.666$$

To satisfy both the specifications select the higher (W/L) ratio. For matching and symmetry, we also choose $(W/L)_2 = (W/L)_1 = 6.57$.

(3) Determine $(W/L)_3 = (W/L)_4$ ratio from negative CMR

$$(\frac{W}{L})_3 = \frac{2I_{DS3}}{K_N(V_{G1(min.)} - V_{SS})^2} = \frac{2(5E-6)}{(40E-6)(-4.5-(-5))^2} = 1 = (\frac{W}{L})_4$$

(4) Determine $(W/L)_6$ from the PM>60 specification.

$$PM = 90 - \tan^{-1}(w_{GB}/z) - \tan^{-1}(w_{GB}/p_2)$$

$$w_{GB} = \frac{g_{m2}}{C_c};\ z = \frac{g_{m6}}{C_c};\ p_2 = \frac{g_{m6}}{C_1 + C_2};\ z < p_2;\ since\ C_c > C_1 + C_2$$

A pessimistic estimate of PM is obtained by assuming $z = p_2$. That is,

$$PM < 90 - 2\tan^{-1}\frac{g_{m2}/C_c}{g_{m6}/C_c} = 90 - 2\tan^{-1}\frac{g_{m2}}{g_{m6}}$$

$$\tan^{-1}\frac{g_{m2}}{g_{m6}} < \frac{90 - PM}{2}$$

$$\frac{g_{m2}}{g_{m6}} < \tan\frac{90 - PM}{2}$$

$$g_{m6} > \frac{g_{m2}}{\tan\frac{90 - PM}{2}}$$

To achieve $PM > 60$,

$$g_{m6} > \frac{31.4E-6}{\tan(\frac{90-60}{2})} = 117.122E-6 \approx 120E-6$$

From step 4 $V_{DS6(SAT)} = 0.5V$

$$\left(\frac{W}{L}\right)_6 = \frac{g_{m6}}{K_N V_{DS6(SAT)}} = \frac{120E-6}{(40E-6)(0.5)} = 6$$

The current through M6 is given by

$$I_{DS6} = \frac{g_{m6}^2}{2K_N\left(\frac{W}{L}\right)_6} = \frac{(120E-6)^2}{2(40E-6)(6)} = 30uA$$

For balance condition the current through $M6$ must be properly ratioed with the current through $M3$,

$$I_{DS6} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_3} I_{DS3} = \frac{6}{1}(5uA) = 30uA$$

(5) Determine $(W/L)_7$ from the balance condition and that $I_{SD7} = I_{DS6}$

$$\left(\frac{W}{L}\right)_7 = \frac{I_{SD7}}{I_{SD5}}\left(\frac{W}{L}\right)_5 = \frac{30uA}{10uA}(5.333) = 15.999 \approx 16$$

(6) Dc gain A_{VO} is computed and compared with the specification:

$$A_{VO} = g_{m2}g_{m6}R_1R_2 = \frac{g_{m2}g_{m6}}{(g_{ds2}+g_{ds4})(g_{ds5}+g_{ds6})} = \frac{g_{m2}g_{m6}}{(\lambda_2+\lambda_4)I_{SD2}(\lambda_6+\lambda_7)I_{SD6}}$$
$$= \frac{(31.4E-6)(120E-6)}{(0.02+0.02)(5E-6)(0.02+0.02)(30E-6)} = 15{,}7000$$
$$\geq 15{,}000$$

(7) From the output resistance specification $Ro \leq 1.46k$, $(W/L)_8$ can be determined. The output resistance is given by:

$$R_O = \frac{1}{g_{m8}} = \sqrt{\frac{1}{2\beta_8 I_{SD8}}} = \sqrt{\frac{1}{2K_P\left(\frac{W}{L}\right)_8 I_{SD8}}}$$

Solving for $(W/L)_8$, assuming $I_{SD8} = 100\ \mu A$ and Pspice parameter $K_P = 15uA/V^2$

$$\left(\frac{W}{L}\right)_8 = \frac{1}{2K_P R_O^2 I_{SD8}} = \frac{1}{2(15E-6)(1.46E+3)^2(100E-6)} = 156$$

(8) Determine the (W/L) of the current mirrors. First set up the current source *M10* to 100uA using the biasing current source I_B. the V_{GS8} is set up to guarantee it operates at saturation by adding -0.5V beyond its threshold voltage V_{TP} = -1V. that is V_{SG10} = *1.5V*. $(W/L)_{10}$ can now be determined as follows:

$$\left(\frac{W}{L}\right)_{10} = \frac{2I_{SD10}}{K_P(V_{SG10}-|V_{TP}|)^2} = \frac{2(100E-6)}{(15E-6)(1.5-(-1))^2} = 53.33$$

The rest of current sources are determined by proportionality as follows:

$$I_{SD9} = 100uA \Rightarrow \left(\frac{W}{L}\right)_9 = \left(\frac{W}{L}\right)_{10}\frac{I_{SD9}}{I_{SD10}} = (53.33)\left(\frac{100uA}{100uA}\right) = 53.33$$

This completes the design. The result is summarized in the following table:

PAR	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
I(μA)	5	5	5	5	10	30	30	100	100	100
TYPE	P	P	N	N	P	N	P	P	P	P
W/L	6.57	6.57	1	1	5.333	6	16	156	53.33	53.33
W(μ)	36.792	36.792	5.6	5.6	29.865	33.6	89.6	873.6	298.65	298.65
L(μ)	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6
L_{eff}(μ)	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6

4.6. PSpice Simulation

The output voltage *Vo=V(10)* is *0.145V* at quiescent operating point. This non-zero output voltage can be corrected or reduced by applying an input offset voltage, *Vos*. This offset is determined by finding the value of V_{ID} that makes the output voltage *Vo* = *V(10)* = 0. From the graph given below, this is equal to –8.2484μV. The resulting output voltage from simulation is –2.753E-6V.

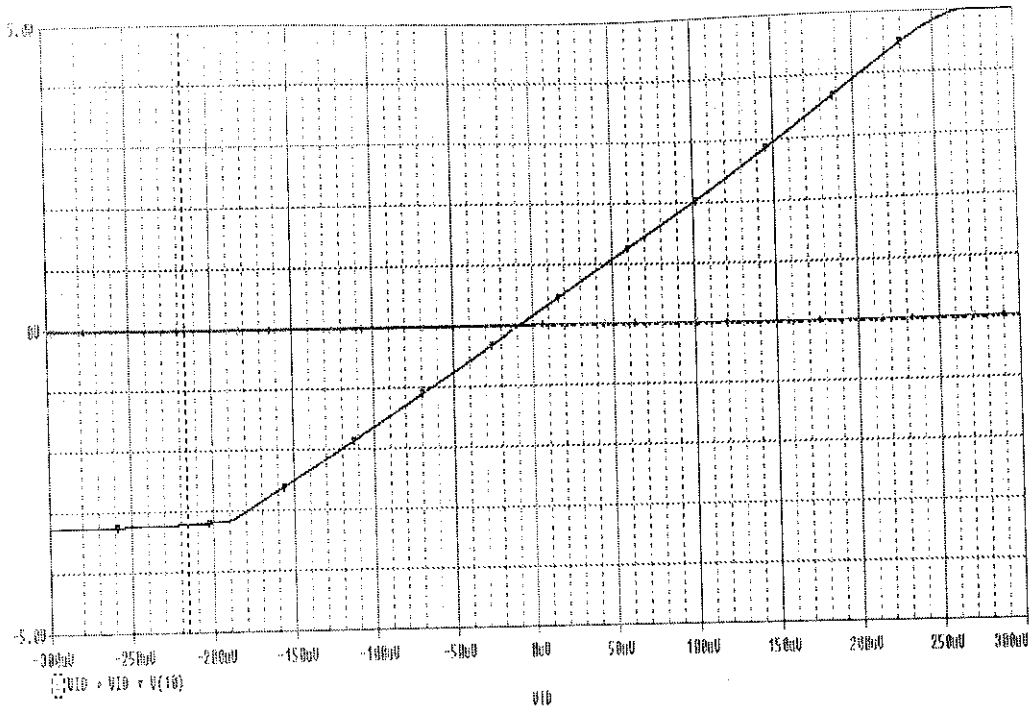


Figure 4.7: PSpice simulation for figure 4.6

- TOTAL POWER DISSIPATION 2.50E-03 WATTS
- $V(10)/V_{ID}$ = 1.816E+04
- INPUT RESISTANCE AT V_{ID} = 1.000E+20
- OUTPUT RESISTANCE AT $V(10)$ = 1.342E+03

Figure 4.8 shows the input and output voltage graph when CMOS op-amp is fed input at the inverting input point.

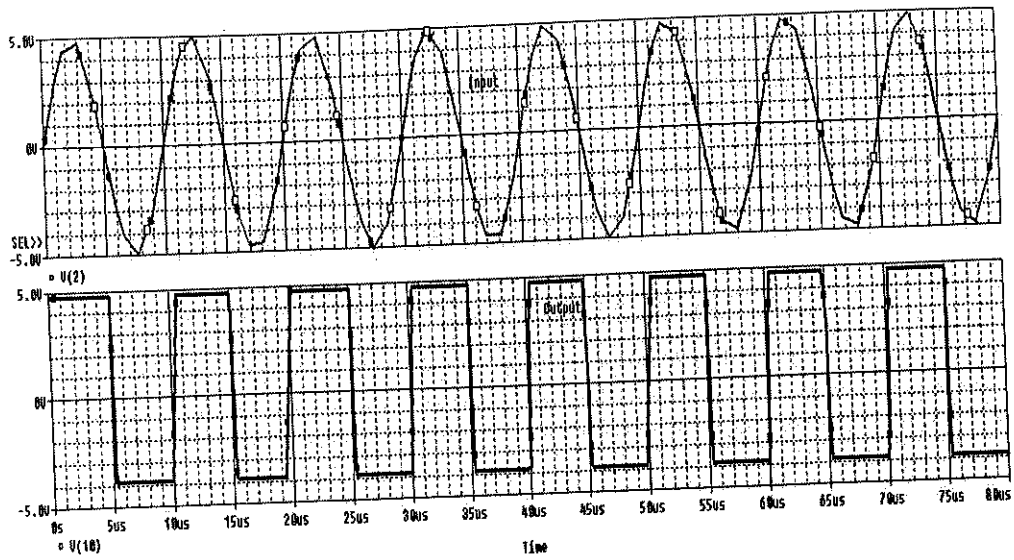


Figure 4.8: Input output of an Inverting Op-amp

Figure 4.9 shows the input and output voltage graph when CMOS op-amp is fed input at the non-inverting input point.

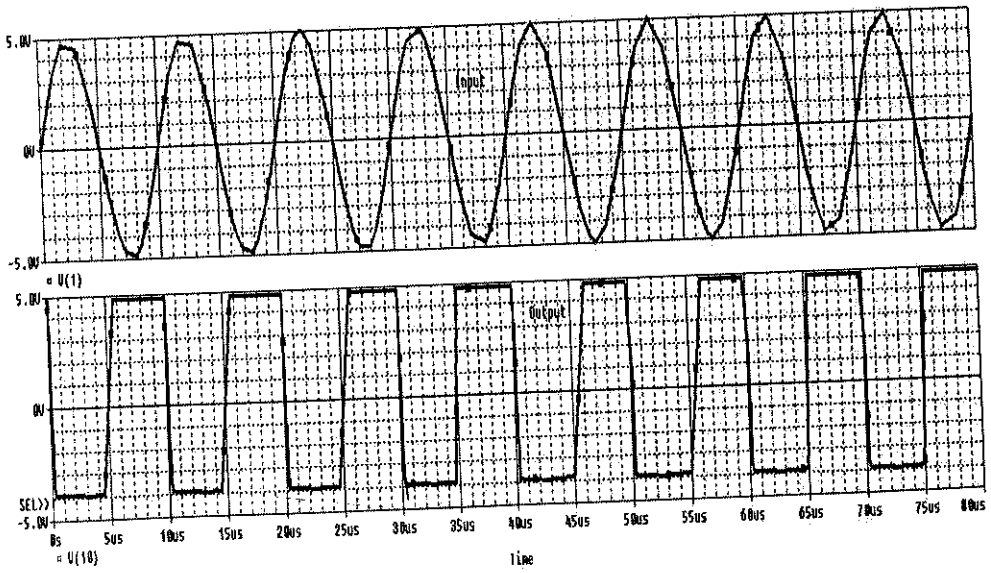


Figure 4.9: Input output of a Non-Inverting Op-amp.

CHAPTER 5

A LOW VOLTAGE CURRENT FEEDBACK OPERATIONAL AMPLIFIER

5.1 INTRODUCTION

In recent years, great interest has been devoted to the analysis and design of current feedback op-amp and current-conveyor Integrated circuits, mainly because these circuits exhibit better performance, particularly higher speed and better bandwidth, than classic voltage-mode operational amplifiers (VOA). The current feedback operational amplifier (CFOA) close-loop bandwidth is independent of its close-loop gain (provided that the feedback resistance is kept constant and much higher than the CFOA inverting input resistance) unlike VOA-based circuits, which are limited by a constant gain-bandwidth product [8]. The CFOA, shown in symbolic form in Figure 5.1(a), is a four-port network which has a describing matrix of the following form:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_O \end{bmatrix} \qquad EQ.5.1$$

Originally, CFOAs were implemented using only bipolar process technology. This technology is intrinsically well suited to process signals in the form of currents (1) giving the high bipolar junction transistor (BJT) trans conductance. More recently, several CMOS realizations for the CFOA have been reported in the literature. The CFOA has always been seen as an extension of the second generation current conveyor (CCII); therefore, the design approach was to cascade a CCII+ with a voltage follower to realize the complete circuit. The obtained bandwidth was always a degraded version of the CCII+ bandwidth. Several CMOS CFOA implementations have been presented to provide offset compensation, high current drive capability and suitability for high frequency applications compensation. The low-power/low-voltage issue, which is increasingly important in very large scale integrated (VLSI) circuits, was partially addressed in.

The CFOA is capable of operating under a minimum supply voltage ($|V_{Tp}|+V_{Tn}+V_{sat}$) and with reduced power dissipation. The new circuit includes a class AB output stage exhibiting high current drive capability and good power conversion

efficiency. A rail-to-rail input and output voltage operation is also nearly achieved.

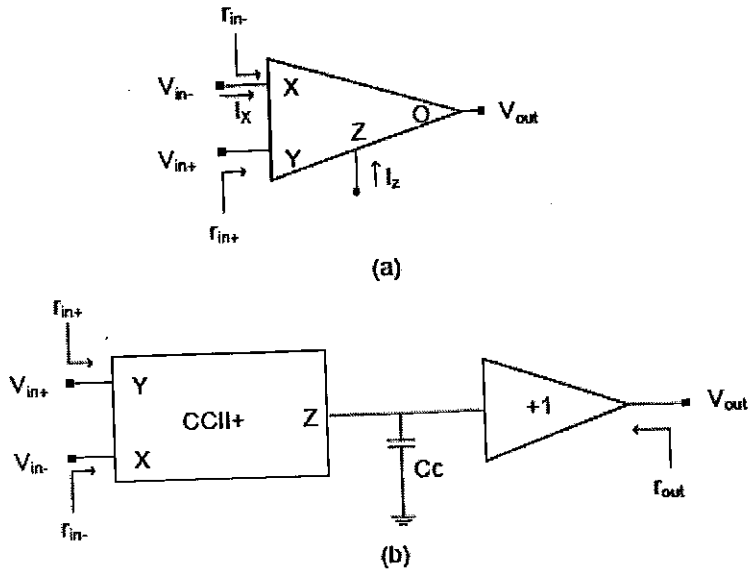


Figure 5.1: (a) Current feedback op amp symbol and (b) CFOA block diagram

As stated above, the CFOA could be realized by the CCII which is cascaded with a voltage follower, as shown in Figure 5.1(b) [9].

5.2 CMOS REALIZATION OF THE PROPOSED CFOA

The CMOS realization of the proposed CFOA, which offers both low-voltage and high drive capability will be described. The CMOS realization of the proposed CFOA shown in Figure 5.2 consists of two matched parallel connected n-differential pairs, (*M*1, *M*2) and (*M*3, *M*4); two matched biasing current source transistors, (*M*5, *M*6); a cascoded current mirror formed of matched transistors, (*M*7, *M*8, *M*9); and two pairs of matched source follower transistors, (*M*10, *M*11) and (*M*12, *M*13).

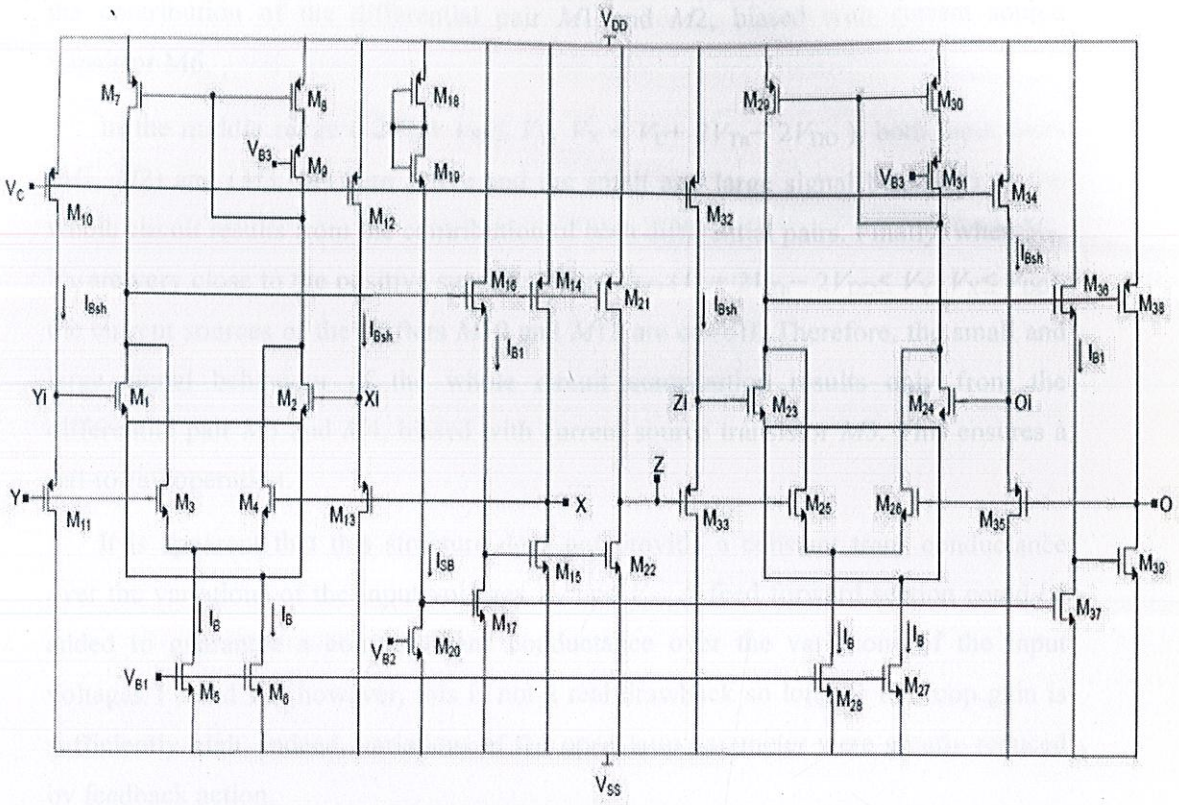


Figure 5.2: CMOS realization of the proposed CFOA.

Transistors *M*5 and *M*6 carry equal bias currents (I_B), while transistors (*M*10, *M*11) and (*M*12, *M*13) produce a positive voltage shift for the input voltage applied on transistors *M*11 and *M*13. All transistors are operating in the saturation region; the control voltage VC applied to transistor gates *M10* and *M12* controls the shifting value as

$$V_{Yi} = V_Y + (V_{DD} - V_c) \qquad \text{EQ. 5.2}$$

$$V_{Xi} = V_X + V_{DD} - V_C \qquad \text{EQ. 5.3}$$

Where V_{Yi} and V_{Xi} are the output voltages from the source followers, V_Y is the high input impedance voltage, and V_X is the low input impedance terminal.

The circuit regions of operation can be explained as follows: V_Y and V_X voltages are closed to the negative supply voltage V_{SS} ($V_{SS} \leq V_Y$, $V_X < 2V_{Tn} + V_{SS}$), so the current source transistor *M*5 and, hence, the differential pair *M*3 and *M*4 are cut-off.

Therefore, the small and large signal behaviour of the whole circuit results only from the contribution of the differential pair $M1$ and $M2$, biased with current source transistor M6.

In the middle range ($2V_{Tn}+ V_{SS}\leq V_Y$, $V_X < V_C+ 2V_{Tn}- 2V_{DD}$), both input pairs ($M1$, $M2$) and ($M3$, $M4$) are active and the small and large signal behaviour of the whole circuit results from the contribution of both differential pairs. Finally, when V_Y, V_X are very close to the positive supply voltage V_{DD} ($V_C+ 2V_{Tn}- 2V_{DD}\leq V_Y$, $V_X\leq V_{DD}$), the current sources of the shifters $M10$ and $M12$ are cut-off. Therefore, the small and large signal behaviour of the whole circuit contribution results only from the differential pair $M3$ and $M4$, biased with current source transistor $M5$. This ensures a rail-to-rail operation.

It is apparent that this structure does not provide a constant trans conductance over the variations of the input voltages V_Y and V_X. A feed forward section could be added to guarantee a constant trans conductance over the variations of the input voltages V_Y and V_X; however, this is not a real drawback so long as the loop gain is sufficiently high. Indeed, variations of the open-loop parameter were greatly reduced by feedback action.

The structure of the CFOA input stage (voltage follower) requires the X terminal to have low input impedance, so a suitable buffer circuit should be used to fulfil this condition and to provide a rail-to-rail swing capability. Transistors ($M14$- $M20$) fulfil the required buffering action with a rail-to-rail swing capability, as shown in Fig. 5.2.

Transistors $M14$ and $M15$ form the push-pull output stage at the X terminal. Transistors $M16$ and $M17$ are level-shifting transistors, providing proper biasing for transistor $M15$. This push-pull action of transistors $M14$ and $M15$ reduces the power dissipation. To prevent crossover distortion, both transistors $M14$ and $M15$ must be ON when no current is withdrawn from the X terminal (standby mode), this current should be small and controllable. This is achieved by using a suitable gate voltage of $M20$, which sets the voltage level shift between the gates of $M14$ and $M15$. The standby power consumption of the overall circuit for dual power supply is given by

$$P_{SB} = 2V_{DD}(4I_{SB} + 4I_B + 4I_{Bsh} + 2I_{B1}) \qquad EQ.5.4$$

The last term in the above equation is the current passing through the level shift transistors ($M16$, $M17$). This current can be kept small by choosing a small aspect ratio

for transistors (*M*16, *M*17). The class AB output stage enables the circuit to derive the heavy resistive and capacitive load with low standby power dissipation and no slewing. It is worth mentioning that smaller miller compensation capacitors can be connected between the gate and drain of transistors *M*14 and *M*21 to ensure good transient response under all loads. Transistors *M7* and *M*8 force the current in transistors *M1* and *M3* to be equal to the current in transistors *M*2 and *M*4;

therefore,

$$I_{M1} + I_{M3} = I_{M2} + I_{M4} \qquad EQ.5.5$$

From the above equation, the matched differential pair transistors carry equal currents; therefore,

$$V_X = V_Y \qquad EQ.5.6$$

The current follower stage, as shown in Fig. 5.2, is made up of transistors (*M*21, *M*22). It conveys the *X* terminal current into the *Z* terminal current;

therefore,

$$I_{Z=}I_X \qquad EQ.5.7$$

Finally, a suitable buffer must be available between the Z and O terminals. It is similar to the buffer between the *Y* and *X* terminals and consists of transistors *M*23 to *M*39;

therefore,

$$V_O = V_Z \qquad EQ.5.8$$

It is worth mentioning that, the proposed CFOA input stage is a dual circuit. This means that when the input stage which is formed of transistors *M*1 to *M*6 changes to PMOS, the current source formed from transistors *M7* to *M*9 and the biasing circuits *M*10 to *M*12 will be NMOS and vice versa. For small-signal analysis, when both differential stages are properly working, the open-loop gain *T(s)* is given by

$$T(s) = \left(\left(\left(\frac{g_{m11} \times (r_{ds11} || r_{ds10})}{1 + g_{m11} \times (r_{ds11} || r_{ds10})} \right) \times g_{m1(or\ m2)} + g_{m3(or\ m4)} \right) \times (r_{ds7} || r_{ds1} || r_{ds3}) \times g_{m14} \times (r_{ds14} || r_{ds15}) \right) \qquad EQ.5.9$$

In the above equations, g_{mi} and r_{dsi} are the trans conductance and the drain to source resistance of the i-th transistor where i is the transistor number. As a result for the feedback, as shown in Fig. 5.2[9], the voltage gain between the terminals *Y* and *X*

becomes

$$A_v(s) = \frac{V_X(s)}{V_Y(s)} = \frac{1}{1 + \frac{1}{T(s)}} \qquad EQ.5.10$$

For high values of *T(s), Av(s)* tends towards 1. The CFOA input resistance at the *X* terminal and the output resistance at the *O* terminal is approximately given by

$$r_{in} = r_{out} \approx \frac{(r_{ds14} || r_{ds15})}{T(0)} \qquad EQ.\ 5.11$$

The CFOA output resistance at terminal Z is simply obtained as

$$r_Z = r_{ds21} || r_{ds22} \qquad EQ.\ 5.12$$

If higher output resistances are needed, cascoded topologies can be used to increase this value and to improve the linearity performance. The CFOA dc open-loop gain can be given as

$$T(0) = \frac{r_Z}{r_{in} + r_{out}} \qquad EQ.\ 5.13$$

5.3 SIMULATION RESULTS

The performance of the proposed CFOA circuit (figure5.2) was verified by performing PSpice simulations with supply voltages ±0.75 V using 0.25 μm CMOS technology parameters. Figure 5.3 shows the output voltage swing of the proposed CFOA when used to realize an amplifier with different gains. The input voltage was applied at the non-inverting input terminal voltage Y, the output voltage obtained at the *O* terminal. The inverting input is terminated with 2 kΩ, while the *Z* terminal is terminated with resistance values of 1 kΩ, 2 kΩ, 4 kΩ, and 8 kΩ. The total standby power dissipation is 0.456 mW.

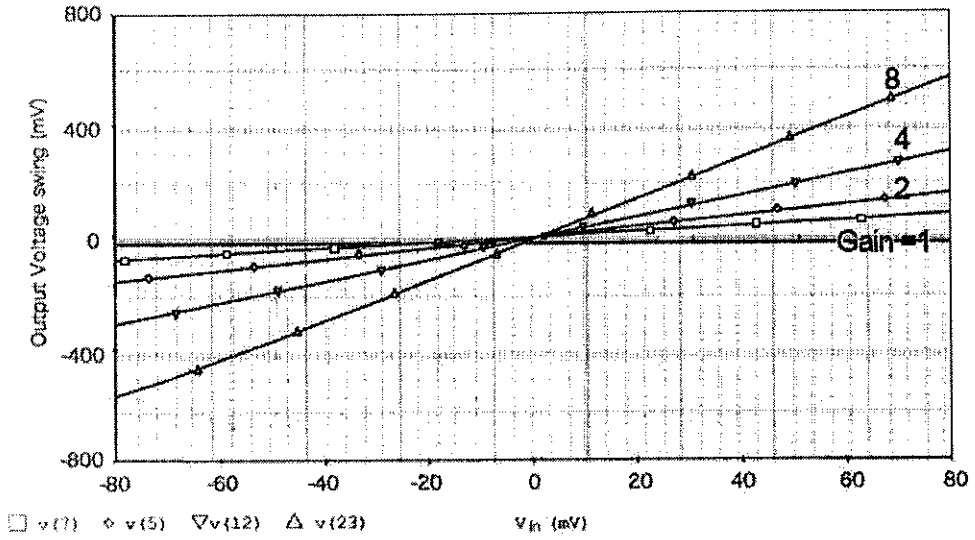


Figure 5.3: CFOA-based variable gain amplifier output voltage.

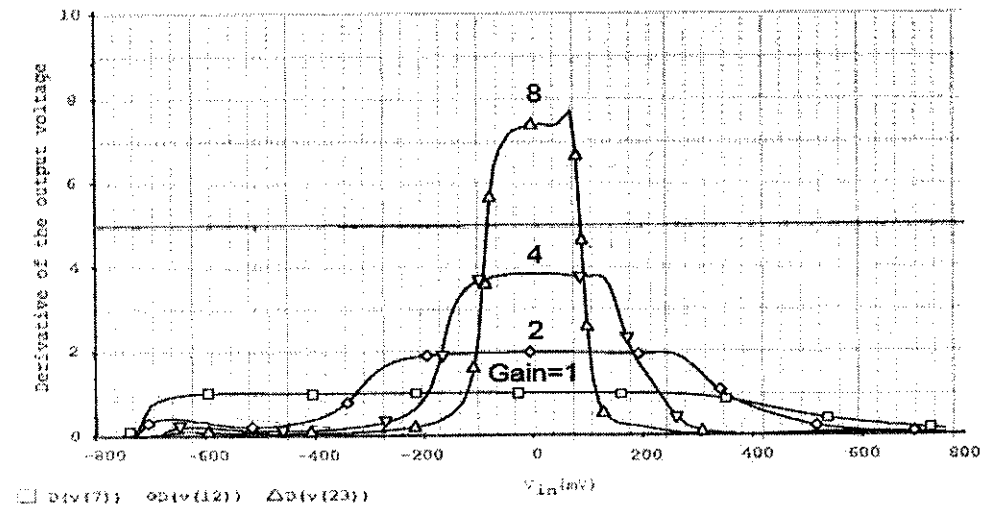


Figure 5.4: Derivatives of the output voltage of the proposed CFOA for different gains.

Figure 5.4 gives the derivative of the output voltage of the proposed CFOA versus the input voltage for different gains.

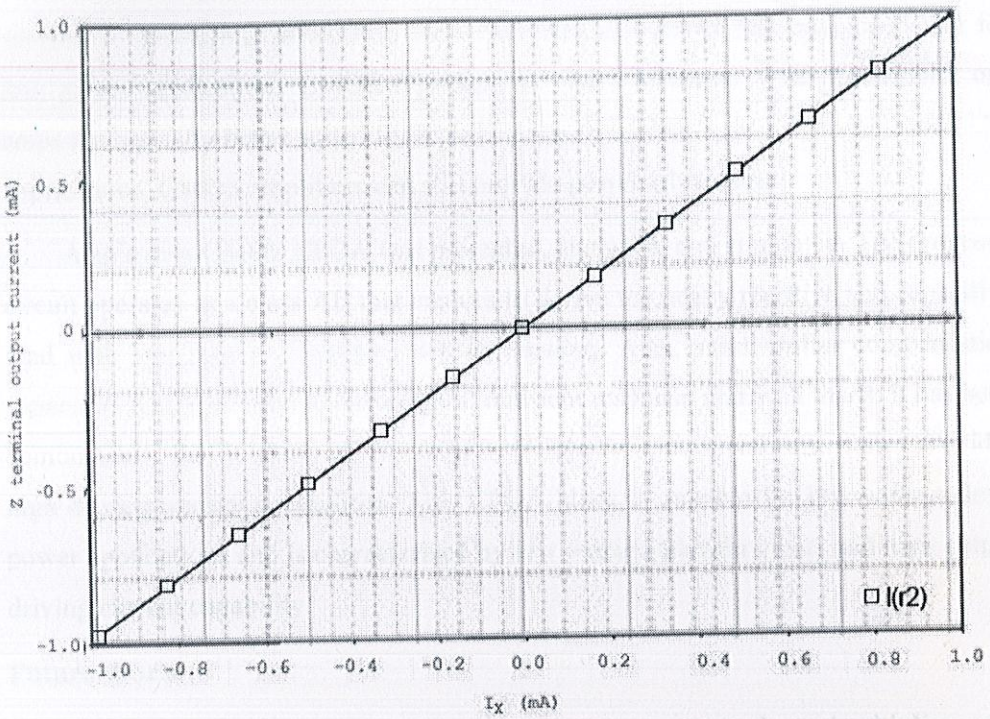


Figure 5.5: Z terminal output current swing versus the X terminal input current IX.

Figure 5.5 shows the Z terminal output current swing versus X terminal input current I_x. which shows that output current swing is linear with the input current .

CONCLUSION AND FUTURE WORK

The working of μA741 using BJT transistors was studied and analyzed in inverting and non-inverting configurations. A CMOS Operational Amplifier was designed and simulated. Its various parameters have also been calculated. We concluded that for low power applications CMOS Op-amps are more efficient. Whereas, bipolar op-amps are typically better suited for high-bandwidth applications. For lower-bandwidth applications, CMOS amplifiers can still provide power advantages.

Also a new CMOS CFOA was presented, analyzed, and simulated. The proposed circuit operates as a class AB that enables to derive the heavy resistive and capacitive load with low power dissipation and no slewing. Also, small miller compensation capacitors had been used to ensure good transient response under all loads. It has been demonstrated that it nearly allows rail-to-rail input/output operations. It also provides high driving current capabilities. This CFOA block is suitable for low-voltage, low-power applications and is characterized by low voltage-transfer errors and high output driving current capability.

Future Work:

CMOS CFOA could be employed to realize a transconductor/multiplier cell, differential integrator, CMOS band pass filter and oscillator. Moreover, further research could be performed to derive other CFOA topologies that offer compatibility with today's industry needs.

List of publications

1. Ayush Gupta, Aditya Bhansali, Swati Bhargava, Shruti Jain, "Configuration of Operational Amplifier using CMOS", March 19-20, 2010, pp 148-151, Interanational Symposiun on Computer Engineering and Technology (ISCET 2010), RIMT-Institute of Engineering and Technology, Mandi Gobindgarh, Punjab, India.

Proceedings
of

ISCET 2010

March 19th-20th, 2010

International Symposium
on
Computer Engineering & Technology

Organized by:
Department of Computer Science & Engineering
[illegible] Institute of Engineering & Technology
Mandi Gobindgarh - 147301, Punjab

Software Engineering

Configuration of Operational Amplifier using CMOS

Avish Gupta, Aditi Bhandari, Sagar Bhandari, Gaurav Gupta

Department of Electronics and Communication Engineering
Jaypee University of Information Technology, Solan

Abstract

The operational amplifier is an extremely efficient and versatile device. In applications upon the broad electronics industry filling requirements for signal conditioning, special transfer functions, analog instrumentation, analog computation, and special systems design. The analog assets of simplicity and precision characterize circuits utilizing operational amplifiers. In this paper we will compare the results of non inverting amplifier and inverting amplifier of operational amplifier made by bipolar junction transistor (BJT) and CMOS using Simulation Program with Integrated Circuit Emphasis (SPICE) simulation.

Keywords: Inverting amplifier, Non inverting Amplifier, BJT, CMOS

1. Introduction

An operational amplifier is a direct-coupled high-gain amplifier usually consisting of one or more differential amplifiers [1, 2]. The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for performing mathematical operations. Originally, the term, "Operational Amplifier," was used in the computing field to describe amplifiers that performed various mathematical operations. It was found that the application of negative feedback around a high gain DC amplifier would produce a circuit with a precise gain characteristic that depended only on the feedback used. By the proper selection of feedback components, operational amplifier circuits could be used to add, subtract, average, integrate, and differentiate. As practical operational amplifier techniques became more widely known, it was apparent that these feedback techniques could be useful in many control and instrumentation applications. Today, the general use of operational amplifiers has been extended to include such applications as DC Amplifiers, AC Amplifiers, Comparators, Servo Valve Drivers, Deflection Yoke Drivers, Low Distortion Oscillators, AC to DC Converters, Multivibrators, and a host of others. While operational amplifier can do is limited only by the imagination and ingenuity of the user. With a good working knowledge of their characteristics, the user will be able to exploit more fully the useful properties of operational amplifiers. The precision and flexibility of an operational amplifier is a direct result of the use of negative feedback. Generally speaking, amplifiers employing feedback will have improved characteristics at a sacrifice of gain. With feedback, the closed loop amplifier characteristics become a function of the feedback elements. In the basic feedback circuit, the feedback elements are two resistors. The precision of the "closed loop" gain is set by the ratio of the two resistors and is practically independent of the "open loop" amplifier. Thus, amplification of almost any degree of precision can be achieved with ease. CMOS is known for lower power consumption [3]. But the advantage true only for slower amplifiers. As the bandwidth increases, a CMOS amp's current increases dramatically. Because of the exponentially increasing current required for CMOS to achieve high speeds [4], bipolar are typically better suited for high bandwidth applications.

2. Circuit configuration

Basic concept of Operational-Amplifier configuration

Generally there are three types of circuits:

1. Inverting Amplifier
2. Non- Inverting Amplifier.
3. Difference Amplifier

2.1 Inverting Amplifier: The positive end of the input voltage V_{in} is connected through a resistor R_i to the inverting input pin (-) on the op-amp (the negative end of V_{in} is connected to ground) shown in Figure 1. The non-inverting input pin(+) is connected to ground.

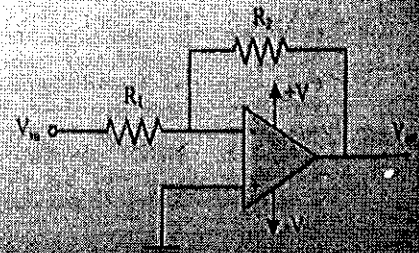


Figure 1 Inverting Amplifier

The gain A_f of an amplifier is defined as the ratio of the output to input voltage.

Bibliography

1. S. Salivahanan and V.S. Kanchana Bhaaskaran, "Advance Operational Amplifier", Linear Integrated Circuits, 2010 Edition, The Mc Graw Hill, pg.97-107,pg. 564-589.
2. Ram Gayakward, "Op-Amps and Liner Integrated Circuits", 1999 Edition, Prentice Hall, pg 123-135.
3. Mancini R., "Converting from Voltage feedback to Current feedback amplifier", Intersil Corporation, 2006.
4. V. Saxena, R.J. Baker, "Compensation of CMOS Op-amps using Split-Length Transistors", IEEE International MWSCAS, August 2008.
5. Eliyahu Zamir, "Low voltage Standard CMOD Op-amp Design Technique" ,2002
6. R.J. Baker, " CMOS: Circuit Design, Layout and Simulation", Wiley-IEEE, 2005
7. Behzad Razavi, " Stability and Frequency Compensation", Design of Analog CMOS Integrated Circuits, Edition 2002, TMH, Pg. 345-376
8. B.J. Maundy and P. Aronhime, " Alternative Realizations of CMOS Current-Feedback Amplifiers for Low-Voltage Applications", Analog Integrated Circuits Signal Processing, Volume 32, December 2002, pg. 157-168
9. S.A. Mahmoud and H.O. Elwan, "Low Voltage Rail-to-Rail CMOS Current Feedback Operational Amplifier and its Applications for Analog VLSI", Analog Integrated Circuits Signal Processing, Volume 25, 2000, pg.