Amol Vasudeva

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-3 EXAMINATION- May-2018

B. Tech VIII Semester

COURSE CODE: 11B1WCI834 MAX. MARKS:35

COURSE NAME: Parallel Processing

COURSE CREDITS: 3 MAX. TIME: Two Hours

Note: All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.

---

1. Analyze the data dependences among the following statements in a given program:

S1:	Load R1,	M(100)	/R1 ← Memory(100)/
S2:	Move R1, R1		/R2 ← (R1)/
S3:	Inc R1		/R1 ← (R1) + 1/
S4:	Add R2, R1		/R2 ← (R2) + (R1)/
S5:	Store M(100), R1		/Memory(100) ← (R1)/

where (Ri) means the content of the register Ri and Memory(10) contains 64 initially.

(a) Draw a dependence graph to show all the dependences.

(b) Are there any resource dependences if only one copy of each functional unit is available in the CPU? **[5 marks]**

2. Elaborate the Bernstein conditions for detection of parallelism, with a suitable example. **[3 marks]**
3. Explain the applicability and restrictions involved in using Amdahl's law and Gustafson's law to estimate the speedup performance of an n-processor system compared with that of a single-processor system. Ignore all communication overheads. **[5 marks]**
4. Compare the instruction set architecture in RISC and CISC processors in terms of instruction formats, addressing modes, and cycles per instructions (CPI). **[3 marks]**
5. Discuss the advantages and disadvantages in using a common cache or separate caches for instructions and data. **[2 marks]**
6. Why do most RISC integer units use 32 general-purpose registers? Explain the concept of register windows implemented in the SPARC architecture. **[4 marks]**
7. Explain the difference between superscalar and VLIW architectures in terms of hardware and software requirements. **[3 marks]**
8. Compare the relative merits of the four cache memory organizations: **[4 marks]**
   (a) Direct-mapping cache
   (b) Fully associative cache
   (c) Set-associative cache
   (d) Sector mapping cache
9. What are the six types of vector instructions? Define these vector instruction types by mathematical mappings between their working registers or memory where vector operands are stored. **[6 marks]**