Design of VLSI Interconnect Circuits for Energy Performance Optimization

Thesis submitted in fulfilment of the requirements for the Degree of

DOCTOR OF PHILOSOPHY

By

Himani Bhardwaj

Department of Electronics and Communication Engineering

JAYPEE UNIVERSITY OF INFORMATION

TECHNOLOGY, WAKNAGHAT, DISTRICT

SOLAN, H.P., INDIA

DECEMBER, 2024

CONTENTS

DECLARATION

I hereby declare that the work contained in the Ph.D. thesis entitled **"Design of VLSI Interconnect Circuits for Energy Performance Optimization"** submitted at **Jaypee University of Information Technology, Waknaghat, India** is an authentic record of my work carried out under the supervision of **Dr. Shruti Jain & Dr. Harsh Sohal**. I have not submitted this work elsewhere for any other degree or diploma. I am fully responsible for the contents of my Ph.D. thesis.

Himani Bhardwaj
Enrolment No.: 206003
Department of Electronics and Communication Engineering
Jaypee University of Information Technology, Waknaghat,
Solan, H.P-173234
Date: 20-11-2024

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY
WAKNAGHAT, P.O. – WAKNAGHAT,
TEHSIL – KANDAGHAT, DISTRICT – SOLAN (H.P.)
PIN – 173234 (INDIA) Phone Number- +91-1792-257999
(Established by H.P. State Legislature vide Act No. 14 of 2002)

CERTIFICATE

This is to certify that the work reported in the Ph.D. project report entitled **"Design of VLSI Interconnect Circuits for Energy Performance Optimization"** which is being submitted by **Himani Bhardwaj (206003)** in fulfilment for the award of Doctor of Philosophy in Electronics and Communication by the **Jaypee University of Information Technology**, is the record of candidate's own work carried out by her under my supervision. This work is original and has not been submitted partially or fully anywhere else for any other degree or diploma.

Dr. Shruti Jain
Professor, Associate Dean (Innovation)
Department of ECE
Jaypee University of Information Technology,
Waknaghat, Distt-Solan, H.P.

Dr. Harsh Sohal
Associate Professor
Department of ECE
Jaypee University of Information Technology,
Waknaghat, Distt-Solan, H.P.

ACKNOWLEDGEMENT

First and foremost, I am grateful to and dedicate everything to the Divine GOD for his unwavering support, guidance, and forbearance throughout my life and during this research effort. Such a large-scale research undertaking can never be completed by one person working alone. This has been made possible by the numerous people who have contributed in various ways. I would like to express my profound appreciation to everyone who helped me during my doctoral studies.

I would like to extend my profound gratitude and special appreciation to my supervisors, Dr. Shruti Jain and Dr. Harsh Sohal, for their candid and insightful opinions on various matters about my research topic, as well as for supporting my work and for helping me develop as a research scientist. They gave me motivational advice that helped me finish my research project successfully. I consider it an honour to be able to work under their direction. Your guidance on both my studies and my job has been invaluable. When I most needed it, your constant moral support, priceless recommendations, and advice were a blessing.

I would like to express my gratitude to Jaypee University of Information Technology for allowing me to complete this research effectively and for providing the tools and resources I needed. I am indebted to Prof. (Dr.) Rajendra Kumar Sharma, the Vice-chancellor, for his inspiring and modest demeanor, which has always motivated me. A special thank you to Prof. (Dr.) Ashok Kumar Gupta, the Dean (academics & research), for providing high-quality instruction with ethics and values as its foundation.

I would like to express my sincere gratitude to Dr. Rajiv Kumar, Head of the Department of Communication and Electronics for their assistance, encouragement, and cooperation. I also want to express my gratitude to the DPMC members for all of their help and insightful advice during my research. I would like to express my gratitude to all of the Department of Electronics and Communication Engineering faculty members for their support and advice throughout this project.

Last but not least, I want to express my gratitude to my parents for their encouragement, spiritual support, personal attention, and care. I will never forget the hardships my parents endured while I conducted my research. I could not have overcome my disappointments and setbacks were it not for their love and blessings.

I owe a debt of gratitude to everyone who helped make this dissertation feasible and without whom this amazing journey and research experience would not fade from my priceless memories.

Even while some may go unmentioned, none is overlooked.

Thanks to all.
Himani Bhardwaj

LIST OF ABBREVIATIONS AND ACRONYMS

ADL	Adiabatic Dynamic Logic
Al	Aluminium
ASIC	Application Specific Integrated Circuit
C	Capacitance
CMOS	Complementary Metal-Oxide-Semiconductor
CMS	Current Mode Signalling
Cu	Copper
DSM	Deep Submicron
FinFET	Fin Field Effect Transistor
GHz	Giga Hertz
IC	Integrated Circuit
IMD	Intermetal Dielectric
IoNT	Internet of Nano Things
ITRS	International Technology Roadmap for Semiconductor
L	Inductance
MOS	Metal-oxide-semiconductor
PCB	Printed Circuit Board
PTM	Predictive Technology Models
R	Resistance

Si	Silicon
SoC	System on Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
SSAT	Simulative Sweep Analysis Technology
ToF	Time of Flight
VHDL	VHSIC Hardware Description Language
VLSI	Very Large-Scale Integration

LIST OF FIGURES

Figures **Page No.**

LIST OF TABLES

Tables **Page No.**

ABSTRACT

In deep submicron (DSM) technologies, such as those at 90 nm and lower, interconnects are crucial. In previous technologies, gate delay predominated over interconnect delay; however, this is no longer the case, and interconnect delays are becoming more and more significant. This is because, with DSM technologies, an interconnect cannot be viewed as a simple resistor; instead, accompanying parasitics like capacitance and inductance must also be taken into account. As a result, any signal that travels through one of these connections will always be delayed. One common method to cut down on (or eliminate) the delay is buffer insertion. This method involves inserting buffers at regular intervals along an interconnect to try and recover the signal each time the parasitics influence it. However, the switching times of buffers themselves vary. Therefore, a significant number of these buffers along an interconnect may add to the total latency in signal propagation. Buffer switching also adds to the loss of power. Furthermore, a significant issue with DSM technology is leakage power, and buffers have the potential to use power even when they are not switching. Therefore, it is imperative to develop methods that, in addition to decreasing total latency, also use less power—both dynamic and static.

This thesis investigates a proposed interconnect structure (H-model) for both RC and RLC interconnect lines. The interconnect structures are proposed for two types of networks namely lumped and distributed network using L and π-models. An Elmore delay estimate is drawn for long wires and it is verified that for long wires delay increases with the square of interconnect length. To resolve this issue, Schmitt trigger and CMOS inverter using FinFET technology are used as a substitute for buffers to lower power and delay in interconnects. However, the focus is on the reduction of power consumption and dissipation to be able to be used for small portable devices. Hence, the buffers are implemented using Energy Recovery Techniques to reduce power consumption as well as power dissipation into the interconnect circuits. As a result, power is observed to be decreased yet, increasing the area of the chip. Further, to address the issue of area as well, current mode signalling is used to the interconnect circuits to reduce additional delay due to the large buffers added in between long wires. However, decrease in technology and wire geometry, long wires (say 10mm) show introduction of inductance as a parasitic component in the interconnect circuits. This not only forces to study RLC lines but also the issues which come along with it such as coupling noise

and distortion. Also, it is shown that the proposed H-model can be used for IoT applications with best results.

CHAPTER 1

INTRODUCTION

CHAPTER 1: INTRODUCTION

Interconnects are the connecting wires between different electronic devices and components in an integrated circuit. The impacts of these cable connections are now irreversible because of the increasing clock and operating frequencies of electronic gadgets, which are reaching several GHz. In reality, it is anticipated that connection effects also known as signal integrity issues like delays, power consumption, and cross-talk will become a bottleneck as electronic circuit speeds continue to rise. To avoid such issues various methods and techniques are defined such as circuit modelling for high frequency circuits.

Interconnects are the wires that are responsible for providing power, ground, and transmitting signals to different parts of a chip. However, the performance of an interconnect highly depends upon the material used for it. Generally defining parameters for an interconnect are the resistance, capacitance and the inductance. These parameters determine the overall performance of the interconnect circuits by measuring timing constant, power consumption as well as power dissipation. Hence, proper interconnect modelling and optimization must be done to minimize the parasitic effects affiliated to them.

Another key aspect for an interconnect circuit are the metal layers and vias. An IC may have multiple metal layers, depending upon the complexity of a design. The connections between the various chip components are routed via these metal layers. Whereas, vias are used to provide signals that can be transferred vertically between the various metal layers via vias. To build a 3D interconnect structure inside the IC, vias are necessary. To understand the proper functioning and layout of an interconnect circuit design first basic VLSI design flow must be studied.

1.1 BASIC VLSI DESIGN FLOW

Using hundreds or even millions of transistors to create integrated circuits (ICs) on a single silicon chip is known as very large-scale semiconductor integration (VLSI). To successfully create these massive electronic systems, VLSI design requires a number of difficult steps and approaches. The design flow, which is a set of procedures and stages that direct engineers in turning an idea into a working chip, is an essential component in VLSI design. It is also known as the design methodology which requires a systematic approach used in VLSI design

to ensure the efficient and effective development of integrated circuits. It provides a structured framework that helps designers navigate through different stages of the design process, from concept to production. A number of steps are involved in the design flow, such as specification, design entry, synthesis, verification, layout, and manufacture. Fig. 1.1 shows the basic flow for VLSI design.

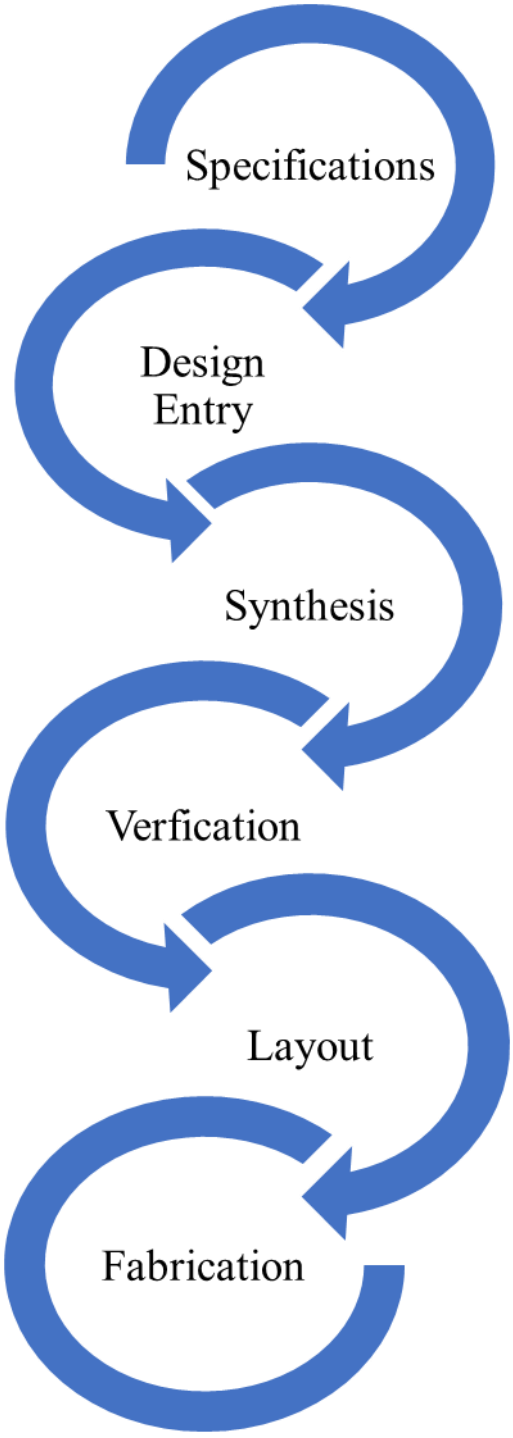


Fig. 1.1. Basic VLSI Design Flow

A typical design process comprises two primary phases: front-end (functional design) and back-end (physical design). The front-end phase of the design includes specifications, design entry, synthesis, and verification of the digital logics and designs. Specifications are the customer's requirements from an integrated circuit. Some customers may require an application specific IC to perform a certain task such as desired functionality, performance targets or power constraints etc. So, it may be said that logic in design flow can change according to the customer's requirement. Once the specifications get finalised, designers move to the design entry phase. That means after finalising the technology and the geometry of devices to be used to make a particular application specific integrated circuit, engineers begin to design the structure of the ASIC. Design entry is the creation of high-level representation of the circuit design using descriptive languages such as Verilog/VHDL. Design entry requires the structure and behaviour of the circuit design. After the circuit design is created and finalised, engineers move to synthesis phase in which gate-level representation is done using synthesis tools. These tools map the functionality of the circuit described by descriptive languages into a set of standard libraries. The power constraints, area and performance related specifications can be optimised in this synthesis phase. And after gate-level specifications are done, the circuits are verified for their proper functionality before layout phase begins. It is a critical step where designers ensure that the intended circuit matches the proper functionality and specified requirements. Various techniques such as functional simulation, formal verification, and timing analysis are employed to validate the design. Once the front-end phase completes, back-end process starts which includes layout phase and fabrication phase. After verification of the circuit's functionality, its physical creation comes into creation. This entails arranging the chip's components and designing the connections that connect them. To minimise wire length and lessen parasitic effects, among other manufacturing restrictions, layout tools are employed to optimise the physical design. Eventually, all of the circuit's functionality and physical designing comes to the final phase that is the fabrication. Sending the layout files to a semiconductor foundry for manufacture is the last step in the design flow. Based on the layout specifications, the foundry employs sophisticated manufacturing methods to produce the physical integrated circuit. This calls for procedures like etching, depositing, and photolithography. These are the techniques utilised in the process of creating an integrated circuit.

Both the front-end and back-end phases are considered to be the important phases in the VLSI design flow when it comes to interconnections. The back-end physical design process

takes a gate-level netlist into a layout that includes floor planning, module placement, and interconnect routing and the physical setup yields parasitic impedances. The functional design approach must take the interconnect latency into account, as interconnection becomes more and more crucial. A significant number of timing violations may result from a circuit design that is based on faulty delay models. Timing closure is frequently achieved through design iterations. Adding physical information early in the logic synthesis step is one way to solve this issue. Before the synthesis process, a preliminary floor plan is made to give an approximate idea of where the cells are located and how long the interconnects are. With the far more accurate timing model that this estimate offers, synthesis efficiency is increased and a placed gate-level netlist is produced. This is referred to as "Physical synthesis." Interconnect is essential to the design flow for the phases of timing verification and physical synthesis. The connection analysis criteria for these two steps differ. All through the synthesis process, precise routing information is not available, hence models like closed-form models that have higher efficiency and acceptable accuracy are preferred. At the post-layout verification stage, realistic timing data characterising the entire integrated circuit are calculated, requiring both high efficiency and great accuracy.

1.2 VLSI INTERCONNECTS

The rapid advancement of integrated circuit (IC) technology has led to the miniaturization of transistors and the increased complexity of Very Large-Scale Integration (VLSI) circuits. Due to this, designing and building high-performance VLSI systems has become extremely difficult, especially in the areas of power consumption and interconnect latency. A collection of electronic circuits and parts arranged on a small planar silicon semiconductor substrate is called an integrated circuit, or chip. Interconnects, which are planar or vertical conductor parts, are used to electrically connect these electronic circuits and components [1]. Interconnects are the fundamental unit of signal connection between chips or between chips on a printed circuit board (PCB). The arrangement and design of an integrated circuit interconnects directly affects its performance, effectiveness, reliability, efficiency, and overall fabrication yield because the amount of data flowing via networks and data centres today is growing at an unstoppable rate of about 25% per year. High-bandwidth, low-latency communication solutions that are highly optimised are necessary for the efficient movement, storing, and processing of this data. Numerous considerations, including electrical conductivity, mechanical and chemical compatibility, and fabrication difficulties, go into selecting the composite material for the interconnects [2]. In the last fifty years, silicon (Si)

has emerged as the industry standard substrate for ICs, which have found countless uses in the computer, consumer electronics, and communication sectors [3]. Integrated circuit performance is increasingly dependent on the overall signal, power, and thermal integrity of their high-speed interconnects. Robert Noyce of Fairchild Semiconductor created monolithic integrated circuits (ICs) in 1959 using aluminium (Al) instead of silicon (Si) as the connecting material. Aluminium's strong adhesive properties, low resistance, and simplicity of deposition made it a preferred connection material from 1959 until the early 1990s [4]. However, electromigration problems with Al-based interconnects reduce the dependability of the IC and shorten its lifespan [5]. Because of this, copper (Cu) interconnects, which have higher conductivity and lower electromigration than Al interconnects, replaced Al-based interconnects in the late 1990s and early 2000s [5]. Interconnections have a major impact on circuit performance as semiconductor technology shrinks to sub-10nm nodes [6]. Because interconnection latency is becoming more and more influential, the scaling of feature sizes has also resulted in intrinsic circuit performance restrictions. In order to provide directions for the development of interconnect technologies, a thorough analysis of the relationship between interconnect delay, power consumption, and numerous technology parameters – such as wire resistance, capacitance, inductance, width, length, and load capacitance has been conducted [6][7]. Depending upon these parasitic components and the dimensions of interconnects different types of on-chip interconnects can be generalised as shown in Fig. 1.2 [8]: local, intermediate or semi-global, and global interconnects.

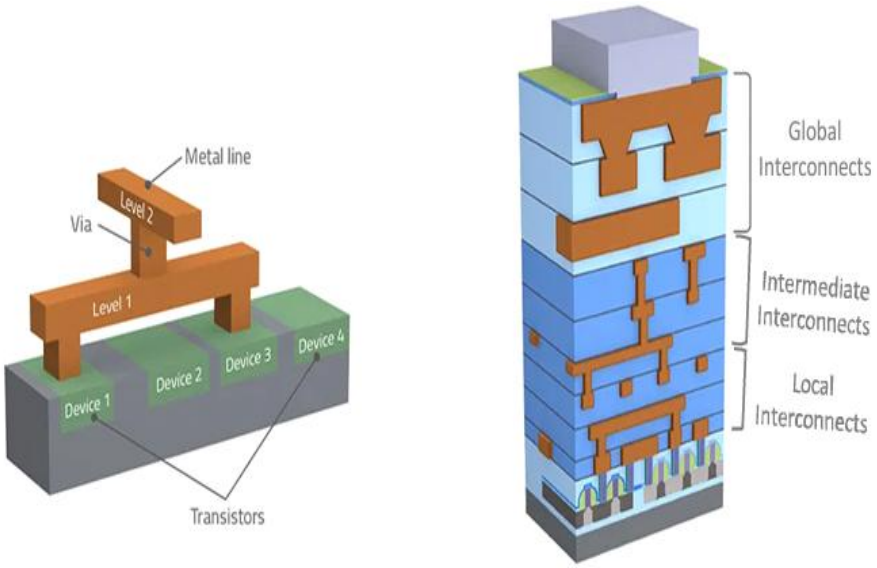


Fig. 1.2. Types of interconnects [8]

Depending upon dimensions and geometry, different types of on-chip interconnects can be defined as -

i. *Local interconnect* – These are the smallest wires, runs shortest distant connecting two or more components within a block. Local interconnects are the lowest, or initial, level of interconnects. They usually connect emitters, bases, and collectors in bipolar technology and gates, sources, and drains in MOS technology. Polycrystalline silicon, a local connection, doubles as the gate electrode material in MOS technology. Local interconnects are also provided by silicide gates and silicide source/drain regions. Furthermore, TiN a by-product of a silicide gate technique can be utilised as a local interconnect. Since local interconnects don't travel very far, they can afford to have larger resistivities than global interconnects. However, they also need to be resistant to greater processing temperatures.

ii. *Intermediate interconnect* – These are the wires which are slightly longer than the local interconnects that connects devices within the same block. These are also known as semi-global interconnects.

iii. *Global interconnect* – These are the long wires, run long distance connecting two blocks on a chip. Ground lines, electricity, buses, and clocks are examples of global interconnection. These are responsible for communicating between different regions of the chip or even between multiple chips therefore are made up of low resistive metal.

The process of producing chips begins with the creation of each component on the wafer. After that, these components are connected and the power and ground wires are connected. However, there is still not enough space to establish all the connections, therefore chip makers construct interconnects in vertical layers or levels. Interconnects in complicated circuits might have ten or more layers on which ohmic connections link an interconnect to silicon substrate active areas or devices. The active regions are isolated from the first level global connection by a high resistivity dielectric layer, typically silicon dioxide, and electrical contact is established via holes in the dielectric layer between the connection and the silicon's active areas. Because they are separated by the same dielectric layer, contact can be established between the local and first-level global interconnects at the same time during processing as shown in Fig. 1.3. Typically, connections made between two tiers of global interconnects are referred to as vias. They are created by gaps in the various intermetal

dielectric layers. Vias, or connections between interconnect levels, enable the transmission of power and communications from one layer to the next as shown in Fig. 1.3 [9,10]. Whether they are vias or contacts, their objective is to minimise their contribution to the overall electrical resistance while electrically connecting various levels of conducting layers. Dielectric materials are used to separate interconnects from one another as well as from the active areas and devices. Intermetal dielectrics, or IMDs, are the dielectric layers that divide one global connection level from another. Vias link interconnects via these different layers [10]. We now need to think about what will happen to the structure's proportions as technology advances.

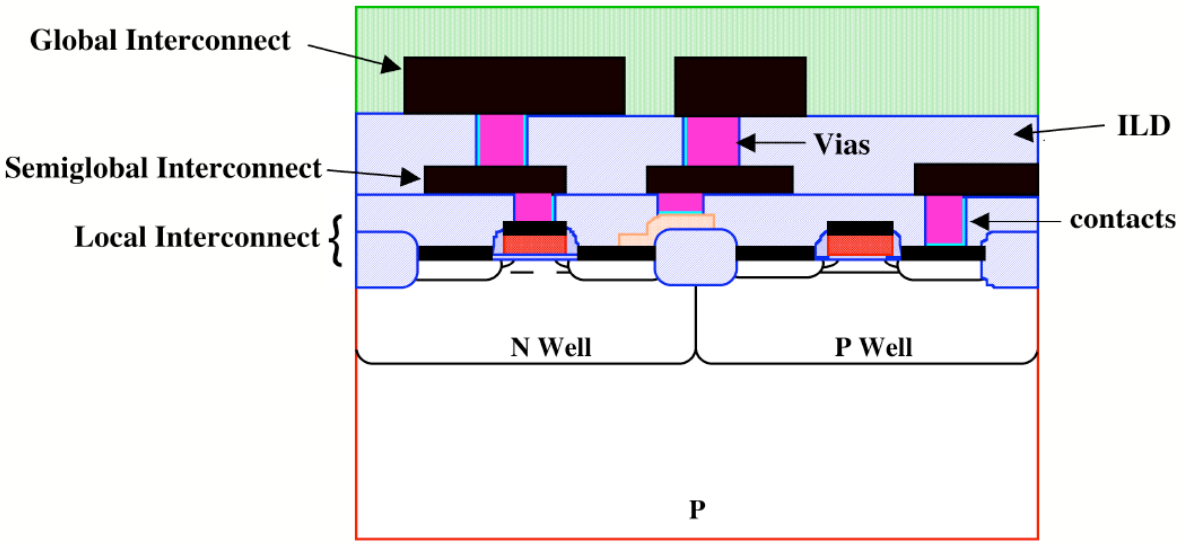


Fig. 1.3. Connections between different types of interconnects [9]

1.2.1 INTERCONNECT CHARACTERISTICS

Interconnects now make up roughly 40–44% of the overall chip area, making them too crucial to overlook [11]. The on-chip link lengthens as technology gets smaller. The parasitic components of the interconnect—that is, the resistance, capacitance, and inductance—increase with the length of the interconnect. An RLC circuit is shown in Fig. 1.4 [11].

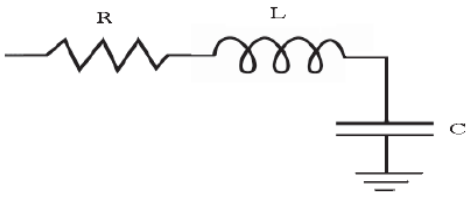


Fig. 1.4. An RLC interconnect circuit [11]

These are the passive devices that control the performance parameters of the interconnect circuit. Additionally, the breadth, thickness, height, and dielectric of the connection are derived from its geometry. The interconnect geometry has a significant impact on the values of these parasitic components as well as the performance of the delay and power. The interconnect delay is commonly affected by the resistive and capacitive parasitic. However, when a change occurs in the width of the wire, the delay also gets affected. A decrease in width of an interconnect increases the delay in an interconnect. Nanotechnologies require more frequency to operate which can further increase the power consumption in the circuits. The wire should ideally only be used to link functional pieces and not impact the functionality of the design. A wire that has equal potential at both ends experiences instantaneous voltage changes at one end and appears at the other without any delay. Desired material qualities for a connection include [12]:

i. Low resistance to electricity
ii. Low intermetal dielectric (IMD) constant, or low capacitance (for minimal RC delay, cross talk, and power loss)
iii. Strong resistance to electromigration
iv. The material's ease of deposition in thin film form
v. Capacity to endure the high heat and chemicals needed for the fabrication process
vi. Stable structures of contact
vii. Conformity to SiO2-based insulating films
viii. Minimal surface roughness and internal stress
ix. Simple etching with plasma techniques
x. Compatible operation with every other semiconductor process
xi. Inexpensive

When VLSI technology decreases, the size of interconnects (wires) also decreases by the value known as "scaling factor (s)". The scaling factor, which reduces the dimensions of interconnects, is an integer. Generally, scaling primarily affects three characteristics of wires: resistance, capacitance, and inductance [13]. Since, the geometry of interconnect becomes important for different nano technologies, their parasitic components can be described as:

a) *Resistance* – A material's resistance is its ability to block the flow of current. Once the dimensions of a material are known, calculating or predicting its resistance is not too

difficult. The resistance of the connection for a rectangular cross-sectional area is given by Eq. (1.1).

$$R = \frac{\rho L}{TW} \tag{1.1}$$

Where ρ is the resistivity, L is the length of the interconnect, T is the thickness and W is the width of the interconnect. Initially, aluminium material was used for making interconnects but as the technology upgraded manufacturers moved to copper material as it provides low resistivity and high electrical conductivity than aluminium. Due to high electrical conductivity and low resistivity, copper interconnects show less amount of resistance as compared to aluminium. Resistances allow current to flow through them, which lowers voltage and weakens signal levels. Additionally, wire delay (τ) is proportional to wire resistance that is τ=RC. The RC effect dominates the delay for lengthy interconnects due to the dependence of delay on the square of length of the interconnect. Although the resistance of an interconnect has up to now been assumed to be linear and constant, at very high frequencies, another element known as the skin effect becomes significant. When high frequency current begins to flow on the connecting wire's surface, the resistance becomes frequency dependent. The current density falls off exponentially as moves deeper into the wire, causing the effective cross-sectional area to drop and the resistance to rise. The signal going across the connecting wire is distorted as a result of the additional attenuation brought on by this higher resistance. Skin effect, however, only becomes an issue with broader interconnects [14]. Since, the interconnects are termed as short and long, their lengths can be scaled down as well with a certain scaling factor S as the technology scales down from micro to nanometres. Short wire length scales down with technology scale down but this does have any effect on the increase of interconnect delay. This is because due to the reduced cross-sectional area of the conductor, the wire's resistance increases by a factor of 1/s, while its capacitance reduces due to its reduced surface area. As a result, the delay never changes. Whereas for the long interconnects, length increases. This is because of the increase in the metal layers in the chip forcing the global interconnects to increase in length to connect up all the areas of devices. Increase in length means increase in resistance of the global interconnect eventually increasing interconnect delay. The net interconnect latency of the circuit will depend on the particular circuit structure and line length distribution. What matters are the patterns that these and other studies indicate will emerge: Although the gate delays will continue, the global interconnect delays will increase and have a greater influence on the

circuit performance, and the local interconnect delays remain roughly the same. "R" scales by (1/s) for short wires, while "C" scales by (s). As a result, the RC delay for short wires remains unchanged, indicating that they have the same capacity to transmit high frequency signals. Rise in the value of resistance can arise reliability issues in the circuits such as electromigration. During practical operation, a chip may reach temperatures beyond 100 degrees Celsius. The loss of power at high frequencies and the resulting dissipation of heat causes a rise in temperature. An increase in temperature promotes the diffusion of solid-state metal ions. Electro-migration results from momentum transfer between electrons and ions in metal interconnects, which is induced by the scattering of moving electrons with the ions. The term "electron wind" is occasionally used to describe this ion-electron interaction. The wire breaks or shorts to another wire as a result of this. A gap in the interconnects in this kind of scenario may result in an open circuit, or chip failure. Electromigration is one of the biggest and most enduring threats to the dependability of interconnects [15]. Apart from electromigration other reliability issue can be ohmic voltage drop also known as IR drop. An ohmic voltage drop caused by current passing through an actual wire lowers the signal levels. The voltage's impacted value modifies the logic levels and lowers noise margins in relation to the supply terminals' distance. The system's performance is further impacted by IR dips on the supply network. A slight decrease in supply voltage has the potential to result in a notable rise in delay [15].

b) *Capacitance* – Interconnect capacitance modelling for contemporary integrated circuits is a challenging task. Like resistance, capacitance is also dependent on the interconnect's geometry, as well as the separation and distances from other wires above and below. Fig. 1.5 displays the fundamental capacitance components used in the interconnect investigations.

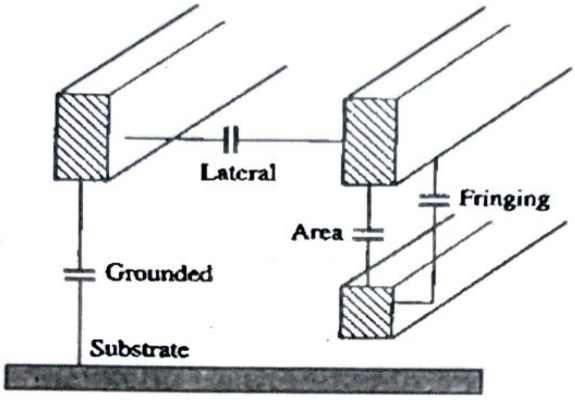


Fig. 1.5. Interconnect capacitance [16]

The initial capacitance is the ground capacitance, which is present between a line and the substrate. Deep sub-micron technologies are generally indifferent to it. The second capacitance is the lateral capacitance that forms between two metal lines on the same layer. The main capacitance in the connected circuit is what's generating the noise and delays. Area capacitance, or third capacitance, is the result of the overlap of two connecting lines on distinct metal layers. Finally, there is the fringe capacitance that develops across different surfaces and edges between two crossing lines. The coupling capacitance is made up of the three capacitances: lateral, fringe, and area capacitance. Over time, ground capacitance decreases and lateral capacitance is the main cause of the coupling capacitance increase. Additionally, the electrical phenomenon connecting wires in a specific area within the area of interest is known as coupling capacitance. Three different types of capacitances are typically seen in an interconnection arrangement, and each one is crucial to the extraction of capacitance as a whole. Also, these capacitance extractions depend upon the spacing between the interconnect lines. The easiest component of capacitance to compute is the area capacitance per unit length. The capacitance can be modelled by parallel plate capacitor model with a dielectric constant as expressed by Eq. (1.2) [16].

$$C_{area} = \frac{\varepsilon}{t}(WL) \tag{1.2}$$

where W is the wire's width, L is the length of the wire, ε is the dielectric's permittivity, and t is the dielectric's thickness. As width reduces with technology scaling, the area capacitance reduces linearly. For lateral capacitance and fringe capacitance, separation between the two interconnect lines must be considered. The lateral capacitance is inversely proportional to the spacing between the interconnect lines and can be expressed by Eq. (1.3) [16].

$$C_{lateral} = \frac{\varepsilon}{S}(TL) \tag{1.3}$$

Where S is the spacing between two lines, T is the wire's thickness and L is the interconnect length. Hence, larger the spacing less will be the lateral capacitance and can be ignored. However, if the spacing among the interconnect lines is less, lateral capacitance is to be considered. Similarly, the fringe capacitance can be expressed by the Eq. (1.4) [16].

$$C_{fringe} = \epsilon \ln\left(1 + \frac{T}{H}\right) \tag{1.4}$$

Where *T* is the thickness and *H* is the height of the interconnect. For densely packed interconnects, fringe capacitance is zero whereas for widely spaced interconnects, there remains a fringe capacitance at every edge. Since, thickness and height are already fixed by the technology, this capacitance becomes almost independent of the geometry. Because interconnect delay is more important than gate delay, the DSM regime emphasises the precision of parasitic extraction of the interconnect impedances. Typically, two- or three-dimensional extraction is required. Accurate capacitance values can be obtained with a 3-D field solver like Fast Cap, but it comes with high latency and memory requirements. With increasing integration, the number and geometric complexity of the on-chip interconnects increase dramatically. As such, it is not feasible to use a field solution throughout an entire IC. Interconnect capacitance is made up of the coupling capacitance between neighbouring interconnects in the same layer, Cc, and the capacitance between the interconnect and adjacent metal layers or substrate, Cg. In the DSM regime, it is expected that Cc will surpass Cg as the aspect ratio rises and the wire spacing falls. Adjacent layers are typically considered a ground plane for capacitance extraction in early stages of connection design and analysis. Capacitance as a parasitic component is also prone to some reliability issues such as coupling capacitance. In the integrated circuits, every wire is connected to a grounded substrate and nearby wire on the same and adjacent layers. Certain capacitive components are connected to other wires with voltage levels that fluctuate dynamically. Such floating or fluctuating capacitors negatively impact the circuit and produce crosstalk. The charged capacitance determines how long it takes for a signal to go through a wire. Increased dynamic power translates into increased capacitance. The increasing source of noise in delay estimation is coupling capacitance. Other signal integrity issue can be crosstalk. It happens as a result of an unintended coupling between a network node and a nearby signal cable. A source of noise is created as a result of the disruption. At present switching speeds, the predominant consequence is capacitive cross-talk. The impedance of the line being studied affects the possible effects of capacitive crosstalk. Noise may restrict the operation and performance of the design. The influence of noise may reduce the design's operating frequency and result in malfunctions. Cross-talk might result in a hold violation or setup.

c) *Inductance* – Interconnect circuits experience an inductance factor when technology scales down and clock frequency rises. It is mainly observed in wide wires used for clock distribution network. Until recently, the transmission-line effects in CMOS VLSI were not a significant concern since, in most situations, the gate delay resulting from entirely or

primarily capacitive load components outweighed the line delay. However, the intrinsic gate delay components tend to reduce considerably as manufacturing technologies advances to finer (sub-micron) design standards. The manufacturing devices, yield, and packaging technique are the primary determinants of chip size. Interconnect delay becomes more significant with sub-micron technology because of the unchanging chip size and worst-case line length. Furthermore, transmission line effects and signal coupling between adjacent lines intensify with decreasing metal line widths. Inductance is an electromagnetic phenomenon, and its effects aren't always restricted to a certain area. Additionally, it becomes noticeable when the switching frequency rises to the GHz region and the resistance decreases. If not managed appropriately, this component can lead to several problems in the interconnect circuits, such as overshoot and impedance mismatch. It is far more difficult to extract the connection inductance than resistance or capacitance. Because inductance can only be determined for a closed current loop and not just for a wire segment, the inductance problem is very challenging. The area of the loop determines the inductance of the loop. It is not enough to know the current's forward direction; one must also identify the return path, which is difficult to do for the majority of signals. Local interconnects in lower metal layers have a lesser impact on inductance than wide global interconnects in top metal layers. Adjacent layers can no longer be regarded as a ground plane as in capacitance extraction because the wires in them are typically orthogonal. The long-range inductive coupling effects are another factor contributing to the challenge of inductance extraction. In addition to introducing inaccuracy, artificially limiting the inductance extraction to close geometries may lead to unstable models. Inductance can be of two types - self-inductance or mutual-inductance. When current flows via a conductor, a magnetic field is produced, which leads to inductance parasitics. Any conductor that has current flowing through it produces a magnetic field. The same metal may then experience self-inductance from this magnetic field, or another metal may experience mutual inductance when it crosses the magnetic field [17]. The interconnect impedance expressed due to the resistance and inductance present can be seen as Eq. (1.5).

$$Z = R + j\omega l \tag{1.5}$$

Where Z is the interconnect impedance, R is the interconnect resistance, j is the complex number, ω is the operating frequency and l is the inductance value. The inductor can be

considered a short-circuit for low-frequency operation while operating with direct current because there is no voltage drop across it. However, in high-speed designs the rate of change of current is increasing rapidly with respect to time. Therefore, it becomes essential to address inductance effect at package points and power distribution systems. At high operating frequency, RC interconnect lines start to behave like a transmission line under certain circumstances that can change the delay equation for the circuits. The interconnect impedance as mentioned in Eq. (1.5) can determine if the interconnect will act as a RC interconnect line or an RLC interconnect line. If R >> $j\omega l$, then the interconnect acts as an RC interconnect line where inductance is negligible and can be ignored. If R << $j\omega l$, then the interconnect acts as an RLC interconnect line where inductance value cannot be ignored and will show significant effect on the signal line. But when considering importance of inductance, it is necessary to consider both wire resistance as well as buffer on-resistance driving the wire. In most cases, the buffer resistance is large and dominates. Therefore, self-inductance can be ignored for most of the signal lines on the chip. However, if the buffer is large and the wire is wide, inductance effects will be noticeable. This is prominent in most of the clock lines. Further, the transmission lines can be lossy as well as lossless depending upon the parasitic components present in the wires. The lossless transmission line includes inductance and capacitance values but no resistance value. It is driven by a supply voltage source and a source resistance. Considering no interconnect resistance, the characteristic impedance for lossless transmission line can be expressed by Eq. (1.6) [16].

$$Z_o = \sqrt{\frac{L_{int}}{C_{int}}} \tag{1.6}$$

Where Z_o is the characteristic impedance, L_{int} is the per unit length inductance, and C_{int} is the per unit length capacitance. When an input is given, the response depends upon the impedance and source resistance values. That is when the resistance is greater than the impedance, RC effect dominates with large propagation delay and rise time. When resistance is less than the impedance, inductance effects will be important to address as they obtain an oscillatory response with short propagation delay and rise time. For lossy transmission line, distributed effects are taken into account. This means that the length of interconnect becomes equally important to determine the effects of inductance. As a

signal propagates down the wire, it experiences attenuation due to wire resistance. When it reaches the end of the wire, it reflects off the load impedance and travels back to the source. This reflected signal also gets attenuated and leads to ringing effects in the wire. Due to signal attenuation, it becomes difficult to locate inductive effects in long wires. Therefore, it becomes necessary to determine a critical length at which the inductance effects can be observed and rectified. The maximum length for an interconnect with inductive effects can be expressed by Eq. (1.7) [16].

$$l_{max} < \frac{2}{R_{int}}\sqrt{\frac{L_{int}}{C_{int}}} \tag{1.7}$$

Where l_{max} is the maximum interconnect length, R_{int} is the per unit length resistance, C_{int} is the per unit length capacitance, and L_{int} is the per unit length inductance. If the resistance per unit length increases the length over which inductance is important decreases. On the other hand, the buffer's output signal's transition time also regulates the transmission line impacts. If the round-trip time of the signal is short as compared to the rise time of the signal, then no transmission line effects can be seen. The round-trip time can be expressed by Eq. (1.8) [16].

$$t_{round-trip} = 2t_f = 2l\sqrt{L_{int}C_{int}} \tag{1.8}$$

Where t_f is time-of-flight. The transmission line effects are seen if the rising time is less than twice the time-of-flight. So, the minimum wire length can be expressed by Eq. (1.9) [16].

$$l_{min} > \frac{t_r}{2\sqrt{L_{int}C_{int}}} \tag{1.9}$$

Where l_{min} is the minimum wire length and t_r is the rise time. The critical interconnect length for inductance effects to be noticeable can be given by combining Eq. (1.7) and (1.9) and expressed by Eq. (1.10) [16].

$$\frac{t_r}{2\sqrt{L_{int}C_{int}}} < l < \frac{2}{R_{int}}\sqrt{\frac{L_{int}}{C_{int}}} \tag{1.10}$$

For delay calculations, only considering interconnect parasitic components are not sufficient. Buffer resistance must also be considered for accurate results.

Mutual inductance can be the most problematic inductance since it causes noise and delay on neighbouring lines in unexpected ways. Mutual inductance is determined as the time varying current in one line proposing a voltage drop in the second line. When current flows in one-line, mutual inductance induces a return current in the other line. So, the voltage drop on each line will be the sum of self-inductance and mutual inductance with the other line. These effects can be large and can create functionality errors which can be recurring in nature. Buses are more prone to mutual inductive effects. To keep inductive effects in check different solutions can be considered such as choosing a definite critical length for interconnect or the shielding techniques. However, reliability issues can be observed for inductive effects when becomes prominent such as Ldi/dt voltage drop. This issue affects the timing and functionality of gates connected to power lines if the drop becomes too significant due to inductance.

1.2.2 INTERCONNECT MODELS

In the procedures of circuit design and verification, interconnect modelling is essential. A precise and effective connection model can greatly improve these procedures. Modelling of interconnects can be done for single interconnects as well as coupled interconnects whose parasitic components depend upon the length of the interconnect. Models of single and coupled interconnects are explained as:

a) *Single Interconnects* - Numerous interconnect network simulation tools are built upon the single interconnect concept. Over the past few decades, a variety of on-chip connection models from distributed transmission lines to lumped C/RC/RLC models have been presented. When choosing the right model, efficiency and accuracy must be bargained. Single wires can be implemented using two types of models. These models not only help in decreasing the complexity of interconnect design but also help in simplifying the performance parameters of the circuit. Lumped and Distributed models are the two types of single interconnects that can be explained as:

i. Lumped model – With the advancement of deep submicron technologies like 7nm and 5nm, metal wire widths have decreased dramatically, leading to a rise in resistance.

Interconnecting cannot be modelled as a single capacitive load; rather, a resistance must also be modelled. In this case, RC lumped model comes into play. This model is used for short wires because only single parasitic component is dominant. In other words, if it is a lumped RC model then it will consist of a resistance whose value is lumped into one single resistance (*R*) and a capacitance whose value is lumped into one capacitance (*C*). Analysis of lumped network with large number of resistances and capacitances become complex as it contains many time constants like poles and zeroes. To solve this issue, Elmore Delay model is studied and utilized. Further, lumped model can be divided into three types of interconnect structure as shown in Fig. 1.6: –

a. L-model – This is the most basic model, consisting of a resistance and a capacitance, where the delay is expressed as the wire's product of R and C.
b. π-model – In this approach, the delay is the product of the wire's R and C/2 values, and the capacitance is divided in half.
c. T-model – This model divides the resistance value in half and calculates the delay as the product of the wire's C and R/2.

The advantage of lumped interconnect is that it is the simplest form of model but its disadvantage is that it is pessimistic and inaccurate for long interconnects.

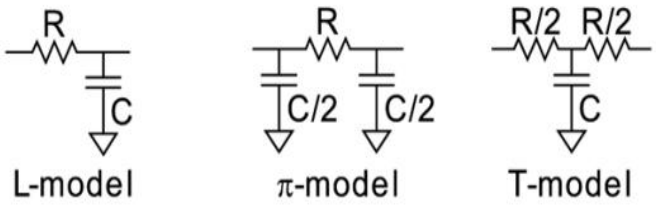


Fig. 1.6. Lumped RC models [18]

ii. Distributed model – This model is used for long wires because the entire resistance (*R*) and capacitance (*C*) of the wire is distributed along the entire length of the net as shown in Fig. 1.7.

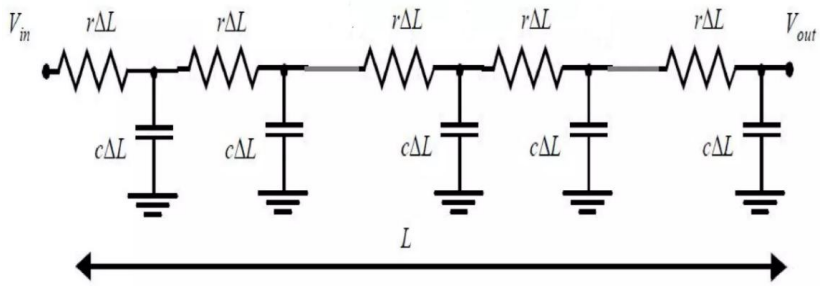


Fig. 1.7. Distributed RC model [19]

Signals travel more slowly along global and intermediate interconnects than they do through gates. In this case, it is important to consider the dispersed features of the connection. This advantage of distributed model is that it is used for long wires and provide accurate results but the disadvantage is that it is complex and does not provide close form solution. To solve this problem, Elmore delay estimation is used if the distributed line is approximated into lumped line.

b) *Coupled Interconnects* - Because of the often-utilised bus structure, modelling coupled interconnects requires specific consideration during the circuit design process. Decoupling the systems into separate interconnects and then applying single line models to each of these interconnects provide a general solution for connected multiconductor systems. However, de-coupling long wires into single wires increases the computational complexity [20].

1.2.3 INTERCONNECT DELAY ESTIMATION

The size of the parts that make up a system-on-chip (SoC) has decreased significantly with nanometre technology. This discovery indicates that modern technology has significantly shrunk in size, putting all of its components close to one another. Size reduction is a crucial component of contemporary technology since consumers want compact, portable devices. However, there are drawbacks to compact and portable devices, such as lag, overheating, and dependability problems. The production process is getting more complicated as the advanced technology nodes' physical dimensions decrease and they are getting closer to what is believed to be the fundamental operating limit of the device. Furthermore, no further requirements reductions are possible for the components because they are application-specific. To facilitate component connectivity, the wire designs simply need to be improved. Metal lines called interconnects are used to establish electrical connections between the active components in a circuit to transfer and distribute power and signals. However, interconnect size likewise lowers as chip size does. Chip delay, power consumption, and noise are mostly caused by interconnect structures, which are getting smaller due to the increased need for high speed. Nonetheless, the shape of interconnects can be used to control these performance metrics. Generally rectangular in design, interconnects have the proper geometry with width (W), thickness (t), height (h), and spacing (s) as shown in Fig. 1.8. The insulator thickness, or height of interconnect, measures the separation between layers, while the spacing measures the separation from adjacent conductors. The technology employed and

the interconnect's length determine the interconnect's geometry. Furthermore, the significance of the interconnect geometry should not be understated, since it can regulate the circuit's RC delay phenomenon.

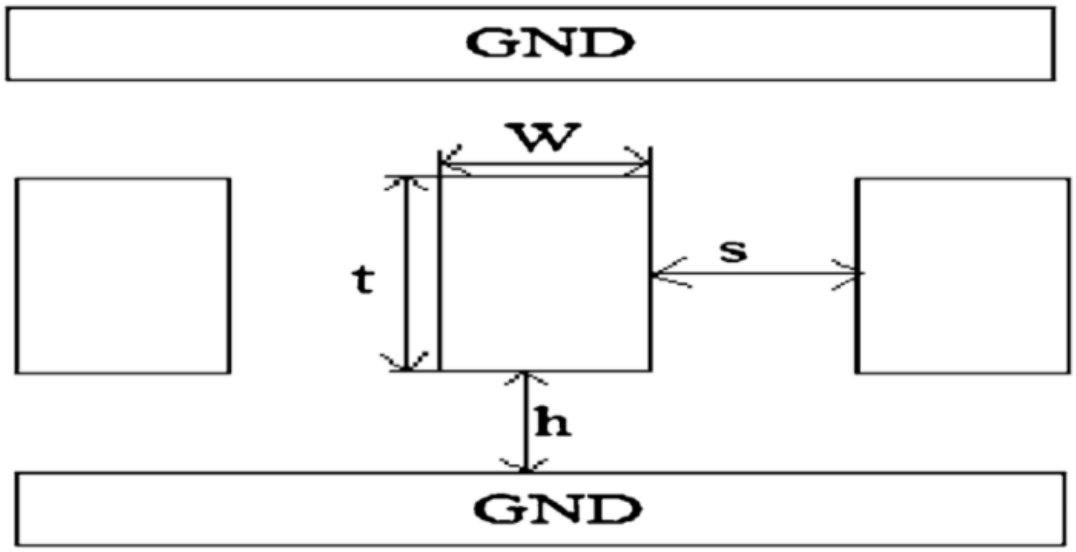


Fig. 1.8. Interconnect geometry

Interconnects are the fundamental unit of signal connection between chips or between chips on a printed circuit board (PCB). The layout and design of an integrated circuit's interconnects have a direct effect on its functionality, dependability, efficiency, performance, and total fabrication yield. Several factors are taken into account while choosing the composite material for the interconnects, such as electrical conductivity, mechanical and chemical compatibility, and fabrication challenges. Integrated circuit performance is increasingly dependent on the overall signal, power, and thermal integrity of their high-speed interconnects.

Interconnects are required to shrink in size in conjunction with transistors' constant reduction. At this point, the RC problem represents a major obstacle that conventional copper interconnects must overcome to scale further. When parasitic components are looked individually, the electrical resistance (*R*) of a material, indicates how challenging it is to flow electrical current through a specific cross-section of that material. The capacity of a material to hold an electrical charge is known as its capacitance (*C*). Since device speed is inversely proportional to resistance and capacitance (*RC*), low RC is required to develop fast processors. When considering resistance of the interconnect, device speed is slowed because higher-resistance lines carry less current. This is due to the fact that increased resistance slows down the flow of electrons, making it take longer to reach the threshold voltage or

minimum charge at a transistor's "gate" in order to switch it on. The difficulty with interconnect scaling is avoiding becoming a bottleneck and losing that performance gain by decreasing the flow of electrons between transistors, even as transistor speed increases with scaling. The insulating dielectric substance surrounding the metal lines and their separation from one another determines the capacitance. Increased capacitance slows down electrons and can lead to unintentional 'cross-talk', in which a voltage change in one metal line affects a nearby line's signal, disrupting the device. The development of "low-*k*" dielectric materials has greatly reduced capacitance in addition to maintaining an appropriate distance between lines. There are other ways to get lower values, however, as the *k* value drops, the resulting ultra-low-*k* films become more brittle, which presents more difficulties for manufacturing.

The simplest and easiest way to deal with the interconnect delay is to study Elmore Delay Estimation. By multiplying the resistance in the path to the i^{th} node by the capacitance at the branch's end, the Elmore delay analysis model calculates the delay from a source to one of the leaf nodes [21]. It provides a simple delay analysis in place of the tedious numerical integration and differential equations of an RC network. Eq. (1.11) [16] can be used to express the Elmore delay.

$$\tau = \sum_{k} R_{ik} C_k \tag{1.11}$$

Where C_k is the capacitance at node k and R_{ik} is the total of all the resistances from source to node k. Even though Elmore's delay estimates delay more quickly, only the first moments are taken into account, necessitating more development.

1.2.4 INTERCONNECT SCALING AND INTERCONNECTS AS CIRCUIT COMPONENTS

The goal of the semiconductor industry has been to make microprocessors faster and more functional. In the ensuing generations of integrated circuits, transistor cost, integration, and scaling all experienced significant reductions, as predicted by Moore's law. By merging millions of transistors on integrated circuits (ICs) or numerous systems on a chip, devices and interconnects must be aggressively expanded to fulfil the ever-changing requirements of advanced technology. Moreover, systematic transistor scaling has enhanced the functionality of the device. In contrast to devices, interconnects still encounter a major barrier to future scaling. While scaling causes the transistor delay to decrease, the growth of the equivalent

resistance-capacitance (RC) delay is the primary driver of increases in connection losses and declines in signal integrity. Therefore, given that interconnect delay is more important than transistor delay, it is evident that interconnect delay cannot be disregarded for next-generation technology. Consequently, more thorough research should be done on the interconnect's performance for high-speed and low-loss devices.

Early on in the creation of ICs, the connection capacitance was the only factor taken into account when estimating an IC's total latency. Due to the aggressive down-scaling of Cu interconnect dimensions has led to exponentially increased resistivity, which was referred to as the “size effect” [22]. Additionally, a traditional method was used for many years to study the signal delay of interconnects in both analogue and digital circuits. The straightforward *RC* model, however, quickly became overly optimistic at faster working speeds. Because less resistant materials are used in current ICs, the inductive effect also plays a significant role that needs to be accurately taken into account. Due to energy dispersion, attenuation, and scattering, all materials show conductor and dielectric loss. The conductor loss resulting from signal attenuation, higher current density, crystal lattice defects, and scattering is represented by resistance (*R*), capacitance (*C*), and inductance (*L*). On the other hand, conductance (*G*) is used to model the dielectric or shunt loss, which is caused by energy dispersion in the substrate and dielectric medium.

1.3 SOFTWARE USED

LTSPICE software was used to run all of the simulations on a system with an Intel(R) Core (TM) i7-10700 CPU running at 2.90GHz and 16.0 GB of RAM. Software that is best suited for quicker simulation of power electronics and electronic circuits is called LTSPICE. The online community support for LTSPICE is strong. It is a popular SW tool for simulation that is free, very easy to use, lightweight, and rich in component libraries. It also permits the addition of store-bought components. All users have to do is locate or write the component's SPICE model. Software program called LTSPICE does simulations using SPICE as well, but it does it more quickly and accurately than PSPICE by utilising superior algorithms, techniques, and hacks.

With improvements and models to improve the modelling of analogue circuits, LTSPICE is a robust, quick, and free SPICE simulator programme that also functions as a schematic capture tool and waveform viewer. Through the use of its graphical schematic capture

interface, schematics can be investigated and generate simulation results that can be further examined using the integrated waveform viewer.

1.4 DATA SET AND PERFORMANCE PARAMETERS

The values of parasitic components of the VLSI interconnects depend upon the length and the geometry of the wire. All the values of parasitic components are derived from Predictive Technology Models (PTM) [23] from interconnect length of 1mm to 10mm. A new generation of Predictive Technology Models (PTM) is in development for technology nodes ranging in size from 130nm to 32nm.

These predictive model files can be scaled to accommodate a broad range of process variables and are compatible with common circuit simulators, like SPICE. Competitive circuit design and research can begin using PTM even prior to the complete development of modern semiconductor technology. These modal files determine the geometry of the interconnect design for different technology nodes currently being used in the industries. The technology node used for the evaluation of interconnect parasitic components for different length is 45nm technology and the geometry of wires used is listed in Table 1.1.

Table 1.1. Wire geometry for 45nm technology

Parameters	Values (μm)
Width	0.2
Height	0.1
Spacing	0.4
Thickness	1

The interconnect length considered ranges from 1mm to 10mm long with their respective resistance, capacitance and inductance values. Table 1.2 shows the values of total resistance and capacitances concerning different interconnect lengths evaluated from predictive technology models [24].

Table 1.2. Parameters values concerning interconnect length [24]

Length (mm)		1	2	3	4	5	6	7	8	9	10
Parameters	Capacitance (fF)	191	383	575	767	959	1150	1342	1534	1726	1918
	Resistance (Ω)	110	220	330	440	550	660	770	880	990	1100

It is also possible to compute the individual resistance and capacitance values for both lumped and dispersed networks while taking uniform distribution into account. Table 1.3 and 1.4 shows the individual parasitic components values per unit length for lumped and distributed network respectively.

Table 1.3. Individual parasitic components value concerning interconnect lengths for proposed lumped RC structure [24]

Length (mm)		1	2	3	4	5	6	7	8	9	10
Parameters	Capacitance (fF)	191	383	575	767	959	1150	1342	1534	1726	1918
	Resistance (Ω)	27.5	55	82.5	110	137.5	165	192.5	220	247.5	275

Table 1.4. Individual parasitic components value concerning interconnect lengths for proposed distributed structure [24]

Length (mm)		1	2	3	4	5	6	7	8	9	10
Parameters	Capacitance (fF)	95.5	95.75	95.83	95.875	95.9	95.83	95.85	95.875	95.88	95.9
	Resistance (Ω)	27.5	27.5	27.5	27.5	27.5	27.5	27.5	27.5	27.5	27.5

The distribution of total resistance and total capacitance values per unit connection length is known as a uniform distribution. These measures are used to assess many performance metrics, including power usage and time constant. The interconnects' resistance multiplied by their capacitance value equals their delay. Nevertheless, it varies depending on how the interconnect's length and structure alter. Regarding power consumption, the results of the SPICE simulation are used to estimate the average power usage.

1.5 MOTIVATION

Deep submicron (DSM) technologies cause interconnects to behave differently from resistors, possibly exhibiting parasitic characteristics like capacitance and inductance. The RC delay increases quadratically as the interconnect capacitance (*C*) and interconnect resistance (*R*) both rise linearly with a linear increase in interconnect length. An integrated circuit must have its RC delay decreased in order to operate at a faster pace. Large connection impedance also causes increased power dissipation in addition to increased signal propagation delay. Projections from the International Technology Roadmap for

Semiconductors (ITRS) indicate that connection delay can contribute more than 50% of the delay when the feature size is more than 180 nm [25]. For high performance architectures to achieve timing closure, delay and power optimisation approaches for interconnect are therefore becoming more and more crucial. To lower the power consumption, power dissipation, and timing constant of the VLSI interconnect circuits, the thesis seeks to develop an alternative approach for the VLSI interface for DSM technology. These advancements are primarily driven by portable applications, like notebook computers and portable communication devices, that demand high throughput at minimal power dissipation. In the majority of these situations, achieving high chip density and high throughput—two equally challenging objectives must coexist with the need for minimal power consumption.

1.6 RESEARCH GAPS

From the literature review, it is evident that different tools and techniques are applied and studied for different technology nodes. It is seen that authors have not only focused on applying various techniques to boost the performance of the interconnect circuits but also focused on the structure of interconnects by adding extra components of the circuits. The performance of the interconnect structures was seen to be improved however; certain gaps can be identified:

i. **To reduce overall resistance of an interconnect circuit** –

With technology scale down, the wire geometry also changes which ultimately affects the resistance of the circuit. Rather than shifting to new material, techniques to reduce resistance is more important with the decrease in technology node.

Objective I: Design and Implementation of RC global interconnects with different lengths.

ii. **To optimise overall power performance for long wires** –

The main focus in the literature review was to minimize the timing constant of the circuits. Some presented techniques for less power consumption. However, there still remains the need for less power dissipation which causes heat generation ultimately leading to system failure.

Objective II: Design and Implementation of RC global interconnects with Buffer Insertion Techniques.

iii. To reduce area, and delay for interconnect circuits –

As seen in literature review, performance parameters were improved by inserting buffers in between long wires. However, increase in area was observed. To improve latency, throughput and power consumption in an interconnect circuit current mode signalling technique was studied and implemented to the proposed interconnect circuit with reduced resistance.

Objective III: Design and Implementation of RC global interconnects with Current Mode Signalling Technique.

iv. To reduce inductive effect in interconnect circuits -

Although, improving all the parameters still inductance effects can be seen in the interconnect circuits with the reduction in technology. New interconnect circuit was implemented and simulated by reducing the inductance parasitic component instead of introducing different parameters to the interconnect circuits.

Objective IV: Design and Implementation of RLC global interconnects.

1.7 RESEARCH OBJECTIVES

After reviewing and identifying research gaps, following objectives are formed –

Objective I: Design and Implementation of RC global interconnects with different lengths.

Objective II: Design and Implementation of RC global interconnects with Buffer Insertion Techniques.

Objective III: Design and Implementation of RC global interconnects with Current Mode Signalling Technique.

Objective IV: Design and Implementation of RLC global interconnects.

1.8 THESIS ORGANIZATION

The thesis's remaining chapters are arranged as follows:

Chapter 2 presents a literature assessment of various interconnect topologies and technologies/techniques used.

Chapter 3 describes a novel interconnect circuit architecture (H-tree) for connecting lengths ranging from 1mm to 10mm. Theoretically, the parasitic components of both lumped and distributed networks are calculated, and Elmore Delay Estimation is used to optimise the networks' delays for innovative interconnect structures. Difference between uniform and non-uniform distribution is presented. Lastly, performance parameters are evaluated using LTSPICE and are verified theoretically using different input supplies i.e. pulse and ramp input supply.

Chapter 4 provides an overview of the traditional buffer insertion method for delay reduction and signal restoration. The advantages of buffer insertion in linear interconnects are discussed, along with how they are used to reduce delays and noise. This chapter covers the principles of power dissipation, propagation delay, and design criteria. Introduction to Schmitt trigger design is included along with the use of Energy recovery techniques. The use of energy recovery logic for the Schmitt trigger and CMOS inverter circuit employing FinFET technology to reduce power consumption and dissipation is thoroughly discussed. Further, buffer insertion technique using energy recovery logic implemented for the novel interconnect circuit designs is studied. Additionally, it is demonstrated how buffer insertion is growing more and more resource-intensive in emerging technologies, turning it into a cumbersome procedure. The final section discusses the space and power consumption limitations of buffer insertion technology.

Chapter 5 provides a detailed explanation for Current Mode Signalling (CMS) Technique for interconnect circuit designs. Advantages and Disadvantages of CMS technique is drawn over Buffer Insertion technique for novel interconnect circuit designs. Further, area reduction and better performance results are procured and concluded with the limitations of the said technique.

Chapter 6 provides an introduction to inductance as a parasitic component for interconnect circuits. Simulation explanation is provided for the introduction of inductance as a parameter. Further, delay expression is evaluated for RLC transmission line. Performance parameters are evaluated and explained along with the importance of RLC interconnect lines with decrease in technology nodes.

Chapter 7 draws the conclusion and future scope of the thesis.

CHAPTER 2
LITERATURE REVIEW

CHAPTER 2: LITERATURE REVIEW

The following section provides a thorough overview of published research on the subject of the study with a defined goal and approach. A study of the literature covering the years 1990–2024 has been completed while keeping in mind the difficulties and problems raised concerning this subject. The survey helps identify the needs and research gaps. VLSI Interconnects are currently a broad and well-liked area for research.

For modern low power technology, it is important to combine different blocks into an integrated circuit while keeping low power consumption and delay. This can be done using various interconnect techniques and models and their limitations can also be drawn [11]. Some of these models are mentioned in Fig. 2.1. A brief explanation is provided concerning the published work. This chapter is divided into four parts: VLSI Interconnects with Elmore delay model, Buffer insertion techniques in long interconnects, Interconnects with current mode signalling technique, and RLC interconnect lines.

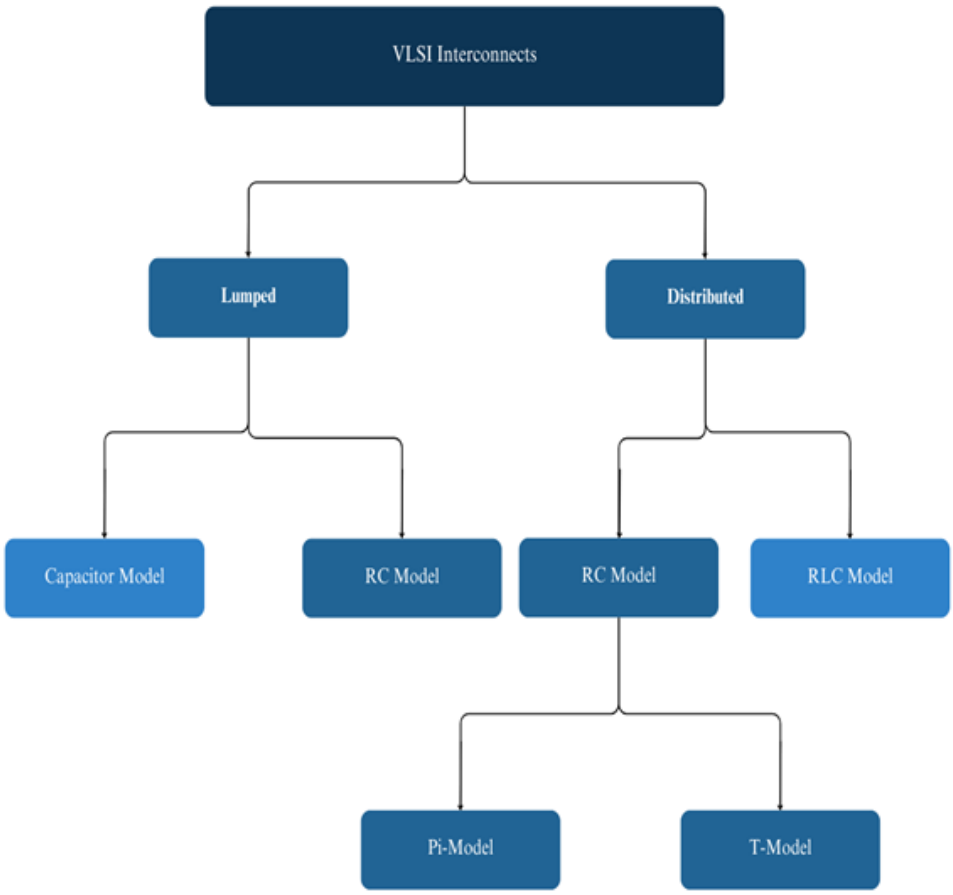


Fig. 2.1. Various interconnect models [11]

2.1 VLSI INTERCONNECTS WITH ELMORE DELAY MODEL

There is a need to focus on the importance of VLSI interconnects in CMOS technology and about the details concerning these wires, their types, different models, wire RC delay and wire metallization [26]. One such model for RC delay is the Elmore Delay Model. It provides with the first moment of impulse response which is commonly referred to as Elmore delay. Since, the focus is on reducing the timing constant of the interconnect circuits certain techniques and modifications can be observed such as Elmore delay as an absolute upper bound on 50% delay of an RC tree to avoid the restriction of delay with input only as step response. A lower bound on delay is also presented using Elmore estimation and second moments of impulse response [27]. Further, four interconnect delay models based on Elmore delay theory are discussed which can be used for an RC tree [28]. Also, a non-linear relationship between SPICE simulations, experimental results and Elmore delay model for N stages of RC ladder circuit can be observed by applying Least Mean Square method on SPICE simulation results [29]. Extending the calculation results by increasing the moments of impulse can also be observed for better performance results. A new delay metric employing the first three moments of the normalised homogeneous component of the step response was created by modelling it as a probability density function in terms of the gamma distribution [30]. An impulsive response is suggested. Crucially, it is demonstrated that the table model needed for the distribution function spans a very narrow range of element values, allowing moderate-sized tables to achieve excellent accuracy. This yields a metric with runtime complexity similar to the Elmore delay approximation and accuracy that is similar to that obtained from model order reduction. [31] proposes a D2M, a delay metric for RC trees which is a straightforward function of the impulse response's two moments. Generally, the metric acts as an upper constraint on the real although the error magnitudes are noticeably smaller than for the Elmore delay. Although it is not as exact as h-gamma, D2M is also more accurate than other delay metrics that can be expressed as functions of the initial few moments. Apart from optimising interconnect delay by applying different variations of Elmore delay models, simply wire sizing and layout techniques can also be seen improving the performance results. A new algorithm for interconnection sizing is proposed in [32]. An Elmore delay model is used to solve the wire sizing problem (WSP), and it does not require the crucial. Nodes on leaves are to be specified. First, the issue of finding the ideal wire diameters under delay limits is discussed, and area-delay trade-off curves are displayed. Furthermore, experimental evidence demonstrates that reaching the net's absolute least delay

is a wasteful use of resources; an engineering solution is better served by setting a delay target that is even 10%–15% above the minimum delay. As for routing and interconnect modelling, different techniques are studied. A simple interconnect modelling is seen in Fig. 2.2 [33].

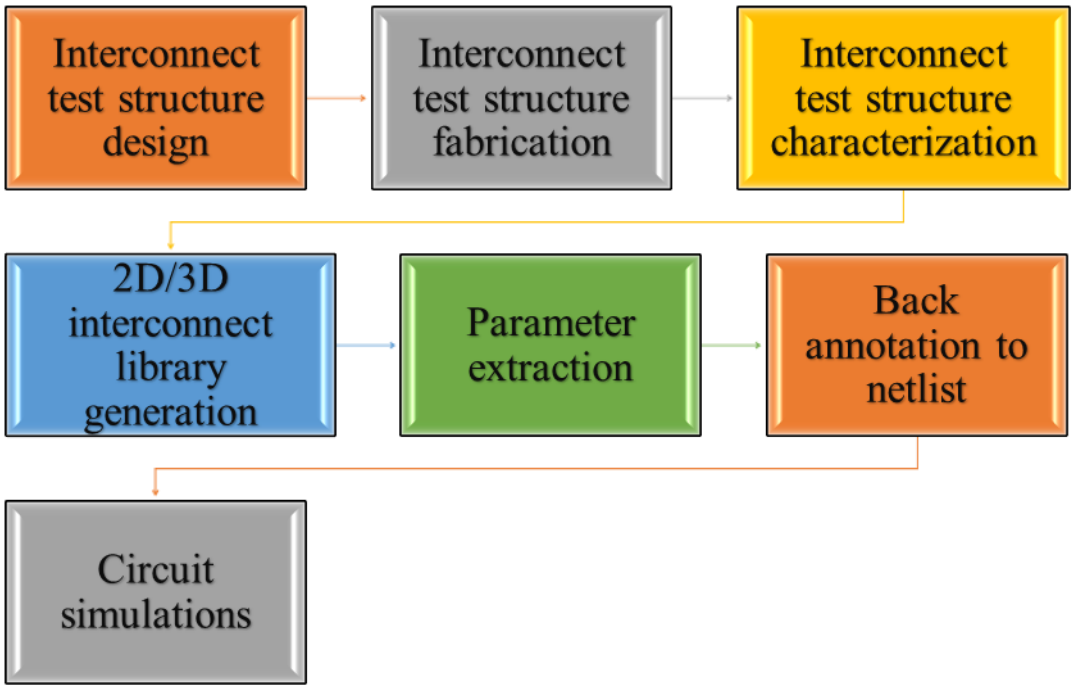


Fig. 2.2. VLSI Interconnect modelling [33]

In the general interconnection modelling flow, the design of the interconnect test structure (ITS) is the first step. Silicon is used to create, measure, and evaluate to derive the material properties (interconnect technology parameters) and connect geometry parameters. The performance of IC circuits is impacted by the large parameter dispersion caused by process variation. Two- or three-dimensional interconnect model libraries are developed based on the characterised interconnect technology parameters (ITP). Layout parameter extraction is done with these interconnect model libraries and device models. Next, they undergo circuit modelling and are re-annotated to the netlist. The overall precision of this flow determines the circuit simulation's correctness. Other than physical interconnect modelling the authors in [33] also explains the concept of interconnect characterization and statistical interconnect modelling. Interconnect characterization explains the concept of long wires and the issues generating in operating these long wires. Since, inductive effects are less than RC effects for few MHz frequency ICs. Yet, for increasing demand for high frequency circuits, more complex geometry and structure will get which becomes too complicated to be simulated by numerical field solvers. The interconnect model library-based parameter extraction

methodology has been created as a solution to the issue and applied in the IC market. Resistance (R) and Capacitance (C) are the basic components required for any interconnect modelling. However, for low frequency circuits interconnect resistance can be considered negligible. To compute the total capacitance of the circuit, using 2-D fringing capacitances and 1-D area capacitances is sufficient. The 3-D fringing is still hardly noticeable. Linking together Quasi-3-D parameter extractors employing 1-D and 2-D interconnect model libraries to carry out parameter extraction. 2-D field solvers based on the Finite-Difference Method (FDM), Finite-Element Method (FEM), or Boundary-Element Method (BEM) provide the 2-D model library. 3-D libraries are used hardly due to various issues related to it. However, a new 3-D library is introduced using Monte Carlo Simulations. These techniques can be used to extract the resistance and capacitance parasitics easily but inductance still remains a problem. After extracting parameters interconnect performance is recorded for issues such as delay and crosstalk because interconnect R and C values are strongly correlated. Authors in [33] explains a worst-case statistical interconnect modelling method to determine values for interconnect delay and crosstalk as shown in Fig. 2.3.

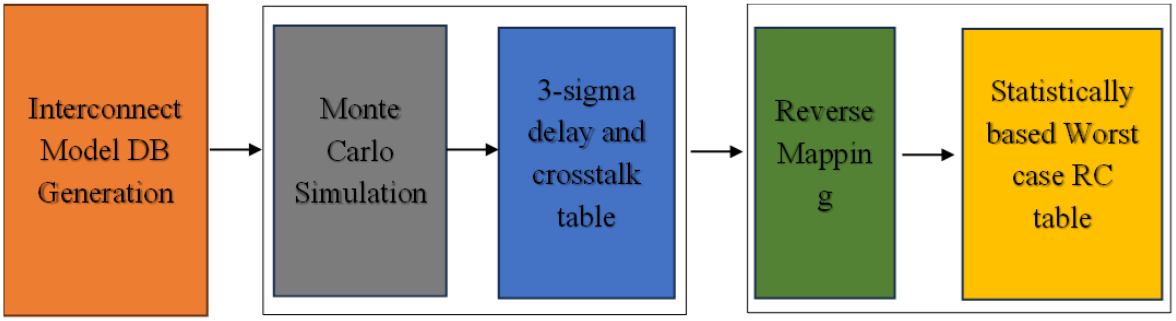


Fig. 2.3. Statistical interconnect modelling [33]

Root-sum-square and skew-corner modelling have been used for worst-case connection modelling. These approaches are overly cautious. The worst-case delay is improved by 20% using the recently created SWIM (Statistically-based Worst-case Interconnect Model generator). In [34], authors present a performance driven layout design for interconnects as shown in Fig. 2.4 with the increasing demand of high frequency long wires. Global interconnect planning and optimisation happen during the floorplan stage, and additional interconnect optimisation happens during global routing. For the past few years, interconnect delay minimisation has been the primary focus of connection modelling and optimisation research. The authors in [34] introduce several widely-used interconnection and driver models as well as several interconnect design and optimisation strategies that have shown to

be highly successful in raising connectivity dependability and performance. The outcomes of the experiments indicate that these optimisation strategies, varying in their efficiency and optimality, have a major effect on the global interconnects' performance.

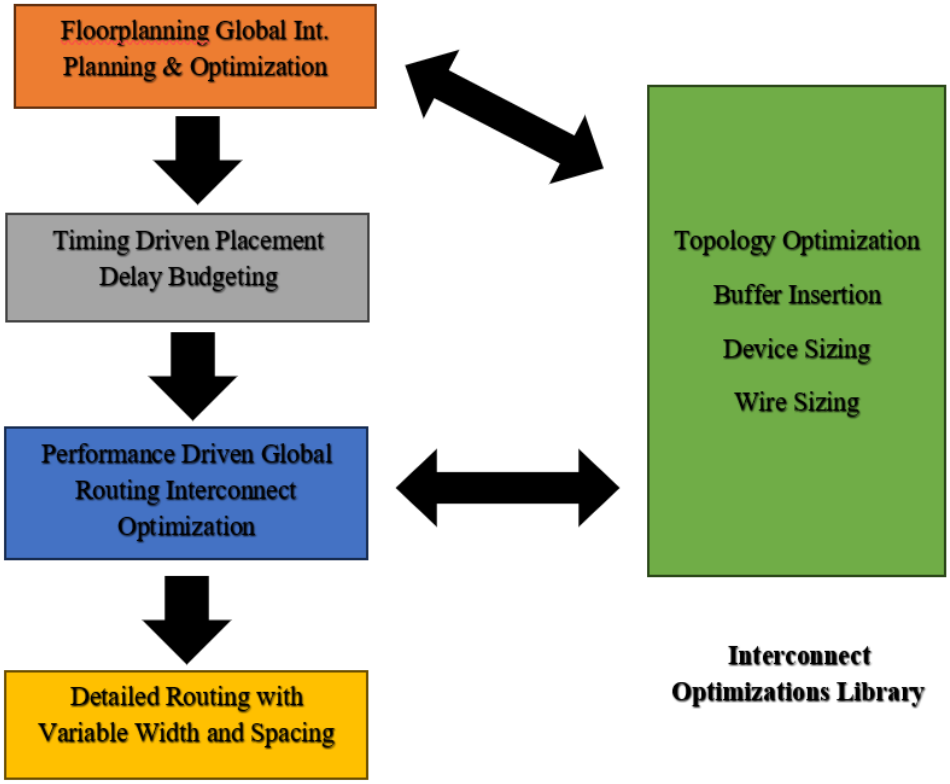


Fig. 2.4. Layout design for interconnects [34]

Applying Elmore delay model has its own limitations when it comes to maintain the speed of the interconnects. Simply re-evaluating it will not solve the issues, since the rise in the resistance of the interconnects is seen. Certain parameters can be considered in addition with the resistance of the wire to alter the structure of the interconnect for different types of interconnect networks such as a new RCG interconnect structure is proposed for generalized interconnect structures using Elmore delay model. The basic idea is to improve the performance parameters by adding conductance into the circuit as an additional parameter [35]. Apart from modelling interconnect with new wire sizing techniques or introduction to new parameters, simply a different input supply can be given to reduce the timing constant in the circuit as well as to conserve power. The ramp as an input supply can be given to the interconnect circuits for better performance results. Using a new method based on solving the diffusion equation and applying reflected diffusion components to account for reflections at the source and load end of the line, authors have analysed finite distributed RC lines under ramp input [36]. There are two methods for calculating the higher-order diffusion

components caused by reflections at the source or load end, one of which is a general recursive equation. In [37], Two straightforward models may be used to assess the propagation delay of a generic RC chain when it has a linear ramp input. The first model is characterised as a piecewise function, whereas the second model is a continuous function. Furthermore, as the rise and fall times of the signal decrease as technology scales, it is important to note that instances where the value is less than 1 are frequent, making the first model the more desirable choice. The suggested metrics were assessed using comprehensive circuit simulations carried out on standard RC chains. The acquired findings showed that, in comparison to SPICE simulations, both models had a comparable maximum error (less than 15% at the output node).

2.2 BUFFER INSERTION IN LONG WIRES

Introducing a new parameter as seen in previous section 2.1 may reduce the delay of the overall device but it can also increase the area of the device. And, however long the wire is it will require a buffer in between to drive it and to avoid crosstalk noise into the circuits and wire engineering. Also, it is already known that when dealing with global interconnects the product of R and C is quadratic in nature with respect to length. To reduce this delay, different materials, techniques or design levels have been adopted to point out the difficulties in CMOS technology as the technology scales down to Nano meter regime [38]. In [39], the impacts of various parameters on connect delay are experimentally investigated, and the optimisation techniques and influencing factors of interconnect delay in large-scale physical design under deep submicron technology are analysed. Lengthening the connection and placing the suitable quantity of buffers can efficiently optimise the latency. Reducing the latency between interconnects and increasing wiring space can be achieved by substituting an equal number of inverters for the buffers on interconnects. When it comes to the buffer insertion in between the long wires, simple 1-bit CMOS inverter is considered best due to its simple design and functioning. Yet, it fails to provide the noise immunity to the circuit. Instead of CMOS inverter as a buffer, Schmitt trigger design is considered for the buffer design to drive interconnect circuits as it not only reduced delay but provides noise immunity as a property of hysteresis also. A Schmitt trigger circuit design for 45, 65 and 90nm technology is implemented and simulated to filter out the issue of noise as compared to the simple CMOS inverter [40]. [41] shows as opposed to a single threshold buffer, the newly suggested Schmitt trigger buffer has a dual threshold feature that reduces crosstalk noise and interconnect delay. Reduced power consumption is also the outcome of using fewer

transistors in the active mode during switching. In [42], authors show how Schmitt triggers can be used as a buffer circuit since they are flexible to use that is their configuration can be adjusted accordingly. The SX-A and RTSX-S families of Actel devices are engineered to provide maximum efficiency, low power consumption, and exceptional dependability. They have consistently proven to be a great option for both military and commercial uses. Furthermore, Schmitt-trigger buffers facilitate the handling of low slew-rate applications. These buffers are easy to implement, reasonably priced, and adaptable enough to allow for many configurations based on the needs of the application. Schmitt-trigger buffer properties, such as threshold voltage, can be set or changed by the user as needed. Schmitt-trigger buffers ensure that the FPGA receives a quick, noise-free input signal. In [43], authors have demonstrated an incredibly economical way to raise the sub-threshold nanoscale circuits' reliability. The implication methodology as mentioned in Fig. 2.5 serves as a broad foundation for specific reinforcement. In order to implement the implication reinforcement, authors choose to employ Schmitt trigger-based circuits, and have shown that this technology delivers good noise immunity at a low cost in terms of area and power overhead.

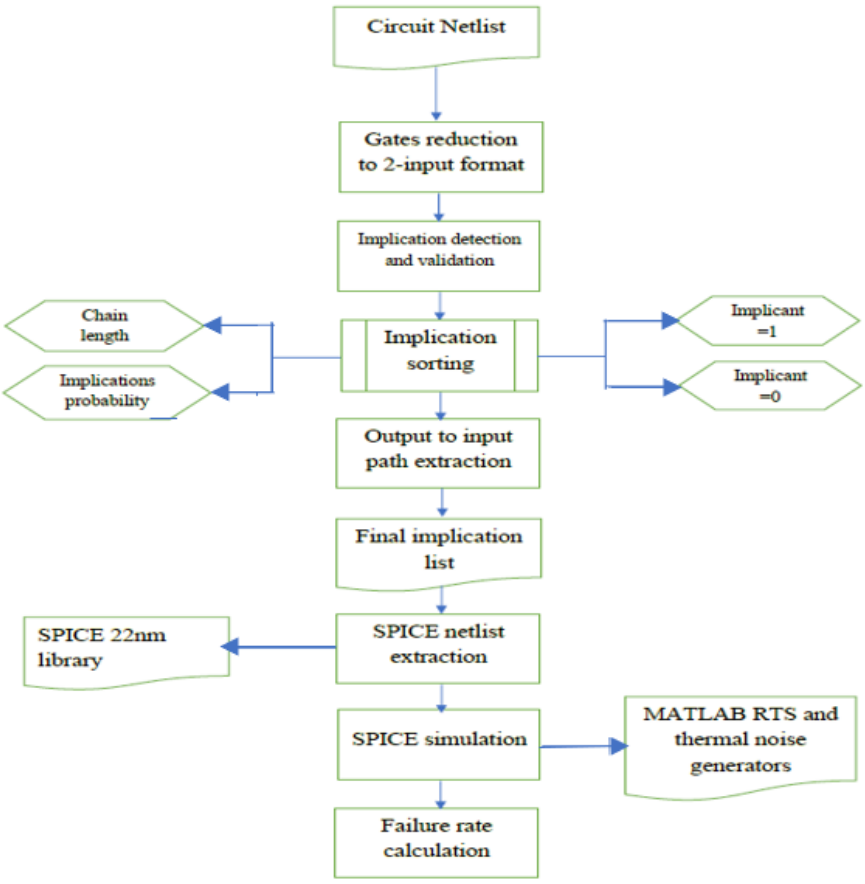


Fig. 2.5. Design flow chart [43]

In [44], an entirely novel CMOS Schmitt trigger that can operate at as low as 0.8V is proposed and exhibited. Comparing the circuit to a typical circuit, the propagation time is reduced. The Design Rule Check (DRC) and Layout Versus Schematic (LVS) checking methods were passed by the suggested circuit. As a result, the circuit has been effectively installed and its industry manufacturing status has been verified. In [45], a larger hysteresis width is offered by the new Schmitt trigger in comparison to the traditional Schmitt trigger. While the new circuit's static power dissipation is nearly twice that of the conventional one, its dynamic power dissipation is nearly equal. This circuit is helpful in situations when a high hysteresis width is needed to increase the noise margin. In [46], the following voltage levels could be supported by an input receiver made with 0.35-μm CMOS technology: as well as 0.9, 1.2, 1.5, 1.8, 2.5, 3.3, and 5 volts. For varying voltage levels, there was a high operating frequency. Its hysteresis feature contributed to its improved noise immunity. As a result, there was less incorrect reception of the logic level in the core. The Schmitt trigger and input buffer are no longer required with the proposed input receiver. Both are combined into one circuit. As a result, the total space needed is smaller than the combined size of the input buffer and Schmitt trigger. Authors in [47] proposes a low-voltage tuneable hysteresis CMOS Schmitt trigger. Low power consumption and configurable hysteresis under low voltage operation which ranges from 0.5 V to 1.8 V are two benefits of this system. The simulation result of the system at 0.8 V and 27 degrees Celsius is deemed adequate. The setup is said to be appropriate for utilised in wireless transponders, sensors, buffers, sub-threshold SRAMs, retinal focal plane sensors, and pulse width modulation circuits. For [48], Tanner EDA tool simulation has been performed at TSMC 130nm technology with a 1 V supply voltage. The circuit's TSPICE simulation results validate the method's efficacy. By adding four transistors that have a lower average power consumption and a smaller footprint, the suggested Schmitt trigger is altered. Using just one PMOS significantly reduces latency since the delay is concentrated in PMOS owing to hole mobility being lower than electron mobility. Four transistors are used to create the proposed Schmitt trigger, which performs better than the traditional Schmitt trigger. Because there are fewer transistors, there is a reduction in both area and delay. Compared to a typical Schmitt trigger, the suggested Schmitt trigger uses less power on average. In [49], the buffers between the interconnects are replaced with the suggested Schmidt trigger (which depends on Sized logic) for additional reduction of strength and delay. A Schmitt trigger consisting of four MOS transistors is used for this investigation. Compared to the current methodologies, the simulation results demonstrate that the suggested

technique exhibits reduced delay and power. The authors have also compared the delay with the increase in nano metre technology nodes as shown in Fig. 2.6.

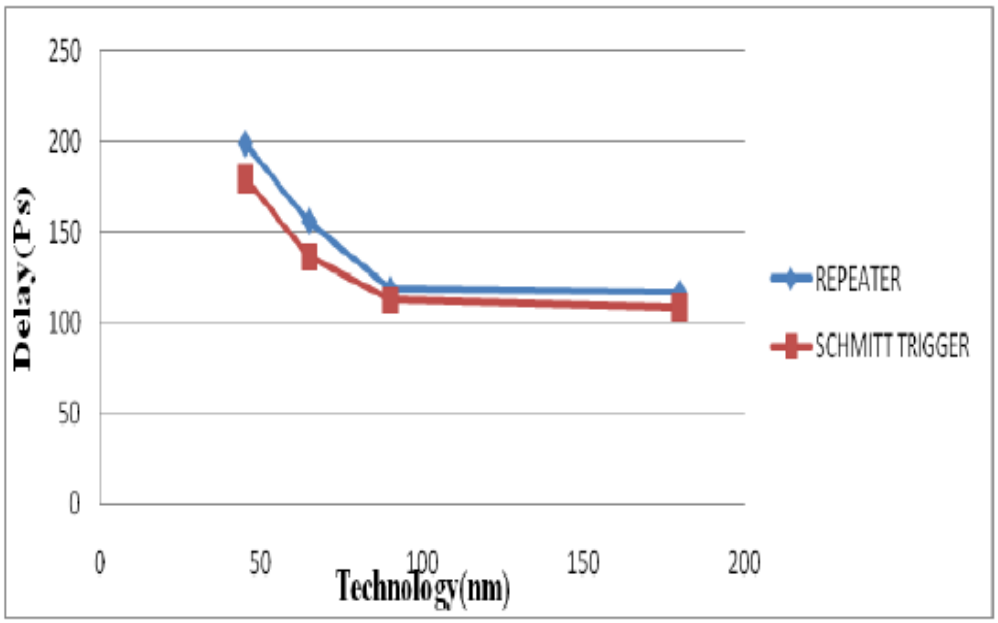


Fig. 2.6. Delay vs Technology nodes [49]

Additionally, Schmitt trigger designs can employ many types of logic, as demonstrated by the author in [50] with complementary pass transistor logic. The circuit is implemented using 180nm technology and its attributes have been quantitatively and analytically measured. Compared to other CMOS Schmitt triggers, the hysteresis feature is more pronounced and less susceptible to process and supply voltage changes. The recently suggested Schmitt trigger circuit is appropriate for applications involving mixed voltage interfaces as it can reject noise. This paper describes a Schmitt trigger circuit that can be used as a foundation circuit for more intricate logic circuits with hysteresis transfer properties. Further, the Schmitt trigger design is also improved by reducing the number of transistors [51] for lower technology using different types of materials CMOS and CNT transistors. The focus is not only reducing the number of transistors in the circuit but also to reduce performance parameters like delay, power, hysteresis loss, leakage current etc. Similarly, an accurate and detailed analysis of the design of six widely used CMOS (SISO) Schmitt trigger circuits is observed [52]. In paper [53], authors have evaluated the impact of geometrical tube parameters variations on scattering and quantum resistance, kinetic and magnetic inductances, and quantum and electrostatic capacitances for isolated and bundles of MWCNTs. The results obtained show that the resistivity of MWCNT-based interconnects

falls sharply with increasing shell count because of an increase in conducting channels, a drop in kinetic/magnetic inductances, and an increase in shell-to-shell capacitances. Due to their higher resistivity, the length variation results predicted that MWCNTs are not the best option for local level interconnects (<100 μm). However, they significantly outperform Copper and SWCNT based interconnects for intermediate (>100 μm) and global level interconnects (>500 μm) resistivity. Apart from the use of CNT material, FinFET technology is also seen to be used in buffer systems to reduce power consumption in the buffer circuits. Author in [54] designs the inverter circuit for 32nm technology node using HPSICE for both CMOS and FinFET technology and compares the power consumption in the circuits. In [55], the replacement of MOSFETs to FinFETs is observed due to reduction in short channel effects. Also, similarly like FinFET material, a different type of FET can be used known as Tunable Field Effect Transistor (TFET). It is gaining a lot of attention from the researchers due to its similar structure as MOSFET, although its functioning differs. In paper [56], authors intend to investigate the applicability of Dielectric pocket (DP) based TFETs for low power applications. To do that, the device's architecture must first be highly optimised using a variety of gate and dielectric engineering techniques. Once this is done, the well-optimized design must then be confirmed for use in analogue, digital, and wireless applications. Reducing number of transistors can be concluded as a better result for reducing the delay in the circuits however, shifting the design and implementing with other materials sems to be difficult. Moving to materials like CNT can be preferred for research purposes but implementing it in real life can be quite a costly task. Apart from only focusing on delay of the buffer system, power consumption as well as dissipation must also be considered. Certain power is consumed by the circuits and certain power is dissipated by the circuits. This power dissipation causes heat generation in the circuits leading the device to lag behind. Sometimes, in case of high amount of heat generation system fails to perform efficiently. To resolve this issue one such method is of bus encoding. Since, global interconnects are used as buses and clocks such a method can be proved to be efficient. In paper [57], author addresses the issue of power dissipation in busses during testing. They conclude that address encoding systems using reference data also regulate the address switching. The data bus and address bus encoding techniques exhibit an average power saving of 30% and 74.8%, respectively, according to the results. Another exhaustive study is done to restore or reuse some of the power dissipated back by the power supply to produce less heat and consume less power. This technique is known as energy recovery technique. Energy recovery technique is the technique which is required to maintain the power consumption of the circuits. It can be

categorized into two classes: Adiabatic Logic and Adiabatic Dynamic Logic as shown in Fig. 2.2 and aims to generate less heat when applied to a circuit.

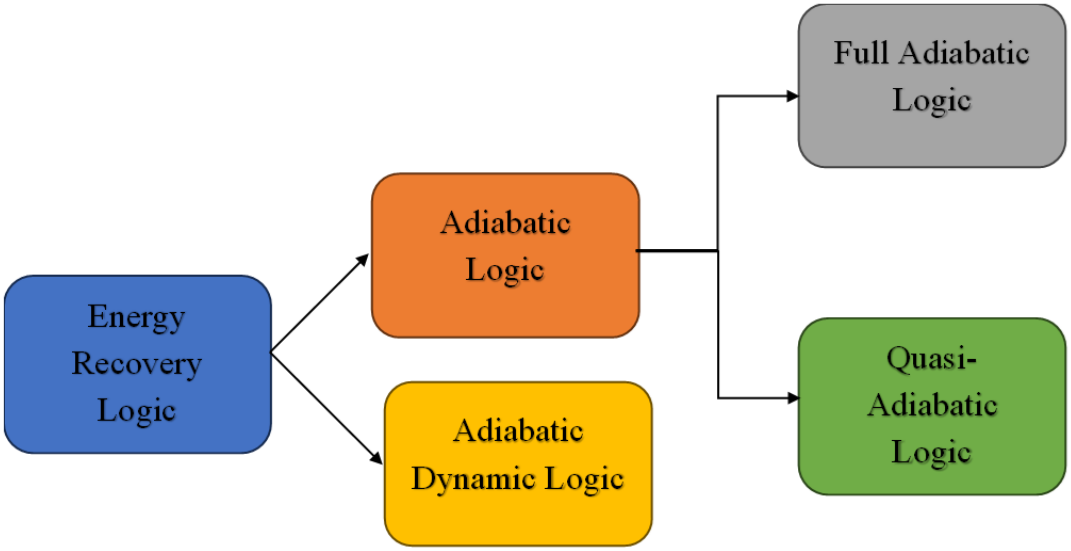


Fig. 2.7. Categories of Energy-recovery logic

Energy recovery techniques as shown in Fig. 2.7 can be classified into adiabatic logic that requires only adiabatic switching process and adiabatic dynamic logic that requires a dynamic logic of the circuit along with the adiabatic switching process. Further, the adiabatic technique can be divided into two categories that is full adiabatic and quasi-adiabatic techniques. However, the focus of this research work will be on adiabatic dynamic technique. Implementing these techniques on buffers that are to be inserted can reduce the power consumption significantly. Still, another issue that pertains with the buffer insertion is the number of buffers to be inserted in between. Proper algorithms are designed for buffer driving ability and number of buffers to be used in between the interconnect circuits [58]. In [59], authors have presented a combined technique from a low swing transceiver and buffer insertion technique. In [60], authors have explored the performance of global interconnects with six different configurations of DG FinFET driver along with the suitability of buffer insertion technique. Inserting buffers in between the long wires is a widely used method for reducing delay in an interconnect circuit. In [61], a summary of a few chosen adiabatic logic styles is completed. On this adiabatic logic and the suggested logic, several logic gates have been developed and simulated at different frequencies. A notable drop in power is seen in the power delay product result. A reduction in the power delay product of up to 46% has been achieved when compared to PFAL adiabatic logic. In [62], authors have introduced a low-energy diode-based adiabatic logic family and two-phase drive adiabatic dynamic CMOS

logic. The 2PADCL's performance possesses a comparatively high throughput and a fast-switching time when compared to ADCL. The modelling results with 2PADCL circuits show that energy usage can be reduced by a factor of two to four. Complete adiabatic systems use around 28% less power than equivalent static CMOS implementations at fs = 1 MHz This includes the creation of the timed supply voltages using a two-phase power clock generator with 97% efficiency. Authors in [63] have compared the traditional static CMOS and the adiabatic PFAL from which it is concluded that adiabatic PFAL delivers a substantial power decrease and therefore higher power performance. The thorough simulation demonstrates that the PFAL circuit can 50% of the energy lost in traditional static CMOS circuitry can be recovered. However, because of its lengthy switching times, the PFAL is not appropriate for applications where delays are crucial. As a result, it operates slowly and is unsuitable for applications requiring quick switching. In [64], a histogram as shown in Fig. 2.8 displays a comparison of power dissipation between CMOS and adiabatic logic. It has been demonstrated through the comparison of CMOS circuits and adiabatic logic techniques that the suggested logic has lower power usage for a lower amount than CMOS. For example, the suggested inverter and 1-bit full adder circuits expend very little power only 12% and 21% of the total power of a static CMOS-based logic circuit when the input frequency fluctuates between 10 and 150MHz.

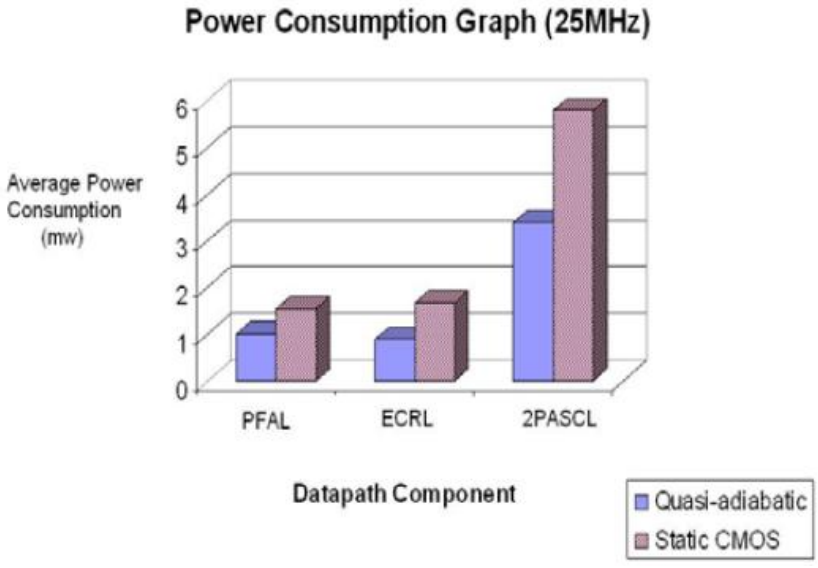


Fig. 2.8. Power dissipation [64]

In paper [65], authors have studied and explained that in some situations, adiabatic logic circuits offer a way to reduce energy dissipation in comparison to conventional logic switching. There is a lower limit to the energy dissipation for the circuits the research results,

beyond which no appreciable improvements can be obtained for longer rise/fall timings. This restriction is mostly brought about by the MOS transistors' finite threshold voltage and, perhaps to a lesser extent, by the nonlinear properties of the MOS channel resistance. In paper [66], authors have concluded that the logics and circuits using adiabatic regime can reduce power dissipation up to 90% which is mainly due to the recycle of energy and reusing it for further processing. Regretfully, the clock consideration poses a significant issue with the adiabatic dynamic approach. The electrical systems will only work correctly when the right clocks are used. Additionally, it ceases to function on high-speed systems and is only appropriate for uses requiring incredibly low energy dissipation. In [67], authors have proposed the FinFET based 2N-N-2P adiabatic logic circuit. By contrasting the design with 2N-2N2P and PFAL inverter/buffer circuits constructed with both MOSFET and FinFET, the suggested logic is validated. In comparison to the 2N-2N2P and PFAL inverter circuits, the FinFET-based 2N-N-2P inverter circuit uses 31% and 38% less power, respectively. Additionally, the 2N-N-2P CMOS-based Compared to CMOS-based 2N-2N2P and PFAL inverter circuits, the inverter circuit uses 12% and 14% less power, respectively. In [68], authors have explained a new and highly developed type of adiabatic CMOS that exhibits great promise for real-world uses and striking demonstrations that highlights the enormous amount of efficiency gains still achievable for universal digital computing in the future. In [69], author provides a simulation of Adiabatic Static CMOS Logic (2PASCL), a two-phase clocked CMOS technology. Through the application of the theory of adiabatic charging and energy recovery, 2PASCL the inverter produces the least amount of energy dissipation of all CMOS and simulated adiabatic inverters. In [70], authors have presented a review on adiabatic logic based full adder circuits and compared its performance in terms of transistor count, power, speed and delay.

2.3 CURRENT MODE SIGNALLING IN INTERCONNECTS

Yet, adding buffers in between using any technique or method means adding an extra circuitry to the whole device again causing area constraints. To avoid such limitations and enhance overall performance of the system different techniques are described with better results such as replacing voltage mode signalling with current mode signalling. In [71], authors have studied about current mode signalling technique for low power and high-speed interconnects. In [72], authors compare voltage mode signalling with current mode signalling for power performance. In [73], various interconnect techniques for on-chip RC and RLC interconnects are compared. It is indicated that the delay benefit for current sensing increases

with wire width. It is also studied about current sensing which eliminates any placement constraints and does not necessitate the placement of buffers along the wire, unlike repeaters. In [74], current mode interconnects for investigating the performance of RLC equivalent R_{eff} C_T mathematical delay model for interconnects are presented. The dominance of inductance effect is optimized using Simulative Sweep Analysis Technique (SSAT). Results are simulated using SPICE. [75] has reviewed various low-power circuit design-based interconnects for the increasing demand of portable devices. The author indicates that global interconnects have a significant impact on the performance and power dissipation of sub-threshold circuits. In [76], authors show a second order transfer function that is developed for current mode high speed VLSI interconnects using a finite difference equation, a Laplace transform at the source, and load termination to stop current mode signalling. The goal of the current work is to use the current voltage mode to estimate the delay of current-mode VLSI interconnects and determine how delay interacts with line inductances, load capacitances, and lengths. Given all the advantages, present mode signalling. In [77], author provides closed-form models for delay estimation of current mode high-speed VLSI interconnects based on the Eudes model and an extension of the Eudes model. The objective of the present Using the current Eudes model and its extension against the HSPICE tool, the work aims to estimate the delay of current-mode VLSI interconnects and determine the interplay between delay for different lengths, line inductances, and load capacitances. This study has demonstrated that, although our expanded model performs better at longer lines, the current Eudes model is unable to provide high accuracy for lines longer than 0.3 cm. In [78], authors reviews and talk about current mode signalling techniques, its advantages and issues that can persist in a circuit.

2.4 RLC INTERCONNECT CIRCUITS

Although, still with the decreasing size of technology and enhanced performance parameters another issue rises that is inductance as a parasitic component. As the technology moves down to lower technologies, inductance factor becomes dominant in the interconnect structure. If not handled properly it can cause issues which can cause system failure. Closed form solutions for 50% delay, rise time, overshoot and settling time of signals in an RLC tree can be observed along with the solutions containing similar results as Elmore delay for RC trees and preserving the simplicity of the circuit [79]. Aside from Elmore delay calculations, the Fourier analysis of on-chip signals for RC and RLC ladder circuits in CMOS integrated circuits can also be done [80]. In [81], a new crosstalk noise mitigation methodology based

on our novel transmission gate design is proposed. This approach results in smaller area overhead compared to driver sizing taken alone and requires minimum change in circuit layout. In [82], the effectiveness and limitations of different on-chip interconnect signalling techniques in deep submicron technology (UMC 90 nm) is analysed. The performance of each circuit is analysed on the benchmarked interconnect (RC or RLC 3-π). Scaling in [83], authors have provided a Fourier analysis of typical on chip signals in CMOS technology circuits. the signals are approximated up to the 15^{th} harmonic component. In [84], a response of a linear nonmonotone system that is comparable to the Elmore delay can be described generally using the approach that is described. The correctness of the RLC tree delay expressions is the same traits that the RC tree Elmore (Wyatt) approximation possesses. There are straightforward mathematical equations given for the 50% delay, rising time, overshoots, and settling time of signals in an RLC tree. Both monotone and non-monotone signal responses are taken into account in these formulas. In distributed RLC lines with capacitive load, new compact expressions for time delay, repeater insertion, and crosstalk have been presented in [85]. Regarding certain useful ranges of the line parameters, when compared to HSPICE simulations, the inaccuracy is roughly 2%, 2%, and 10% for time delay, repeater insertion, and crosstalk, respectively. In [86], an analytical delay model is presented based on a second order approximation that takes into account the impact of complex and real poles for RLC interconnect lines includes ground capacitance and inductance. The effects of output load capacitance and driver/source resistance have also been considered. Our generated models, which include both actual and complicated pole models, have an average error rate of between 10.49% and 10.14% using HSPICE simulation and 15%–20% using alternative models that are currently in use. The HSPICE simulation reveals that when the inductive impact increases, latency increases noticeably.

CHAPTER 3

DESIGN AND IMPLEMENTATION OF RC GLOBAL INTERCONNECTS WITH DIFFERENT LENGTH

CHAPTER 3: DESIGN AND IMPLEMENTATION OF RC GLOBAL INTERCONNECTS WITH DIFFERENT LENGTHS

The importance of interconnects in integrated circuits, both current and future, has led to the publication of a substantial amount of research over the past few decades on a wide range of subjects, including interconnect models, parasitic extraction, and interconnect design techniques.

An overview of the development of on-chip electrical connectivity is given in this chapter. In section 3.1, basic introduction is provided. In section 3.2, Elmore delay estimation is detailed followed by interconnect design criteria. Section 3.3 explains the proposed approach for interconnect designs. Section 3.4 explains results and discussion followed by the experimental evaluations, theoretical evaluations and the comparison. Lastly, section 3.5 provides with the conclusion of the whole chapter.

3.1 INTRODUCTION

Interconnects are now considered to be the essential parts of integrated circuits (IC). These are the metal wires that connect the active devices electrically so that power and signals can be sent and received throughout the circuit. Technology is advancing quickly, leading to more sophisticated integrated circuits with smaller feature sizes needed. However, as the feature size of the connecting wires reduces, the signal integrity issues become more noticeable even as the speed, power, area, and cost qualities increase. During the chip-making process, several components are created on the chips, and these components are subsequently connected. Because there isn't enough room to link everything, interconnects are designed in vertical layers or levels by the makers. A complex IC can have ten or more interconnect layers. These multilevel metal formations ascended much higher and started to dominate the anatomy of IC. Interconnects began to control the power, noise, timing, dependability, and design functionality of the circuits. Depending on the function they are carrying out, the interconnects can be divided into local and global interconnects. Local interconnects are the basic low level wires connecting transistor to transistor whereas global interconnects are the long wires high above in the ICs providing busses or clock connections. Both types of interconnections are necessary and are described in the following sections.

3.1.1 INTERCONNECT DESIGN CRITERIA

Since interconnectivity has emerged as a major concern in high-performance integrated circuits, the focus of the circuit design process has moved from logic optimisation to connection optimisation. The interconnect design process should include several characteristics, such as latency, power dissipation, power consumption, noise, bandwidth, and physical area.

i. Delay

A circuit's speed and interconnect delay are closely related, making interconnect delay a crucial design factor for an integrated circuit. The timing constant due to interconnect has changed considerably due to technology scale down. Since technology reduction changes the geometry of the wire, hence the delay also gets affected in the process. So far, only lumped capacitance model was used to model the wire but with the change in wire width the effect of resistance has also started to play a crucial role creating a valuable effect on interconnect delay. For the computation of interconnect delay both resistance and capacitance must be considered as the delay is the product of both the parasitic. Since, Eq. (1.1) shows the evaluation of resistance for an interconnect, two terms come into feature – sheet resistance and aspect ratio of the wire. Sheet resistance is the R_{sq} is the computation of resistivity of the material used and the wire thickness as expressed by Eq. (3.1).

$$R_{sq} = \frac{\rho}{T} \tag{3.1}$$

Where ρ is the resistivity in Ω-cm, T is the wire thickness, and R_{sq} is the sheet resistance with the unit of ohms per square (Ω/□) [16]. The ratio of *L/W* is referred to as the number of squares of the wire or the aspect ratio of the wire. The aspect ratio increases as the interconnection increases and decreases, provided that R_{sq} remains constant for that particular technology. This is the main reason for the cause of significant RC delay issues.

As for capacitance, wires were used to be much wider than they were thick. As a result, one could roughly describe them as having parallel plate capacitance concerning the grounded substrate. As opposed to layers above or below, wires now frequently have the same thickness and diameter and are closer to one another. In addition, compared to the substrate, the layers above and below are far closer. As a result, a wire's capacitance to ground is insignificant

compared to that of adjacent wires, which may transition and couple noise into the poor wire [87].

ii. Power consumption/dissipation

Power consumption has become one of the vital performance parameters to evaluate overall performance for a portable digital circuit. Targeting power consumption automatically targets the power dissipation into the circuits. These advancements are mostly being driven by portable applications, like notebook computers, and portable communication devices, which demand high throughput at minimal power dissipation. In the majority of these situations, achieving high chip density and high throughput—two equally challenging objectives—must coexist with the need for minimal power consumption. Consequently, the domain of CMOS design, which addresses the low-power design of digital integrated circuits, has experienced a surge in activity and rapid evolution. Further, smaller circuits raise the problem of power dissipation, which can lead to distortion or information loss. Since interconnects dominate the overall system performance for smaller and quicker technologies, this problem can be resolved by concentrating on the interconnects that connect all components together. Furthermore, concentrating on interconnects can significantly lessen power-related problems. The proximity of interconnects due to their tiny spacing can result in several problems, including excess heat generation and crosstalk, as well as complete system failure.

iii. On-chip Area

Recent technological developments have made it possible to integrate billions of transistors into a single monolithic die. There are now notably more interconnects as a result. The die size is anticipated to remain relatively constant for upcoming technologies, nevertheless, according to the International Technology Roadmap for Semiconductors. The number of metal layers needs to be increased to provide sufficient metal resources for connection routing. Nevertheless, increasing the number of metal layers drives up production costs. Moreover, the silicon area constraint is tightened by pipeline registers and buffers placed along the interconnects. As a result, when designing an interconnect, the area criterion should be taken into account when doing tasks like repeater placement and wire sizing.

3.2 ELMORE DELAY ESTIMATION

With today's technology, the ability of the interconnects to attain planned clock frequencies largely determines the circuit performance. For efficient circuit designs, the cognitive factor influencing circuit performance is connected to delay. Multiplying the entire resistance (R) by the total capacitance (C) yields the RC delay (τ) of an RC line. The most used model for estimating delays is the Elmore delay model. It provides an accurate estimation of delay in lumped models and can be used for n-segments of a long wire. Though the Elmore delay estimate is the simplest and fastest estimation, only the first moment of the impulse response is employed for delay computations. An RC ladder's Elmore delay is calculated by multiplying the capacitance of each node in the circuit by the total resistance from the source node to the node that is being visited. To make signal delay simply usable for connection optimisation, it enables us to describe it explicitly as a straightforward algebraic function of geometric characteristics of interconnects [16]. Elmore delay provides output for a step function-type input signal. The time T_d, which satisfies Eq. (3.2) [88], is the 50%-point delay of a monotonic step response if the circuit's step response is h(t).

$$\int_0^{T_d} t\,h(t)dt = 0.5 \tag{3.2}$$

The mean of the impulse response h(t) is used to estimate T_d in the Elmore delay model. When considering the impulse response as the probability density function, the mean can be defined as the impulse response's first moment, or τ_d, as expressed by Eq. (3.3) [87].

$$\tau_d = \int_0^{\infty} t\,h(t)dt \tag{3.3}$$

The Elmore delay is the term used to describe the initial phase of the impulse response. It serves as a reliable approximation of the circuit's delay and the dominant time constant. Therefore, the Elmore delay for an RC ladder can be calculated using Eq. (3.4) [16].

$$\tau_i = \sum_k (C_k \times R_{ik}) \tag{3.4}$$

The capacitance at node k is denoted by C_k, the resistance in common from the source to node i to the source to node k is summed by R_{ik} and node i is the node of interest. The Elmore delay estimation for n number of segments is expressed in Eq. (3.5).

$$\tau = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3 + - - - - + (R_1 + R_2 + R_3 + - - \cdot \quad (3.5)$$

Elmore delay estimates are available for both distributed and lumped RC lines. The lumped and dispersed RC network is displayed in Fig. 3.1.

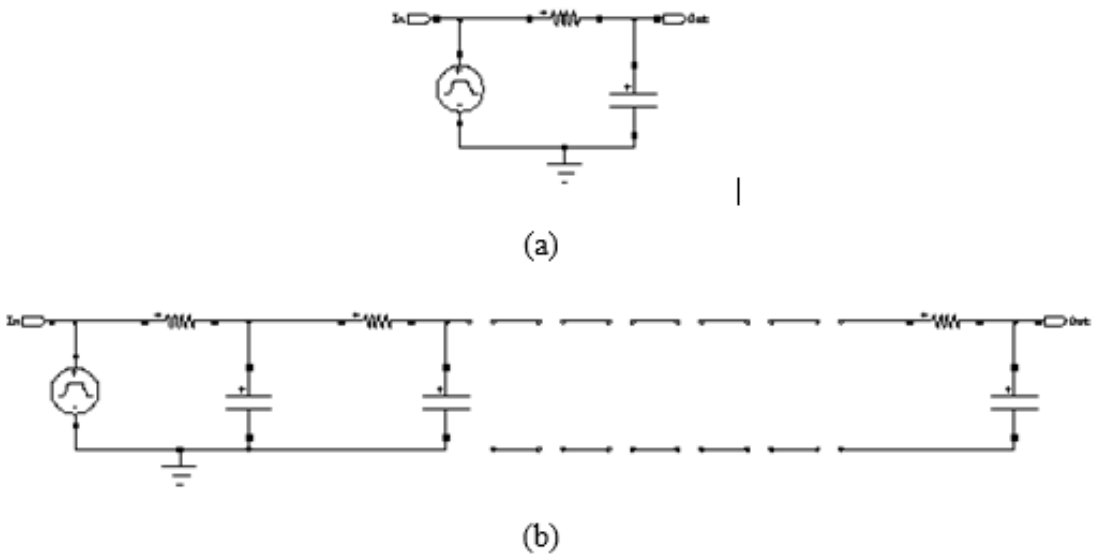


Fig. 3.1. VLSI Interconnect (a) Lumped model (b) Distributed model

The overall delay for a lumped model can be written as $\tau = RC$, the product of resistance and capacitance. A wire's lumped network is seen in Fig. 3.1(a). 50%-point latency for lumped networks is equal to 0.7RC if step input is used [89]. The RC delay for long-distributed wires can be calculated using total wire capacitance (C) and total wire resistance (R). The RC ladder with n segments and a total wire length of L is shown in Fig. 3.1(b). A distributed network's 50%-point delay is equal to 0.4RC if step input is used [89]. With longer interconnects and more advanced technologies, the problem of higher resistance value still exists. Additionally, the length of the connector increases quadratically with the delay for long wires. Thus, for the best delay value, it becomes crucial to minimise the interconnect parasitics. An innovative strategy is used to target overall resistance as well as the interconnect circuits' delay to achieve a stricter relationship for delay.

3.3 PROPOSED METHODOLOGY

The distribution and structure of interconnects determine better performance. In addition, wire sizing that is uniform and non-uniform distribution must be taken into consideration independently of the interconnect structure to maximise performance characteristics. The length of the wire needs to be dispersed evenly to obtain the performance parameters that are

correctly optimised. A non-uniform distribution of length involves dividing the total number of segments at random, as illustrated in Fig. 3.2(b), whereas a uniform distribution of length distributes each segment per unit length, as illustrated in Fig. 3.2(a). An example can be used to comprehend the connection wire distribution. Assume we have a 3 mm wire with a total capacitance of 575 fF and a resistance of 330 Ω. The uniform and non-uniform distribution of 3 mm wire are depicted in Figs. 3.2(a) and (b). The wire is divided uniformly into three segments (n = 3) for uniform distribution. 95.83fF is the value of each capacitance, while 110Ω is the value of each resistance. For a non-uniform distribution, there are two segments (n = 2) in the wire or any number of segments can be done non-uniformly. Individual capacitance is 143.75fF and individual resistance is 165Ω [24]. Even if non-uniform distribution uses fewer parasitic components overall, uniform distribution performs better because its components are distributed equally across units of length. Therefore, when modelling interconnects, uniform distribution is taken into account.

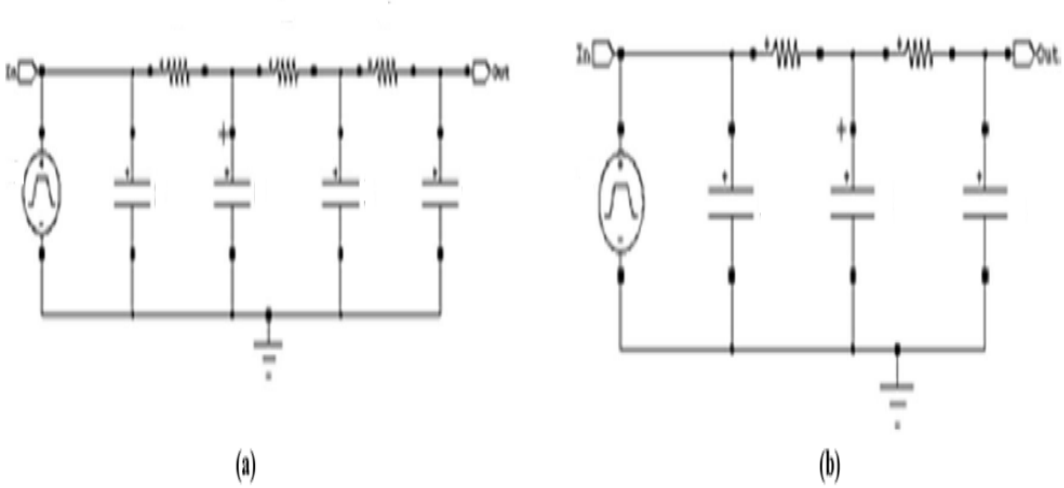
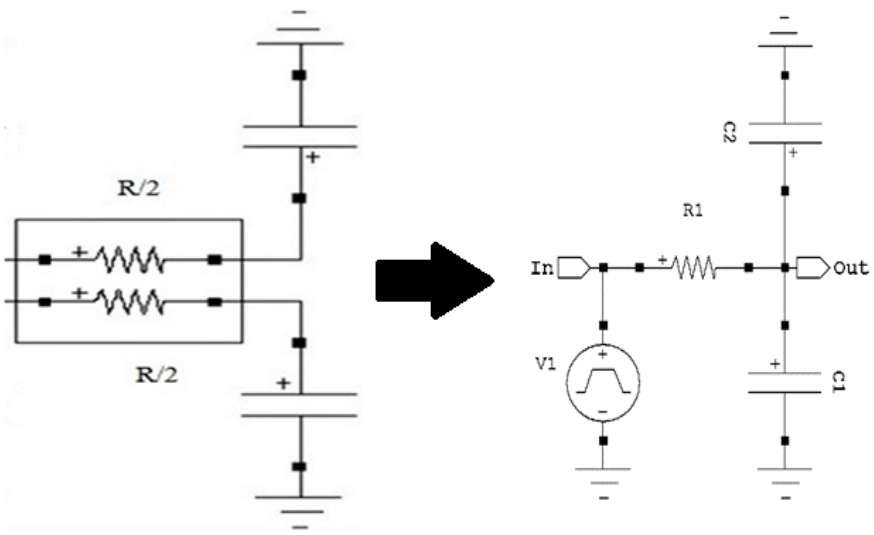


Fig. 3.2. Wire sizing for 3mm wire (a) Uniform Distribution (b) Non-uniform Distribution

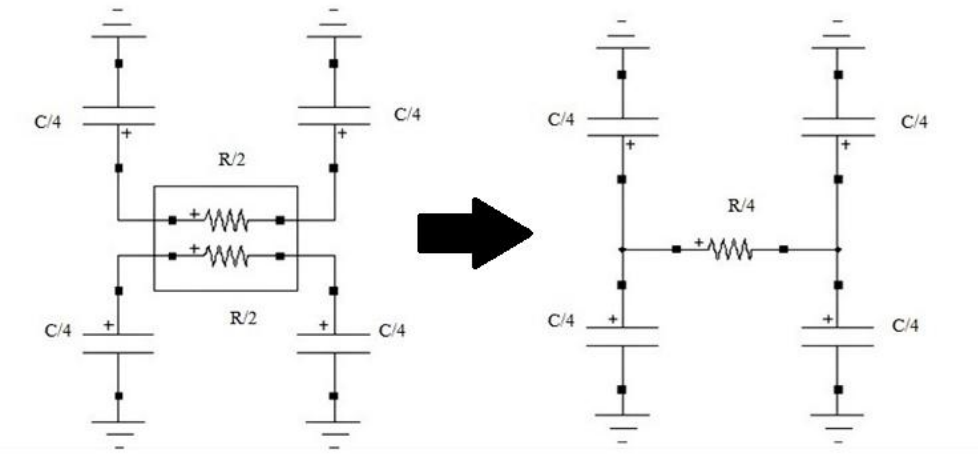
Regarding interconnect topology, the L model is the most basic lumped model in which the Elmore delay calculation for long wires is not satisfied. The delay (τ) is calculated as the product of total resistance and total capacitance (*RC*). This model ought to be avoided as a result. The Elmore delay estimation is entirely satisfied when the T and π-model's delay is determined as *RC/2* by dividing the resistance and capacitance values in half, respectively. The most common model for a distributed RC line is the π-model; it differs from the T model primarily in that the T model has an extra node, which could complicate the model or need more computations. Additionally, the circuits can be separated into 2π, 3π, etc. models for

even better delay values. Although it is believed that the π-model structure optimises performance characteristics, power consumption varies with connection length.

An enhanced Elmore estimation delay model (H-model) is presented to obtain a stricter power-length relation function. This model also linearly decreases interconnect circuit delay by a factor of 4 since wire resistance is reduced four times. Both the L and the π models are used to create the suggested interconnect structure, and a comparison is performed between them. By lowering the circuit's total resistance, the suggested connection arrangement lowers power consumption and delays. The interconnection circuit latency is evaluated in both lumped and distributed networks that use ramp and pulse input signals, respectively. The theoretical evaluation of the suggested model is compared with simulation findings. Resistance, capacitance, and their half values are the components of the suggested structure for the L and π interconnection models. One of the circuits is put together in reverse order due to the manner it is joined. The basic idea is to maintain constant capacitance values while reducing the resistance of connection structures. As seen in Fig. 3.3(a), the resistances and capacitances for the L-model lumped interconnect structure are joined to produce the alphabet T. As seen in Fig. 3.3(b), the resistances and capacitances for the π-model lumped interconnect structure are joined to produce the alphabet H. The resistances and capacitances for the distributed interconnect structure are separated into lumps of equal length while taking uniform distribution into account.



(a)



(b)

Fig. 3.3. The proposed lumped interconnect structure for (a) L model (b) π – model

By connecting the two circuits, the resistance of the suggested design is reduced by a factor of four. The significance of resistance increases with the shrinking of technology. Since resistance and delay are directly related, higher resistance results in higher delays and higher powers. When two circuits are connected in parallel, the resistance in the shown design also becomes parallel. The resistance value is split across the two circuits created by splitting the single circuit into two. Furthermore, as resistance directly affects power and delay, a decrease in resistance optimises the performance metrics. Eq. (3.6) is used to compute the suggested structure's total resistance.

$$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} \tag{3.6}$$

Similar to resistance, each segment's value is distributed equally among them, reducing the total capacitance value for the circuit even if it stays constant overall. Additionally, as technology advances, the length of long wires stays constant, but their thickness and diameter decrease. The area is reduced as a result of this reduction. Because area and capacitance have a direct link, if area decreases, capacitance likewise decreases. The circuits' overall speed is increased as a result. Each segment's total capacitance is computed using Eq. (3.7).

$$C = C_1 + C_2 \tag{3.7}$$

The lowered values of the capacitance and resistance are used to calculate the delay for the proposed lumped interconnect arrangement. Eq. (3.8) expresses the Elmore estimation for the lumped network.

$$\tau = \left[\frac{R}{4} * C\right] = \frac{RC}{4} = 0.25\,RC \qquad (3.8)$$

For distributed networks, the Elmore delay can also be calculated. The dispersed topology of the interconnect with *n*-segments is displayed in Fig. 3.4. The resistances and capacitances in a distributed interconnect system are joined to form the letter H. Algorithm 3.1 describes how the suggested interconnection structure is used to build the RC ladder.

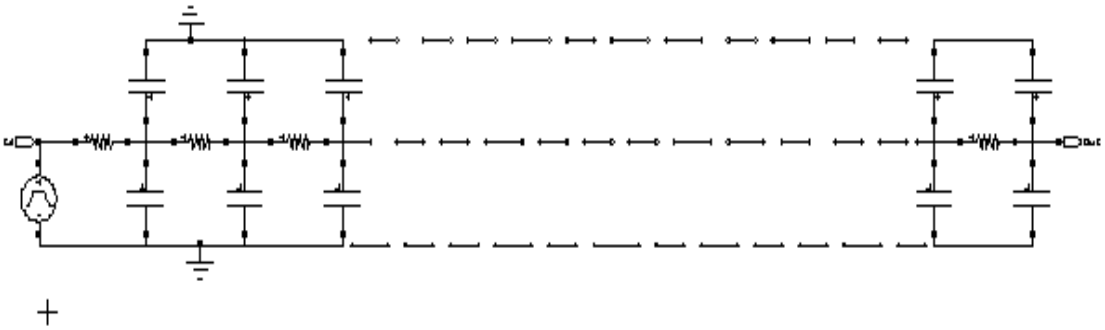


Fig. 3.4. A distributed RC network

Algorithm 3.1: The New Interconnect Structure for Power Consumption and Delay.

Input: Interconnect

Output: Delay, Power consumption

Start

Step 1: Assess the circuit's total resistance and total capacitance while taking the interconnect length into account.

Step 2: Distribute segments to simulate a distributed RC line.

Step 3: Use the suggested construction to simulate the RC ladder for the length under consideration.

Step 4: Split each section in two.

Step 5: To construct the alphabet H, place one half piece upside-down and the other half section upright.

Step 6: Calculate the total resistance of each segment when connected in parallel by dividing the resistance value of each segment.

Step 7: Divide the total capacitance value equally among the segments.

Step 8: For each segment in the RC ladder depicted in Fig. 3.4, repeat steps 3 through 7.

End

As the total resistance of the interconnection circuit reduces, so does the delay. Let us analyse a distributed RC network with the proposed topology shown in Fig. 3.4 to evaluate the newly improved Elmore delay. The length (*L*) of the connection remains constant. If the total capacitance (*C*) and reduced total resistance (*R/4*) grow into *n* equal segments, the Elmore delay can be computed using from Eq. (3.9) to Eq. (3.16) [24, 52]:

$$R_1 = R_2 = - - - - - - - - = R_n = \frac{R}{4n} \tag{3.9}$$

$$C_1 = C_2 = - - - - - - - - = C_n = \frac{C}{n} \tag{3.10}$$

Using Elmore estimation:

$$\tau = \frac{RC}{4n^2} + \frac{2RC}{4n^2} + - - - - - - - + \frac{NRC}{4n^2} \tag{3.11}$$

$$\tau = \frac{RC}{4n^2}[1 + 2 + - - - - - - - + N] \tag{3.12}$$

$$\tau = \frac{RC}{4n^2}\sum_{i=1}^{N} n \tag{3.13}$$

$$\tau = \frac{RC}{4n^2}\left[\frac{n(n+1)}{2}\right] \tag{3.14}$$

$$\tau = \frac{RC(n+1)}{8n} \tag{3.15}$$

Given a step response, the 50% delay for n→∞ is as follows:

$$\tau = \frac{RC}{8} = 0.125RC \tag{3.16}$$

Therefore, Eq. (3.17) is used to calculate the improved Elmore delay for a distributed RC ladder:

$$\tau_i = \sum_k (2C_k \times R_{ik}) \tag{3.17}$$

In this case, node *i* is the node of interest, $2C_k$ is the total capacitance at node k, and R_{ik} is the total resistance shared by the source and nodes *i* and *k*. Eq. (3.18) expresses the Elmore delay estimation for *n* number of segments.

$$\tau = R_1(C_A + C_a) + (R_1 + R_2)(C_B + C_b) + (R_1 + R_2 + R_3)(C_C + C_c) + - - - - - + \\ + R_3 + - - + R_n)(C_N + C_n) \tag{3.18}$$

The circuit's four-fold decrease in resistance, even with the same capacitance, clearly demonstrates the drop in power usage. The connection circuits have been upgraded, as seen by this computation. Therefore, it can be concluded that power consumption is just as important to circuit dependability and efficiency as the delay parameter. It is possible to lower a circuit's power usage by providing the ramp as an input. A signal type known as a ramp increases linearly and consistently over time. The ramp supply shortens the capacitor's charging period, which eventually contributes to low power consumption and dissipation. A circuit with lower power consumption will dissipate less heat and last longer. Furthermore, the resistance and duration of the current flow provide insight into the circuit's dependability. Heat dissipation increases with resistance and time constant; however, this resistance and delay can be reduced by properly distributing the wire.

3.4 RESULTS AND DISCUSSION

Considering 45nm technology and uniform distribution of interconnect parameters, wire geometry can be evaluated using PTM [23] and is tabulated in Table 1.1 in chapter 1. The performance parameters are evaluated for different lengths of interconnect circuits ranging from 1mm to 10mm long.

3.4.1 THEORETICAL EVALUATIONS

The individual resistance and capacitance values can be obtained by dividing the equal values of each resistance and capacitance by four, taking into account uniform distribution, or the distribution of segments per unit length. The theoretical results for lumped and distributed L and π-networks are tabulated in Tables 3.1 and 3.2. Eq. (3.16), Eq. (3.17), and Eq. (3.18) can be used to infer the following theoretical conclusions.

Table 3.1. The performance parameters of lumped network for L and π-model from length 1mm to 10mm for pulse input

Length (mm)	Theoretical delay L-model (ps)	Theoretical delay π-model (ps)
1	21.01	10.5
2	84.26	42.13
3	189.75	94.87
4	337.48	168.74
5	527.45	263.72
6	759	379.48
7	1033	515.63
8	1349	674.96
9	1708	854.29
10	2109	1050

Table 3.2. The performance parameters of distributed network for L and π-model from length 1mm to 10mm for pulse input

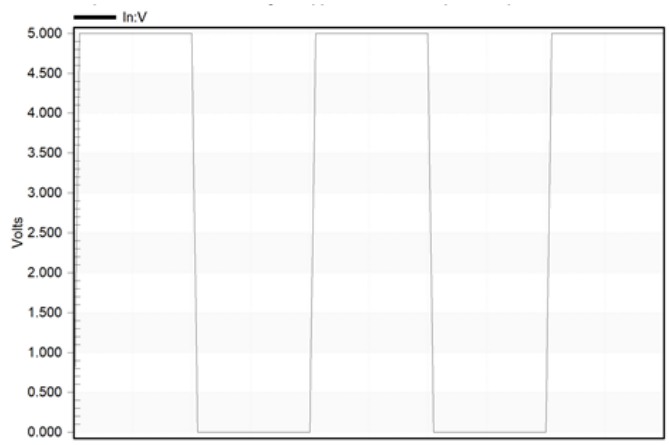
Length (mm)	Theoretical delay L-model (ps)	Theoretical delay π-model (ps)
1	5.25	2.62
2	15.79	10.53
3	31.62	23.71
4	52.73	41.22

5	79.11	63.05
6	110.68	94.87
7	147.60	121.90
8	189.83	168.74
9	237.30	203.02
10	290.09	263.72

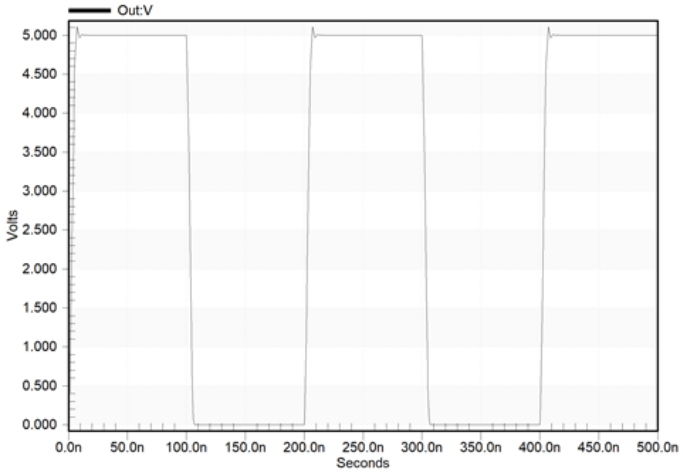
It is clear from Tables 3.1 and 3.2 that the delay rises as the interconnect length does. Additionally, it is necessary to follow the instructions in Eq. (1.10) to obtain precise results for the selection of a circuit's critical or optimal connection length.

3.4.2 EXPERIMENTAL EVALUATION

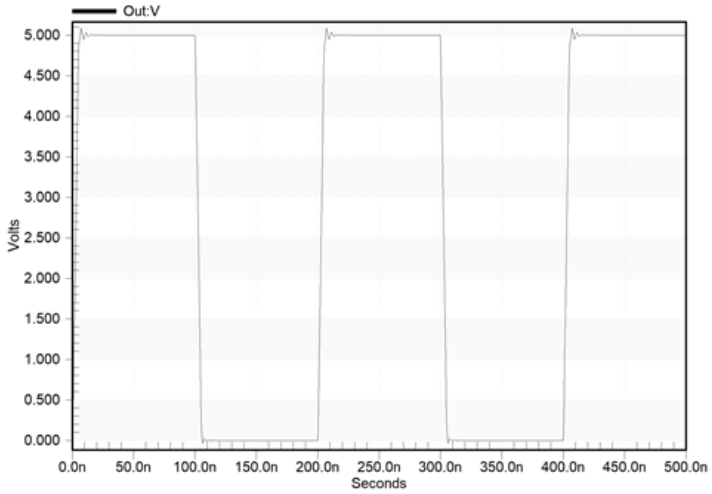
To obtain the individual values of resistance and capacitance, divide the equal values of each resistance and capacitance by four, taking into account uniform distribution, or the distribution of segments per unit length. For example, a 2mm wire has an overall capacitance of 383fF and an overall resistance of 220Ω. A uniform distribution yields an individual resistance (R/4) value of 27.5Ω and an individual capacitance (C/4) value of 95.75fF since the overall capacitance value is spread equally among all the capacitances. Using SPICE, the simulations are run, and it has been noted that the outcomes vary depending on the inputs used. As seen in Fig. 3.5(a), (b), and (c), the output is observed to be slightly distorted for pulse input. Delays or excessive power usage may be the cause of this. As seen in Fig. 3.6(a) and (b), for ramp input, the output maintains its initial shape by lowering the circuit's power consumption through gradual switching. For pulse input supply, time period of 500ns and rise time of 5ns was considered.



(a)



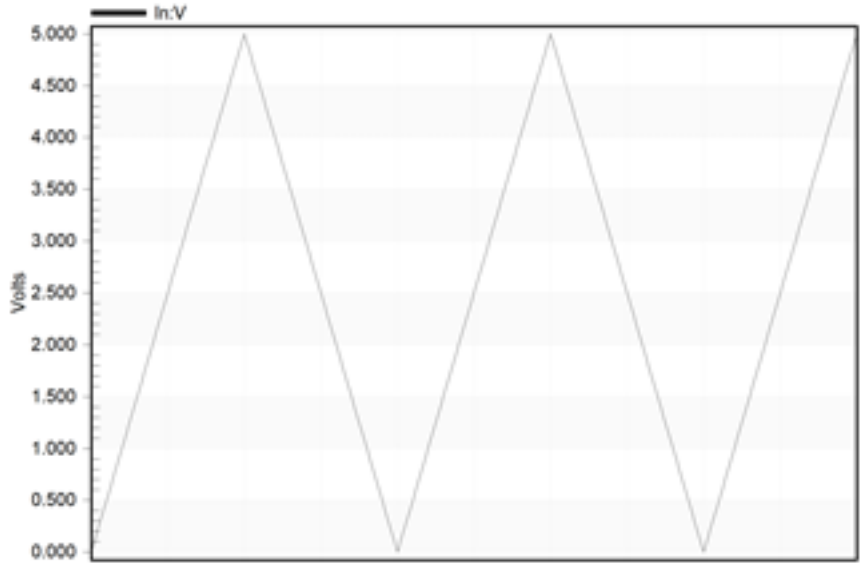
(b)



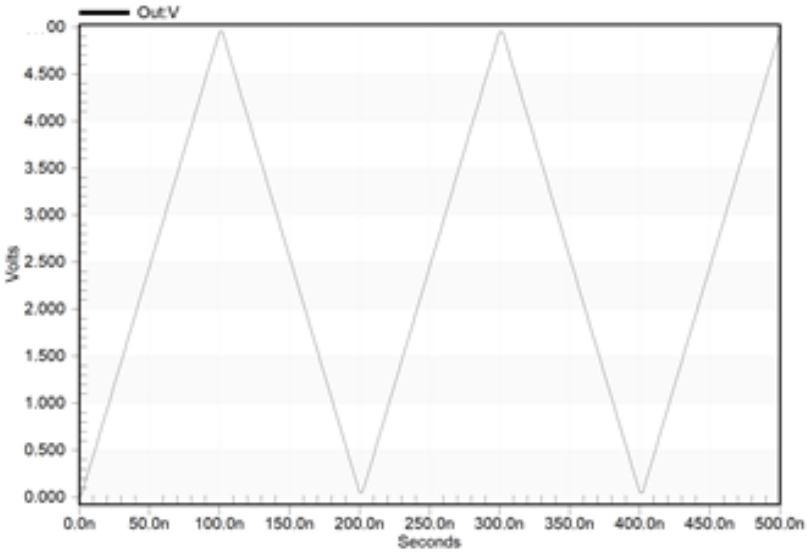
(c)

Fig. 3.5. Simulation results (a) Input pulse signal (b) Lumped Output with overshoot (c) Distributed Output with significant distortion

Fig. 3.5 shows the waveform that results from providing lumped and distributed circuits with pulse input. Both waveforms make it clear that there is a signal overshoot with every increase in the signal. Overshoot is a distortion in the output signal that occurs when the transient value exceeds its final value. Nonetheless, the signal self-stabilizes with the signal's rising time to minimise changes to the output.



(a)



(b)

Fig.3.6. Simulation results (a) Ramp Input (b) Output with no distortion

The waveform for the circuit with ramp input is shown in Fig. 3.6. The time period and rise time was taken same as that of pulse input. It is evident that the circuit's output is distortion-free, and significant power reductions are possible. A further classification for H-model topologies for interconnects is uniform and non-uniform distributions. Once again, the parameters for the H-model with uniform and non-uniform distribution, as shown in Fig. 3.7(a) and (b), are assumed using a 3 mm wire with a total resistance of 330Ω and a total capacitance of 575 fF. For uniform distribution, the wire is divided uniformly into three segments (n = 3). Each resistance is 27.5Ω, and each capacitance has a value of 47.915fF. In the wire, there are two segments (n = 2) for a non-uniform distribution. Individual resistance is 41.25Ω, while individual capacitance is 71.875fF.

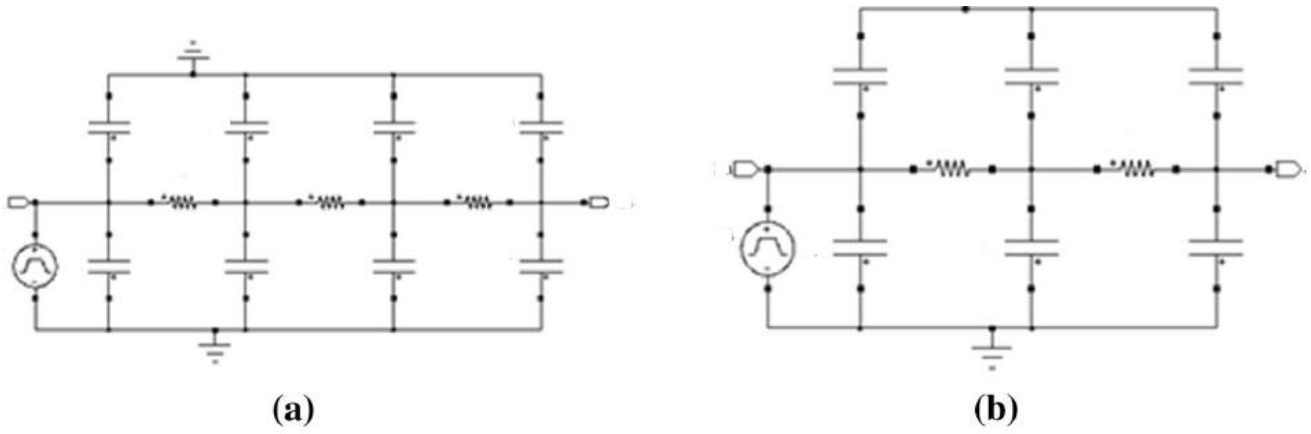


Fig. 3.7. H-model (a) Uniform distribution (b) non-uniform distribution

The proposed interconnect structure was implemented and simulated successfully using LTSPICE software for two types of input supply – pulse and ramp. The simulated performance results for lumped L and π – model interconnect structures using pulse input is tabulated in Table 3.3. Similarly, the simulated performance results for distributed L and π – model interconnect structures using pulse input is tabulated in Table 3.4.

Table 3.3. Simulation results for lumped interconnect circuit with pulse input for L and π models

Length(mm)	Simulated delay L-model (ps)	Simulated delay π-model (ps)	Power consumption L-model (µW)	Power consumption π-model (µW)
1	21.02	10.66	1.81	0.452
2	84.26	42.13	14.63	3.65
3	189.75	94.87	49.89	12.37

4	337.41	168.74	119.36	29.53
5	525.84	263.72	231.7	58.14
6	748.71	379.33	388.85	100.64
7	998.64	515.24	588.64	158.94
8	1260	668.93	823.41	233.4
9	1640	837.38	1084.3	323.44
10	2100	1010	1362.01	427.61

Table 3.4. Simulation results for distributed interconnect circuit with pulse input for L and π models

Length(mm)	Simulated delay L-model (ps)	Power consumption L-model (μW)	Simulated delay π-model (ps)	Power consumption π-model (μW)
1	5.41	0.459	2.82	0.113
2	16.36	0.465	10.75	0.113
3	32.44	0.472	23.68	0.114
4	52.69	0.480	42.14	0.115
5	78.96	0.490	65.91	0.115
6	110.47	0.502	94.87	0.115
7	147.37	0.516	129.15	0.115
8	189.43	0.529	168.70	0.115
9	236.51	0.539	213.55	0.116
10	289.36	0.546	263.72	0.117

Although, researchers have implemented interconnect circuits using ramp as an input supply but pulse response is more preferred since ramp supply does not show any difference in delay values. However, a decrease in power consumption value can be observed because a linear increase in the ramp input signal decreases the power consumption in the circuits. Power

consumption using ramp input supply for lumped and distributed networks can be seen in Table 3.5 and 3.6 respectively. Upon simulation it was observed that by simply increasing a pulse or ramp input supply, the delay was increasing with interconnect length, however, when the delay values were compared there was no change but signal distortion was reduced. This was because the rise time for both the pulses were considered to be same. If the values for rise time differs it will affect the delay in the circuits.

Table 3.5. The power consumption of lumped network for L and π-model from length 1mm to 10mm for ramp input

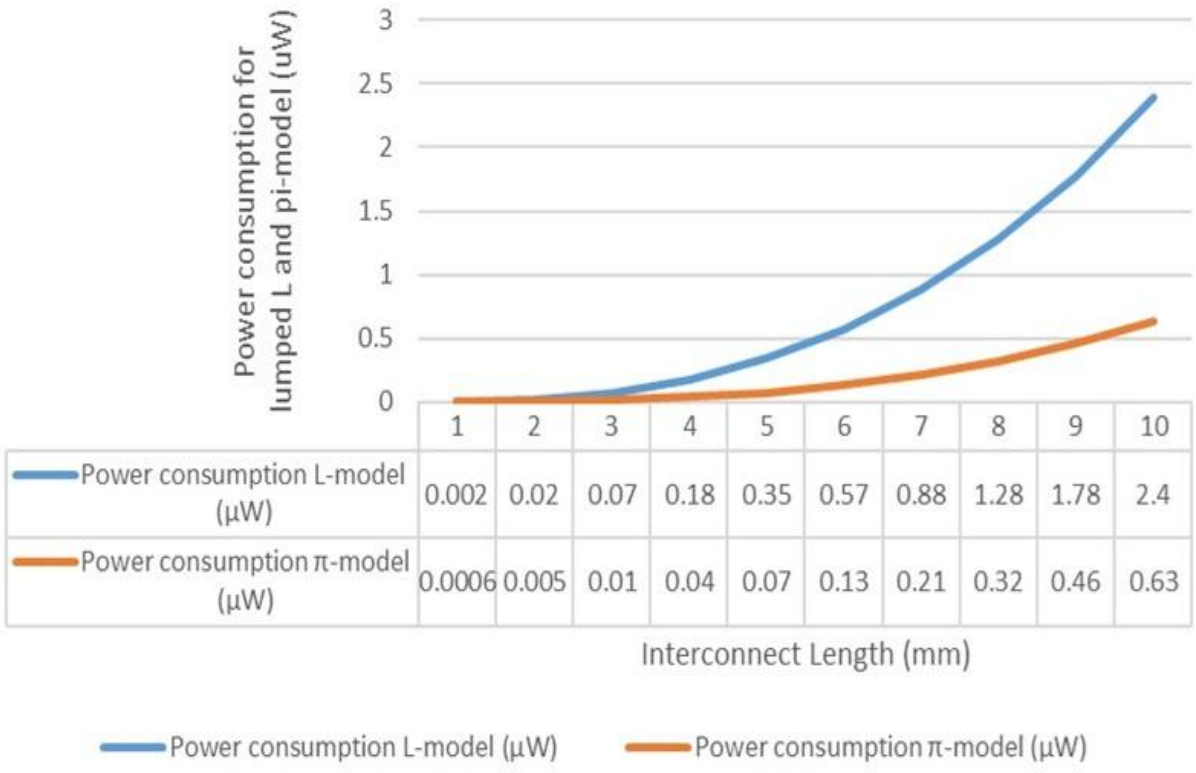
Length(mm)	Power consumption L-model (μW)	Power consumption π-model (μW)
1	0.002	0.0006
2	0.02	0.005
3	0.07	0.01
4	0.18	0.04
5	0.35	0.07
6	0.57	0.13
7	0.88	0.21
8	1.28	0.32
9	1.78	0.46
10	2.40	0.63

Table 3.6. The power consumption of distributed network for L and π-model from length 1mm to 10mm for ramp input

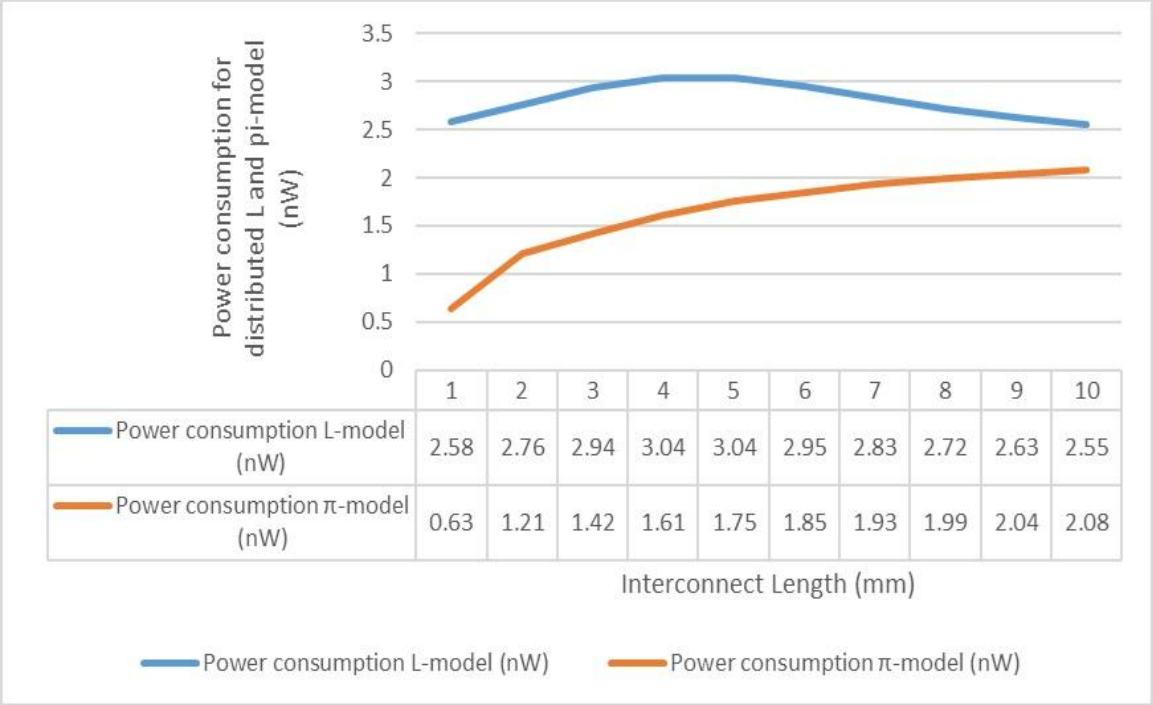
Length(mm)	Power consumption L-model (nW)	Power consumption π-model (nW)
1	2.58	0.63
2	2.76	1.21
3	2.94	1.42

4	3.04	1.61
5	3.04	1.75
6	2.95	1.85
7	2.83	1.93
8	2.72	1.99
9	2.63	2.04
10	2.55	2.08

The power consumption of the lumped and distributed RC connection circuits for varying lengths using a ramp input supply is tabulated in Tables 3.5 and 3.6. Elmore delay estimate yielded computed values that are reasonably close to the simulated values. Furthermore, based on the assessed values, the interconnect lengths can be used to adjust the performance characteristics. The power to interconnect length fluctuations for lumped and distributed circuits with ramp input supply are displayed in Fig. 3.8(a) and (b).



(a)



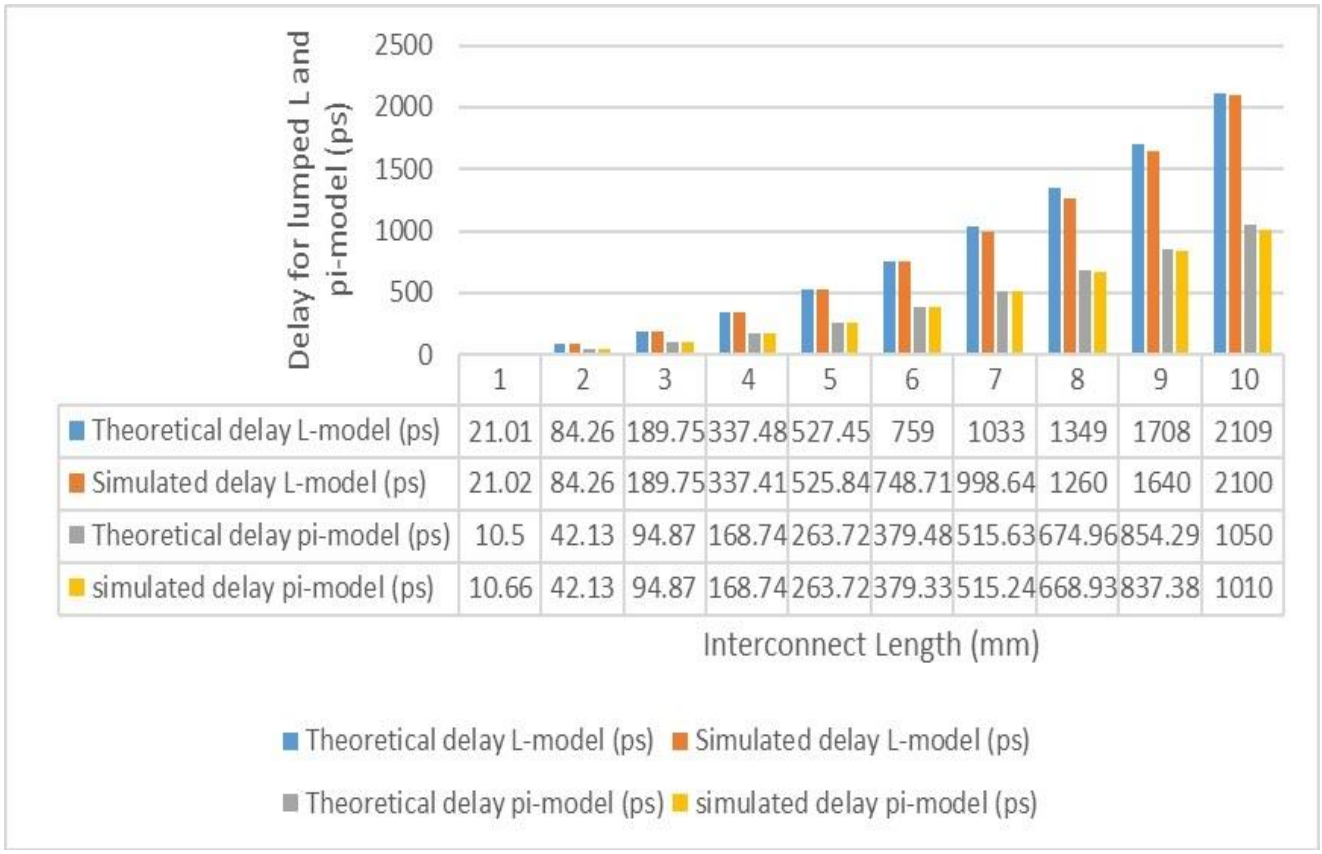
(b)

Fig. 3.8. Power consumption using ramp input supply (a) lumped network (b) distributed network

The non-linear relationship with an increase in connection length is displayed in Figs. 3.8(a) and (b). In the power versus length graph, the power of lumped interconnect circuits increases as the length increases, but the power of distributed circuits using the L-model increases as the length increases and then decreases, and the power of distributed circuits using the π-model increases as the interconnect length increases. Ramp supply also shows that longer wires result in higher power consumption for lumped circuits and lower power consumption for distributed circuits (Fig. 3.8).

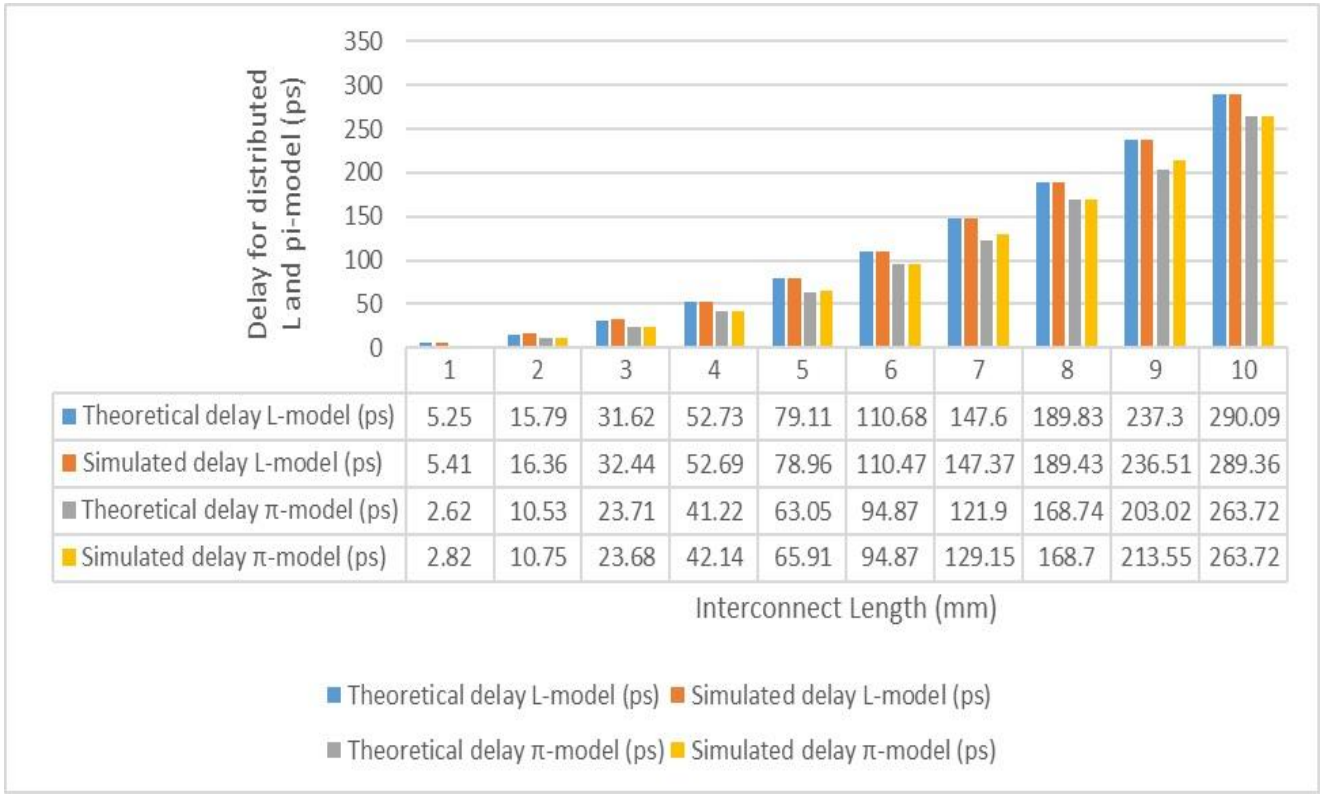
3.4.3 COMPARISON

The comparison of experimental and theoretical values can be done and is depicted using graphical representation for better understanding. Fig. 3.9 and 3.10 shows the delay evaluation for lumped and distributed networks using L and π models for pulse input supply respectively. Fig. 3.11 and 3.12 shows power consumption for lumped and distributed networks using L and π models for pulse input supply respectively.



	1	2	3	4	5	6	7	8	9	10
Theoretical delay L-model (ps)	21.01	84.26	189.75	337.48	527.45	759	1033	1349	1708	2109
Simulated delay L-model (ps)	21.02	84.26	189.75	337.41	525.84	748.71	998.64	1260	1640	2100
Theoretical delay pi-model (ps)	10.5	42.13	94.87	168.74	263.72	379.48	515.63	674.96	854.29	1050
simulated delay pi-model (ps)	10.66	42.13	94.87	168.74	263.72	379.33	515.24	668.93	837.38	1010

Fig. 3.9. The delay evaluation for lumped network using L and π models for pulse input supply



	1	2	3	4	5	6	7	8	9	10
Theoretical delay L-model (ps)	5.25	15.79	31.62	52.73	79.11	110.68	147.6	189.83	237.3	290.09
Simulated delay L-model (ps)	5.41	16.36	32.44	52.69	78.96	110.47	147.37	189.43	236.51	289.36
Theoretical delay π-model (ps)	2.62	10.53	23.71	41.22	63.05	94.87	121.9	168.74	203.02	263.72
Simulated delay π-model (ps)	2.82	10.75	23.68	42.14	65.91	94.87	129.15	168.7	213.55	263.72

Fig. 3.10. The delay evaluation for distributed network using L and π models for pulse input supply.

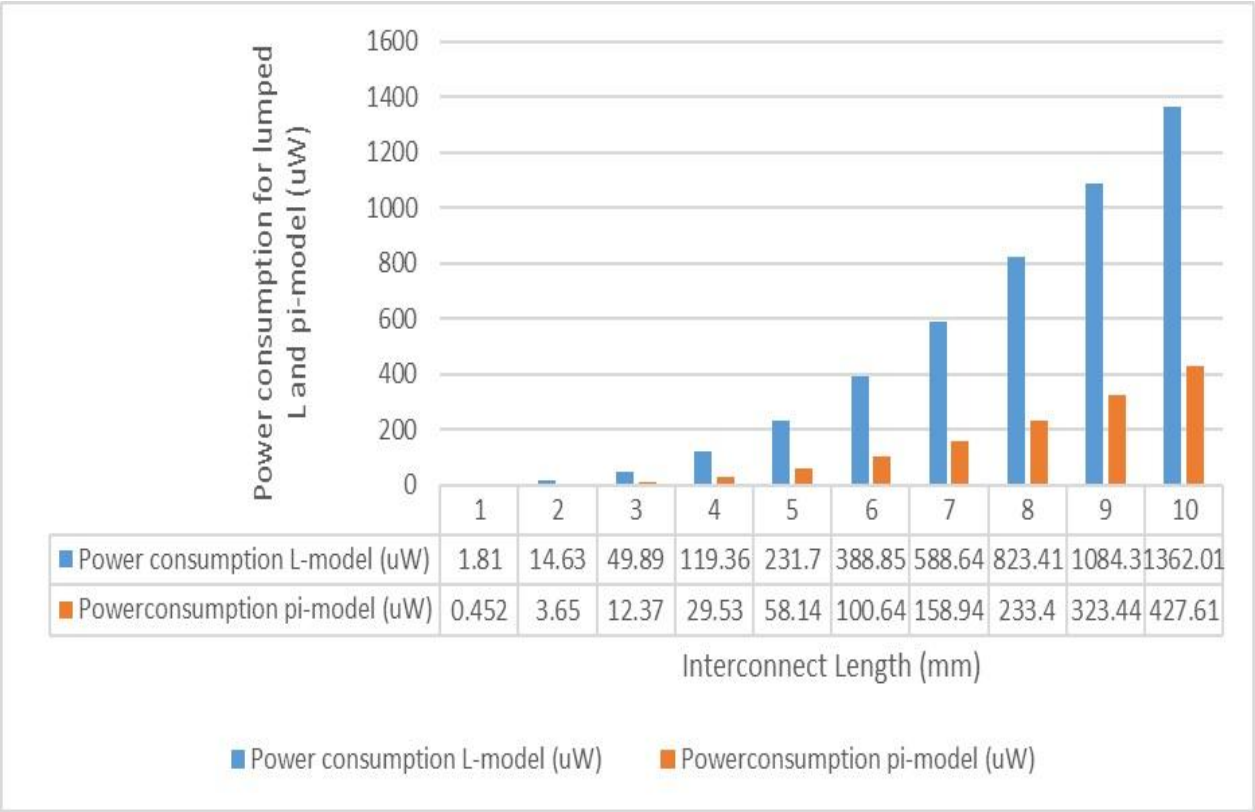


Fig. 3.11. Power consumption for lumped network using L and π models for pulse input supply

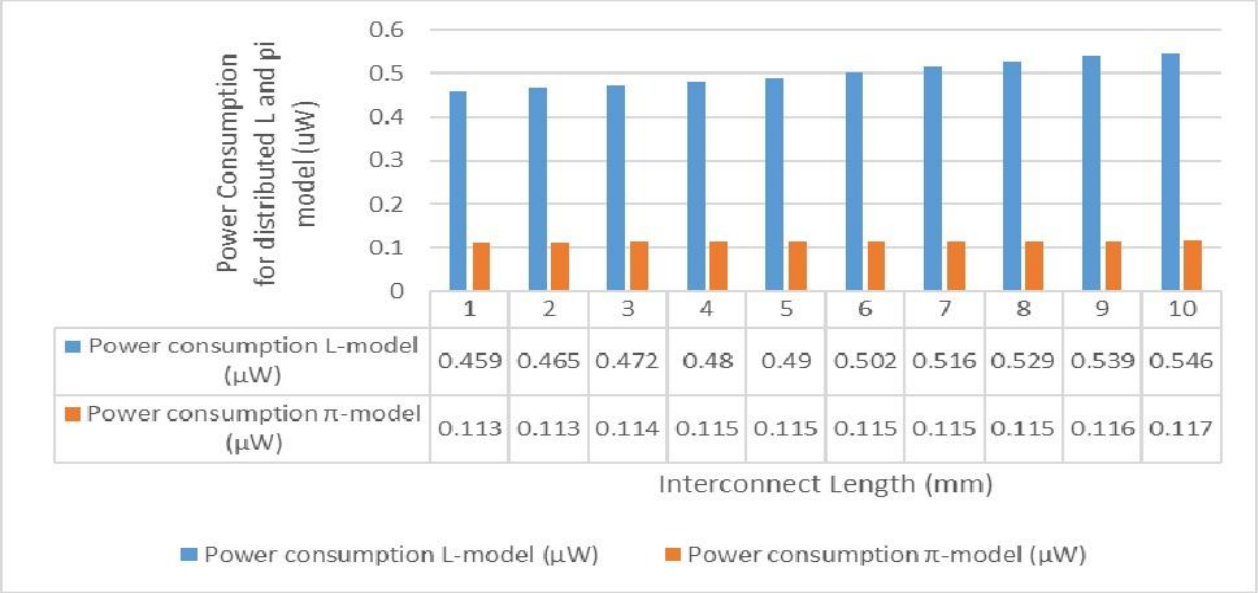


Fig. 3.12. Power consumption for distributed network using L and π models for pulse input supply

The non-linear relationship with the increase in connection length is displayed in Figs. 3.9, 3.10, 3.11, and 3.12. The delay strictly increases with the increase in interconnect length for the delay vs. length graph depicted in Figures 3.9 and 3.10, which shows lumped circuits and dispersed interconnect circuits with varying lengths. Additionally, the graphs' non-linear

relationship exhibits a positive slope. It is confirmed that the impulse response is monotonic by a strictly non-linear increase in delay. In the power vs length graph depicted in Figures 3.11 and 3.12, the power of lumped interconnect circuits rises as the length increases, while the power of dispersed circuits increases slightly as the length increases as well. The graphical representations also show that the power usage increases with interconnect length.

The theoretical and simulated results for the proposed interconnect circuits using L and π-models with different input supplies are compared with other state-of-art techniques. Table 3.7 tabulates the comparison of the proposed technique with the existing ones.

Table 3.7. Comparison with other state-of-art-techniques

Models/Technique			Delay	Power
Proposed interconnect structure (for max L=10mm)	Pulse supply	RC Lumped (L-model)	2.10 ns	1362 µW
		RC Lumped (π-model)	1.01 ns	427.61 µW
		RC Distributed (L-model)	289.36 ps	0.546 µW
		RC Distributed (π-model)	263.72 ps	0.117 µW
Proposed interconnect structure (for max L=10mm)	Ramp supply	RC Lumped (L-model)	2.10 ns	2.40 µW
		RC Lumped (π-model)	1.01 ns	0.63 µW
		RC Distributed (L-model)	290.43 ps	2.55 nW

		RC Distributed (π-model)	263.71 ps	2.08 nW
Ramadass (Pulse supply) [34]		RC Lumped	20.138ns	0.451 µW
		RC Distributed	42.564ns	0.546 µW
Erdemli, E., & Aksoy, M. (Pulse supply) [29]		RC Distributed	41.80ns	-

Increase or decrease in resistance plays an important role in determining the delay and power of an interconnect circuit as resistance acts as an important parasitic component in determining the performance of the interconnect circuit. Since, the proposed interconnect circuit is reducing the resistance by the factor of 4, it will affect the time constant and power consumption in the circuit. As the delay directly depends upon the resistance of the wire (τ=RC) so it can be said that increase in resistance can increase the delay whereas in term of power consumption, the CMOS technology scaling can increase the resistance leading to increase in power [81]. Also, the aggressive down-scaling of Cu interconnect dimensions has led to exponentially increased resistivity, which is referred to as the "size effect" [22]. This effect increases the resistance–capacitance (RC) delay, current-resistance (IR) drop, and power consumption at multiple layers, and thus deteriorates wire's performance. However, in the literature data the interconnect structures do not focus on reducing the resistance value but introduction of a new parameter such as conductance to the interconnect circuits.

In the literature review, it was observed that either modifications were done into Elmore delay estimation using different method [29] or a new parameter was introduced along with main parasitic components that is R, C, and L [35]. However, the need for reduced resistance was still an issue. A novel interconnect structure was implemented and simulated with the reduced value of resistance by the factor of 4. After comparing results with other state-of-art techniques, the power consumption is observed to be improved by 78.5% and delay is observed to be improved by 75.5%. Even though the proposed RC interconnect circuit shows better result in performance but as the wire elongates the delay increases quadratically which can affect the performance of the entire circuit. Therefore, buffers are added in between to linearize the delay.

3.5 CONCLUSION

An inventive interconnect structure with an enhanced Elmore delay estimation model was outlined in this chapter. Additionally, lumped and distributed distribution segments with pulse and ramp inputs were seen in Elmore delay computations for long wires at various connector lengths between 1 and 10 mm. The conclusion drawn from the suggested interconnect structure (H-tree) is as follows:

i. It was determined that when lumped RC networks are used with pulse input signals, both power and delay grow linearly and significantly with increasing connection length, but in distributed RC networks, power increases marginally but delay increases with increasing interconnect length.
ii. For both lumped and distributed networks, the delay for ramp input is nearly the same as that of pulse input supply; however, for lumped circuits, power consumption increases linearly with an increase in interconnect length, while for distributed circuits using the L-model, power increases initially and then decrease with an increase in interconnect length.
iii. In distributed circuits that employ the π-model, the power grows as the interconnection length increases linearly. In light of this, it may be said that distributed networks exhibit more efficient performance metrics than lumped networks.
iv. To lower the interconnect circuits' time constant by lowering their resistance, an optimised Elmore delay estimation was also carried out. In addition to latency, power consumption was found to be optimal when utilising an improved RC model.
v. For all RC networks, a non-linear relationship between delay and power consumption was noted. The Elmore delay is found out to be a non-linear model since for a unit step function, the delay can be expressed by Eq. (3.19):

$$v_i(t) = 1 - e^{-t/T_{Di}} \qquad \text{Eq. (3.19)}$$

where $T_{Di} = \sum_k R_{ki} C_k$

vi. Even though there will be a slight rise in computing costs, the suggested structure performs better in terms of lowering circuit power consumption.

In the future, various materials can be compared to copper material to assess the circuits' performance metrics. Additionally, as technology gets smaller and interconnects longer, the delay grows quadratically, leading to a variety of circuit-level problems. As detailed in more depth in later chapters, these problems are fixed by adding buffers in between the lengthy interconnects to prevent circuit failure and enhance overall performance.

CHAPTER 4

DESIGN AND IMPLEMENTATION OF RC GLOBAL INTERCONNECTS WITH BUFFER INSERTION TECHNIQUE

CHAPTER 4: DESIGN AND IMPLEMENTATION OF RC GLOBAL INTERCONNECTS WITH BUFFER INSERTION TECHNIQUES

This chapter is dedicated to the study of buffer insertion and the challenges that arise in long wires as interconnect length and resistance increase. An overview of inserting buffers and repeaters in between long wires is given in this chapter. A general introduction is provided in section 4.1. Various buffer types are covered in section 4.2. The suggested method for connection architectures, which is followed by energy recovery logic, is explained in Section 4.3. Results and discussion are presented in Section 4.4, along with the comparison and experimental analysis. Finally, the chapter's conclusion is given in section 4.5.

4.1 INTRODUCTION

Wire delay grows quadratically with interconnect length even when a wire is well-optimized to minimise resistance and capacitance per unit length. For very long wires, this quadratic delay characteristics cannot be tolerated as it would become so long even to dominate gate delay. Small interconnects generally known as local interconnects cannot be bothered with quadratic delay but the problematic issue arises when the wire becomes very long generally global interconnects. These wires are associated with clocks, buses, and other major signals. Since, the issue of quadratic delay becomes necessary to address it becomes important to find a standard solution of inserting buffers/repeaters in between periodically along the long wires. A long wire eventually becomes more advantageous to cut in half and insert a repeater or a buffer to drive the other half. Contributing 1/4 of the RC delay to either side of the wire reduces the total RC delay by a factor of 2 [87]. This converts the quadratic delay of long wires into linear delay. However, the number of buffers to be inserted in between is also important to be studied as if too many buffers are inserted the delay increases due to buffers themselves and if too less buffers are inserted then the long wires are prone to quadratic delay effect. The size of buffers to be inserted also becomes an important factor to determine the area and the performance of the interconnect circuit design. Thus, finding the optimum number of equal-sized buffers needed to determine and minimise the delay of the global interconnects is known as buffer insertion problem.

4.2 BUFFER INSERTION IN LONG WIRES

It is well known that the wires are driven by the repeaters connected to them as shown in Fig. 4.1 [88].

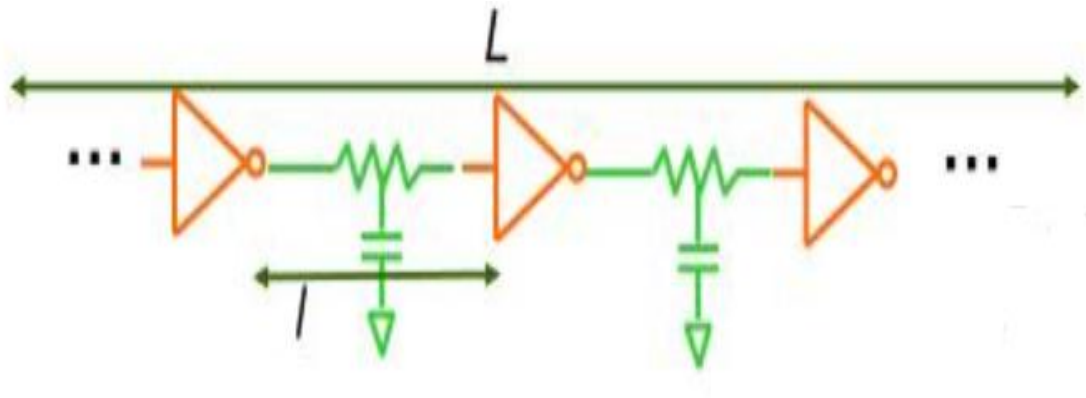


Fig. 4.1. Global interconnect with buffers insertion [85]

In Fig. 4.1, L represents total length of the interconnect, and l represents per unit length. As indicated in Fig. 4.2, the per unit resistance and capacitance of the long connection, or R_{int} and C_{int}, respectively, were taken into consideration to determine the ideal number and size of buffers to be inserted.

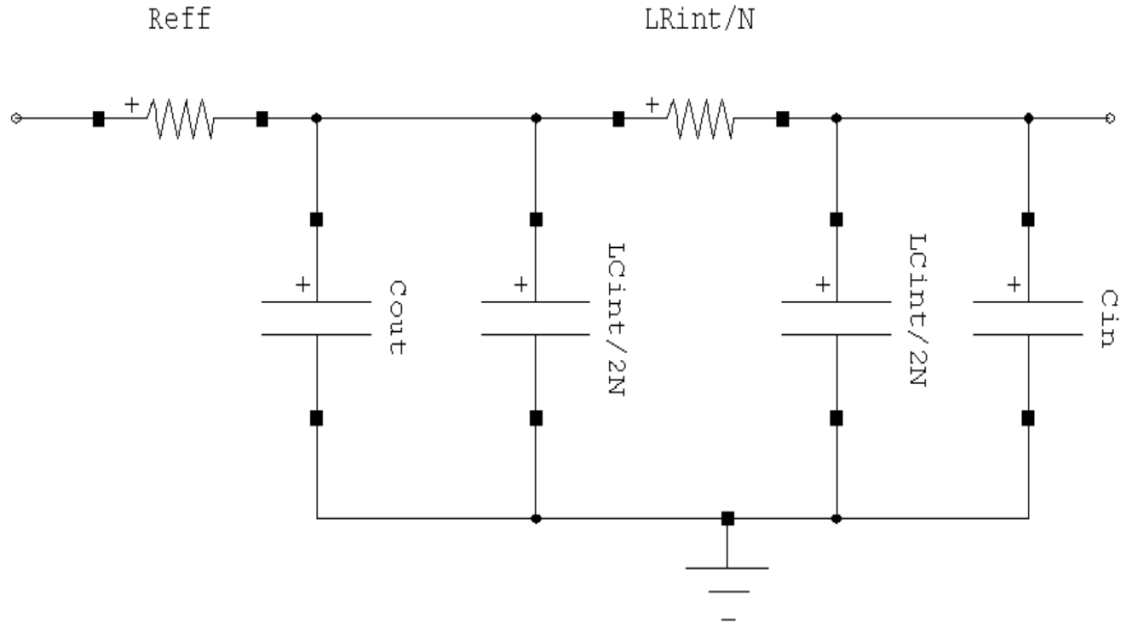


Fig. 4.2. One segment of a long wire

Let N be the optimum number of buffers to be inserted in between including the first buffer. Each segment includes a buffer driving the interconnect and a gate load. Considering

minimum size of the buffers to 1X, the corresponding input and output capacitances as shown in Fig. 4.2 can be expressed by Eq. (4.1) and Eq. (4.2) respectively [16].

$$C_{in} = C_G(1+\beta) \tag{4.1}$$

$$C_{out} = C_J(1+\beta) \tag{4.2}$$

Where C_G is the product of C_g and W and C_J is the product of C_{eff} and W (where W is the width of NMOS of 1X buffer circuit), β is the ratio of PMOS to NMOS device size. For a buffer larger than 1X buffer, let M be the multiplier. For M times larger buffer, the input and output capacitances can be expressed by Eq. (4.3) and Eq. (4.4) respectively [16].

$$C_{in} = M * C_G(1+\beta) \tag{4.3}$$

$$C_{out} = M * C_J(1+\beta) \tag{4.4}$$

$$R_{eff} = R_{eqn}/M \tag{4.5}$$

Where R_{eff} is the resistance of buffer for size M. The Elmore delay for one segment of the wire can be expressed by the Eq. (4.6).

$$t_{seg} = \frac{R_{eqn}}{M}\left(MC_J(1+\beta) + \frac{LC_{int}}{2N}\right) + \left\{\frac{R_{eqn}}{M} + \frac{LR_{int}}{N}\right\}\left(\frac{LC_{int}}{2N} + MC_G(1+\beta)\right) \tag{4.6}$$

Using Eq. (4.6) total delay can be computed as the total delay is N times the segment delay. Thus, the total delay for a wire can be expressed by Eq. (4.7) [16].

$$\begin{aligned} t_{total} &= t_{seg} * N \\ &= N(C_G + C_J)R_{eqn}(1+\beta) + \left(C_G(1+\beta)MR_{int} + \frac{R_{eqn}C_{int}}{M}\right)L \\ &\quad + \left(\frac{C_{int}R_{int}}{2N^2}\right)L^2 \end{aligned} \tag{4.7}$$

Where $N(C_G + C_J)R_{eqn}(1+\beta)$ is the delay for buffer only, $\left(C_G(1+\beta)MR_{int} + \frac{R_{eqn}C_{int}}{M}\right)L$ is the delay for buffer and interconnect both, and $\left(\frac{C_{int}R_{int}}{2N^2}\right)L^2$ is the delay for interconnect only. For optimal values of N and M, derivative is applied to Eq. (4.7) with respect to each variable. The number of wire segments (N) to be done to insert optimal number of buffers can be expressed by Eq. (4.8) and (4.9) respectively [16].

$$\frac{\partial t_{total}}{\partial N} = 0 = \left(C_G + C_J\right)R_{eqn}(1+\beta) - \left(\frac{C_{int}R_{int}}{2N^2}\right)L^2 \tag{4.8}$$

$$N = \sqrt{\frac{\left(\frac{C_{int}R_{int}}{2}\right)L^2}{\left(C_G + C_J\right)R_{eqn}(1+\beta)}} \tag{4.9}$$

The buffer size (M) assuming all buffers to be of equal size can be expressed using Eq. (4.10) and (4.11) respectively [16].

$$\frac{\partial t_{total}}{\partial M} = 0 = C_G(1+\beta)LR_{int} - \frac{LR_{eqn}C_{int}}{M} \tag{4.10}$$

$$M = \sqrt{\frac{R_{eqn}C_{int}}{C_G(1+\beta)R_{int}}} \tag{4.11}$$

Using the values of N and M, an optimum delay through interconnect can be evaluated. According to Eq. (4.7), the middle part of the total delay is dependent on M. If the two expressions are kept to be equal, an optimum value of M can be obtained. This value does not depend on the length of the interconnect but rather the physical characteristics of the transistors and wires. Therefore, this value can be computed once the process parameters are defined.

4.2.1 TYPES OF BUFFERS/REPEATERS

The continuous scaling of VLSI technology has led to the increasing importance of interconnect performance in the overall system performance. As interconnect lengths grow, the need for effective buffer or repeater insertion strategies becomes critical to maintain signal integrity and power efficiency [89]. The type of repeater or buffer needed for a given circuit might determine its specific requirements.

i. CMOS inverter

The most commonly used buffer/repeater is the CMOS inverter circuit. It is one of the simplest and compact buffer circuit which can be used to drive an interconnect circuit. The CMOS inverter is the simplest and most straightforward circuit for the dynamic switching operation. As seen in Fig. 4.3, it comprises a pull-up and pull-down network that connects it to an input source and extracts the output.

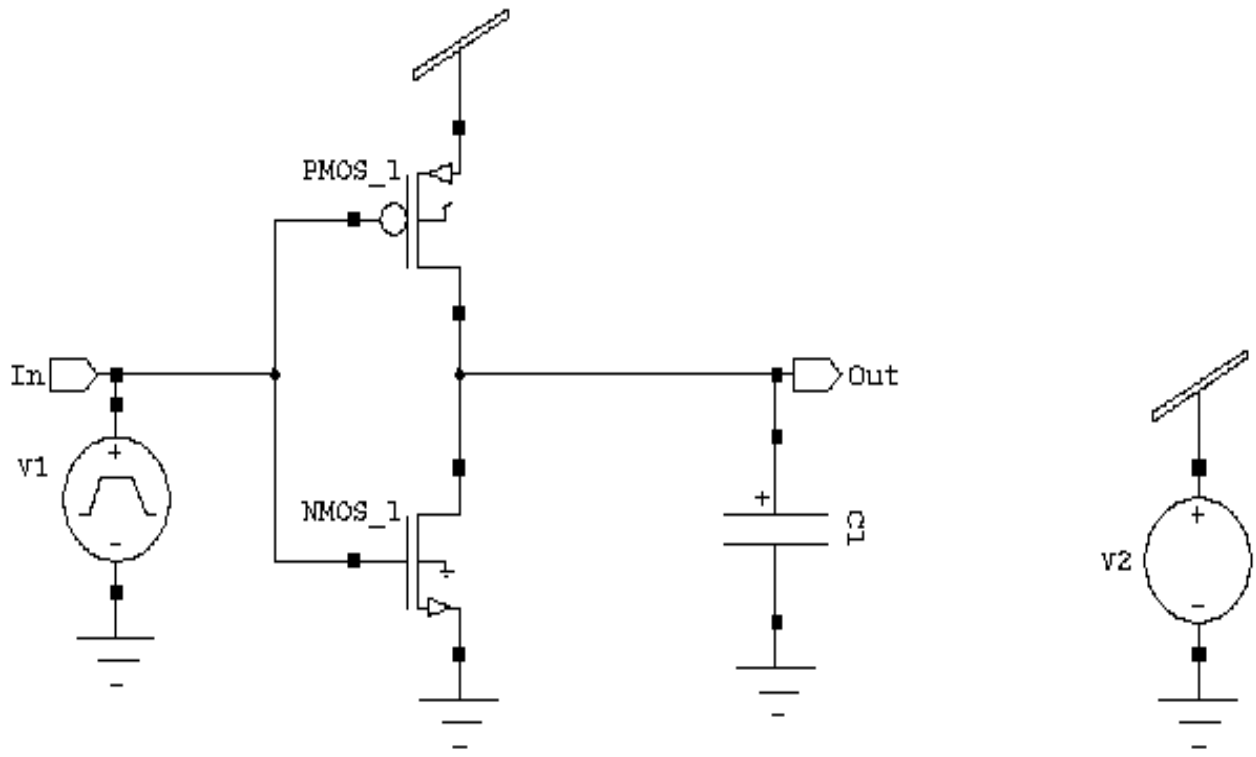


Fig. 4.3. Inverter circuit [90]

The load capacitor in Fig. 4.3 is linked to the device's output, which when the input is low and PMOS is triggered, charges to a high voltage. Similar to this, when the input is high, the load capacitor's charge is discharged to zero, activating NMOS. This type of switching is known as dynamic switching.

ii. Schmitt trigger

Even still, the circuit lacks noise immunity due to its minuscule complexity. To increase the noise tolerance of the circuit, the CMOS inverter is flipped using a Schmitt trigger. The Schmitt trigger circuit is a typical buffer circuit with hysteresis input-output characteristics. These characteristics reject noise, stabilising the circuit. The Schmitt trigger circuit provides noise shielding in the digital and analogue domains due to its hysteresis feature [91]. When

used as a buffer, the Schmitt trigger circuit requires less power and delay than a CMOS inverter since it is immune to noise. The basic Schmitt trigger circuit is depicted in Fig. 4.4.

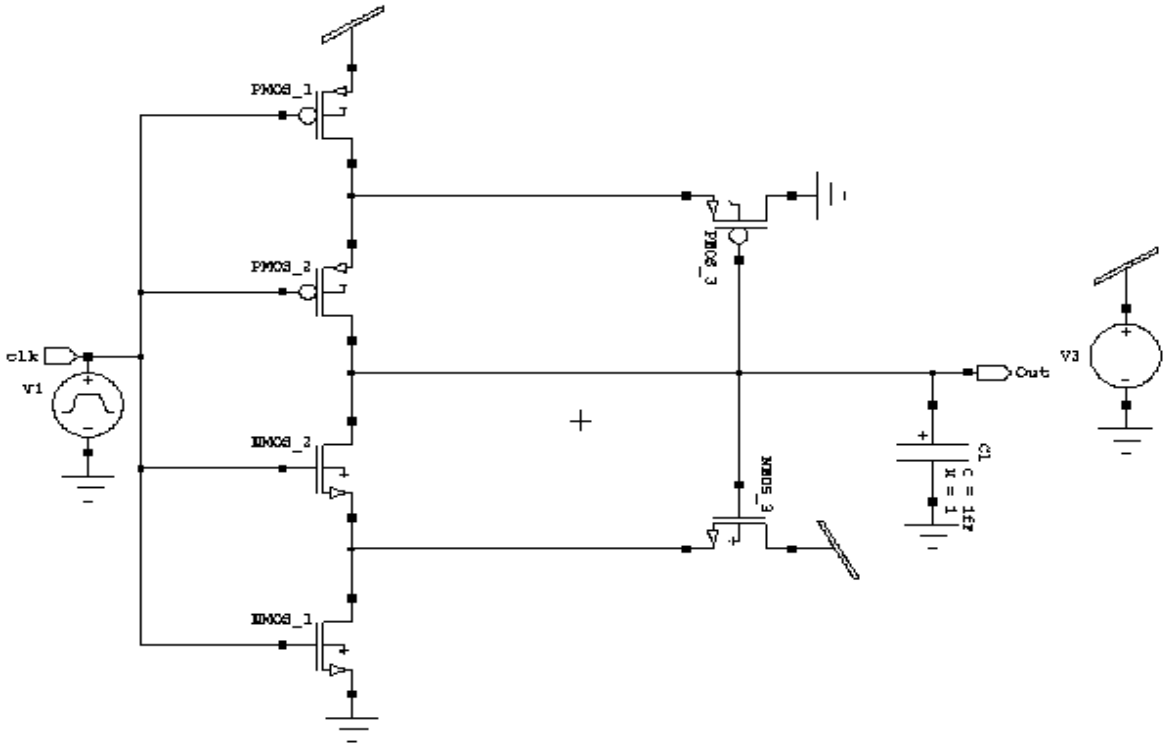


Fig. 4.4. Schmitt trigger circuit [90]

The Schmitt Trigger provides two different threshold voltage levels for the lowering and rising edges. This is helpful since it can avoid mistakes when the user wants to acquire square wave signals from noisy input signals. In total six transistors (6T) three PMOS and three NMOS are used in it. It's a straight forward inverter circuit that serves as a buffer, and two extra transistors give the circuit hysteresis and noise immunity. To provide noise immunity through a hysteresis curve that a basic inverter cannot, the Schmitt trigger circuit also employs dynamic switching with extra transistors [90]. In Fig. 4.4, six transistors are connected with each other to provide the function of an inverter circuit along with noise immunity. When the input of the circuit is held zero, PMOS 1 and PMOS 2 gets ON and output gets charged to V_{dd}. Due to high output, NMOS 3 gets ON and gives path to V_{dd}. Similarly, when the input is changed from zero to one, NMOS 1 and NMOS 2 gets ON, discharging output to zero. But an additional current is required that goes from NMOS 3 to ground. This happens when output becomes zero and NMOS 3 gets OFF. This will give a threshold voltage point when input goes from zero to V_{dd}. Now, NMOS 1 and NMOS 2 are

ON and load capacitance discharges to zero. But PMOS 3 gets ON and will give path to ground. When the input is switched again, PMOS 1 and PMOS 2 gets ON but an additional current is required to turn OFF PMOS 3. This gives the threshold voltage point from V_{dd} to zero and this property is called hysteresis.

iii. CMOS inverter using FinFET technology

Similar to MOSFET, FinFET is a switching device. It's a non-planner device with a three-dimensional structure. The gate in a FinFET is wrapped around the channel to aid in channel control. FinFET preserves the I_{on}/I_{off} ratio, has low sub threshold leakage, and solves the Drain Induced Barrier Lowering (DIBL) problem. They will be replaced with MOSFETs. Compared to CMOS digital inverter circuits, FinFET offers a number of benefits. Among the benefits are lower leakage current and faster switching, which reduces delay. However, the CMOS technology requires less fabrication investment and is quite similar to planner bulk technology. Therefore, converting bulk technology libraries that already exist into CMOS libraries is simple. One more benefit of CMOS over FinFET is its excellent back gate bias choice. The threshold voltage provided by CMOS devices (V_t) can be controlled by setting up a back gate zone. It is hence appropriate for low-power applications. FinFET technology can be applied to CMOS transistors to create an inverter circuit. The FinFET-based CMOS inverter circuit is depicted in Fig. 4.5.

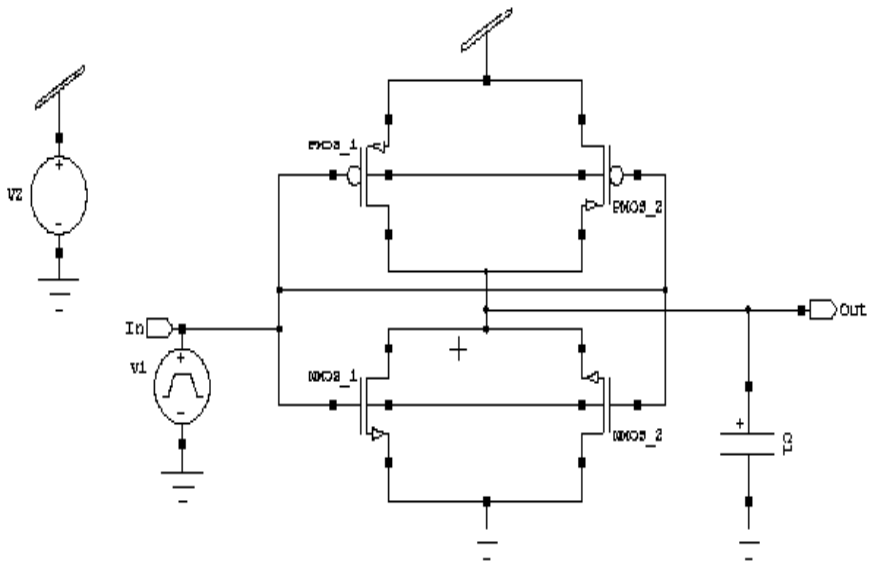


Fig. 4.5. CMOS inverter circuit using FinFET technology [90]

The two connected PMOS make up the pull-up network of the inverter circuit, as seen in Fig. 4.5, while the two linked NMOS make up the pull-down network. Since the two transistors' gates are linked, the circuit is known as employing FinFET technology. It is commonly known that FinFET technology performs better than CMOS technology in terms of latency and power consumption. Still, some power dissipation occurs, which eventually turns into heat. Furthermore, as technology moves towards compact devices (portable ones), heat emission or temperature rise in the circuit design can be a major setback. These issues can be avoided with the use of the adiabatic process. Adiabatic circuits that use adiabatic switching have either very little or no heat transfer since most of the power is recycled or conserved.

Whatever type of buffer or repeater used, the algorithm for insertion problem remains the same. Optimum length, size, and number of buffers must be identified before inserting them in between long wires. A concise algorithm can be used to add buffers in between the lengthy wires. Algorithm 4.1 illustrates how the buffer insertion approach is carried out.

Algorithm 4.1: Adiabatic Dynamic Logic-Based Novel Interconnect Structure with Buffer Insertion

---

Input: Interconnect
Output: Delay, Power consumption

Start

Step 1: Determine the total resistance and capacitance of a wire with length (L).

Step 2: The interconnection is separated into (N+1) segments, and N number of buffers needs to be placed. This is the optimal number of buffers to insert.

Step 3: Calculate the overall time after inserting the buffer: N x one segment's delay.

Step 4: Apply a derivative to each variable to determine the value of N.

Step 5: Reduce latency by optimising the buffer's size.

End

The effect of process, voltage, and temperature changes on the power and performance of the interconnect-buffer system is a significant obstacle in buffer/repeater insertion [89]. Although, Schmitt trigger circuit provides noise immunity to the circuits and consumes less power when compared with the CMOS inverter circuit but it is important to note that the less the technology, more power will be consumed to operate properly. And more power consumption will eventually release more power that means more heat generation. Major concern is the power consumption as well as power dissipation that are to be addressed using various techniques or methods. One such technique can be Energy Recovery Logic.

4.3 ENERGY RECOVERY LOGIC

The necessity to reduce power consumption and, consequently, heat dissipation in VLSI circuits, along with the growing popularity of portable systems, have driven notable developments in low-power design in recent years. As a result, there has been an explosion of activity and quick evolution in the field of CMOS design, which deals with the low-power design of digital integrated circuits. High-performance digital systems such as microprocessors, digital signal processors (DSPs), and other applications are becoming more and more dependent on low-power architecture [92]. Chips with high clock frequencies are designed with increasing complexity as a result of increased operating speed and chip density. In general, the chip's temperature and power dissipation increase linearly with increasing clock frequency. It becomes crucial to take into account the cost of packing, cooling, and heat removal because the chip temperature must be kept at a certain level [93]. Digital systems can accomplish low power consumption through a variety of approaches, ranging from algorithmic to device/process level. The connection qualities, device geometries, and device characteristics (such as threshold voltage) all play a major role in reducing power usage. Transistor power dissipation can be decreased by circuit-level techniques such as appropriate circuit design style selection, voltage swing reduction, and timing systems. Architecture-level techniques include things like intelligent power management of individual system blocks, parallelism and utilisation of pipelining, and bus structure design. Lastly, by carefully choosing the data processing algorithms to limit the amount of switching events for a particular activity, the system's power consumption can be decreased. The notion of adiabatic logic will receive particular attention in this chapter since it is an advantageous way to lower power consumption by reverting back a portion of power back to the supply for reuse.

Energy is transferred with each switching event in conventional level-restoring CMOS logic circuits with rail-to-rail output voltage swings, either from the power supply to the output node or from the output node to the ground. During the output's 0-to-V_{DD} transition, the whole output charge $Q = C_{load}V_{DD}$ is drawn at a steady voltage from the power supply. Thus, the energy of the type $E_{supply} = C_{load}V_{DD}^2$ is collected from the power supply during this transition. At the end of the transition, energy $E_{stored} = C_{load}\,V_{DD}^2/2$ is stored on the output node when its capacitance is charged to the voltage level V_{DD}. As a result, only half of the power source's energy is used by the output node; the other half is lost throughout the PMOS network. The energy contained in the load capacitance in the NMOS network dissipates as a result of a subsequent VDD-to-0 transition of the output node, and no charge is drawn from the power source. The circuit designer can minimise switching occurrences, lower node capacitance, lessen voltage swings or use a combination of these techniques to lower dissipation. The energy that is extracted from the power source, however, is only ever used once before disappearing. The energy extracted from the power source must be recycled using several methods to increase the energy efficiency of logic circuits. A new family of logic circuits called adiabatic logic makes it possible to recycle, or put to better use, some of the energy that is gathered from the power source and further reduce the energy consumed during switching events. To do this, occasionally major modifications must be made to the circuit architecture and operating principles. The amount of energy that can be recycled using adiabatic processes depends on voltage swing, switching speed, and manufacturing technique. The term "adiabatic" is frequently used to describe thermodynamic processes that do not lose energy as heat is dissipated or exchange energy with the environment. The electric charge transfer between a circuit's nodes will be interpreted as the process in this case, and various techniques to lessen energy loss—also known as heat dissipation—during charge transfer events will be examined. In real-world situations, adiabatic and non-adiabatic components typically make up the energy dissipation linked to a charge transfer event. Consequently, it might not be able to eliminate energy loss, even at very high switching speeds.

4.3.1 ADIABATIC DYNAMIC LOGIC

The logic uses adiabatic switching in dynamic CMOS circuits, as the name implies. Most of the energy lost from the circuit is conserved and reused because of this process. It is well known that complementary transistors coupled to the clock and an n-transistor network make

up a dynamic CMOS circuit. Comparing this circuit to static CMOS circuits (2N), fewer transistors (N + 2) are used. Furthermore, the circuits experience no static power loss [94]. Regarding the adiabatic switching procedure, it operates in two modes: evaluation and pre-charge. The potential across the switching devices needs to be maintained low to consume less power throughout the adiabatic switching process to achieve adiabatic swapping. By raising the capacitance to a high voltage using a time-varying source, the load is charged. Similarly, the signal can be angled back to 0V to complete the discharging process.

Examine the circuit as shown in Fig. 4.6, where a steady current source charges a load capacitance.

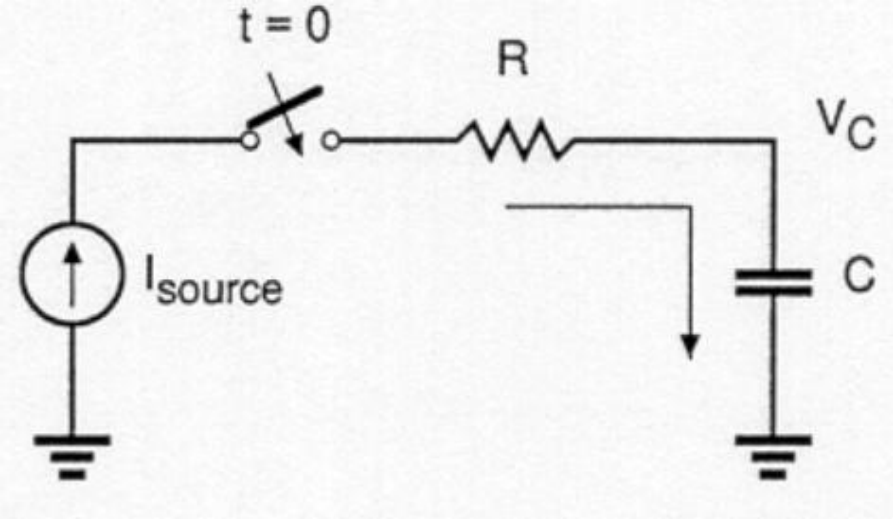


Fig. 4.6. An RC circuit charged with a constant current source [93]

Except for the fact that conventional CMOS circuits charge the output capacitance via a constant voltage source rather than a constant current source, this circuit is comparable to the related circuit used to simulate the charge-up event. Here, R represents the PMOS network's on-resistance. Recall that a linear voltage ramp corresponds to a constant charging current. Assuming that the capacitance-voltage VC is initially equal to zero, the voltage variation as a function of time can be calculated using Eq. (4.12) [94].

$$V_C(t) = \frac{1}{C} * I * t \tag{4.12}$$

Consequently, the charging current may be expressed as a simple function of V_C and time t using Eq. (4.13) [93].

$$I = \frac{V_C(t)}{t} * C \tag{4.13}$$

The amount of energy wasted in the resistor R from t = 0 to t = T can be expressed using Eq. (4.14) [93].

$$E_{diss} = R \int_0^T I^2 dt = I^2 * R * T \tag{4.14}$$

The dissipated energy can alternatively be stated by Eq. (4.15) by combining Eqs. (4.13) and (4.14).

$$E_{diss} = \frac{RC}{T} * C * V_C^2(t) \tag{4.15}$$

Equation (4.15) allows for the conclusion of some of the observations. First, if the charging time T is greater than two RC, less energy is consumed than in an ordinary situation. Since E_{diss} is inversely proportional to T, in reality, the wasted energy can be made arbitrarily little by prolonging the charging period. Furthermore, it is demonstrated that the energy wasted is proportionate to the resistance R, in contrast to the typical scenario in which the dissipation is dependent upon the voltage swing and capacitance. Less energy will be dissipated if the PMOS network's on-resistance is decreased. It is evident that throughout the constant current charging process, energy is successfully transmitted from the power supply to the capacitance of the load. By switching the current source's direction, which permits the charge to return from the capacitance to the supply, some of the energy that has been so stored in the capacitor can also be recovered. Since energy in typical CMOS circuitry evaporates after a single application, adiabatic operation is the only way to take advantage of this opportunity. There is no doubt that the circuit's energy has to be replenished by the constant-current power supply. Therefore, non-standard power sources with time-varying voltage also referred to as pulsed power supplies are needed for adiabatic logic circuits. Additionally, Fig. 4.7 as illustrated can be used to demonstrate the adiabatic switching.

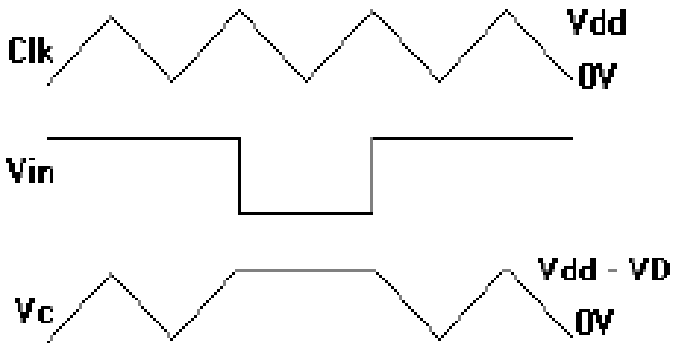


Fig. 4.7. Adiabatic switching process

Adiabatic switching comprises 2 modes of operation namely pre-charge and evaluation mode.

i. Pre-charge mode: when the clock is high, diode is on and the output is charged to V_{dd}-V_d where V_{dd} is the input supply provided to the signal and V_d is some voltage drop across it.
ii. Evaluation mode: depends on input that is if clock is low and input is high, output gets discharged and if clock and input both are low, charge is retained.

Since adiabatic logic is defined to conserve and recycle power in the circuits, it can be used into the buffer circuits for less power dissipation as well. Different buffers with adiabatic dynamic logic can be observed such as:

i. Schmitt trigger inverter circuit using energy recovery logic

The design consists of an n-transistor network tied to the input power source and conventional transistors connected to a clock. Even though dynamic CMOS circuits reduce static power, some power utilisation issues persist. The increasing demand for small and portable electronics has led to the need for smaller and more power-efficient integrated circuit designs [91].

Adiabatic methods, which save the highest possible power while reusing the energy discharged from the circuits, can be considered to increase circuit power. Via an ADL circuit, adiabatic switching is used in dynamic circuits. Fig. 4.8 [92] illustrates a suggested Schmitt trigger circuit with adiabatic switching.

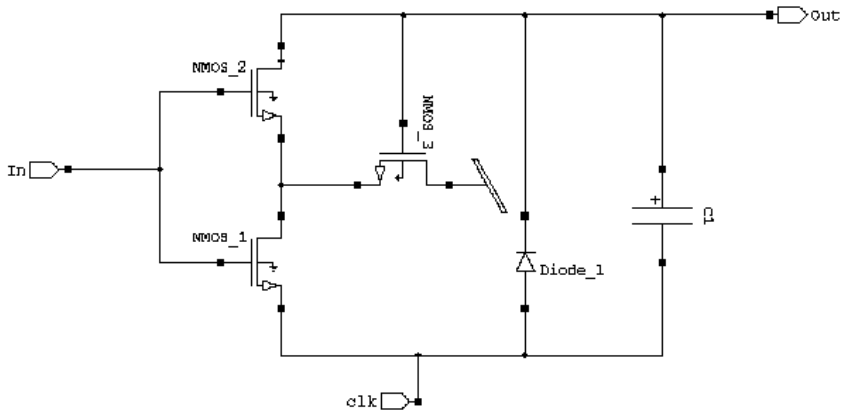


Fig. 4.8. A Schmitt trigger circuit with adiabatic switching [59]

ii. CMOS inverter circuit with FinFET technology using energy recovery logic

This proposed circuit applies adiabatic switching for low power consumption and also makes use of dynamic CMOS logic. The CMOS inverter circuit with adiabatic switching is depicted in Fig. 4.9.

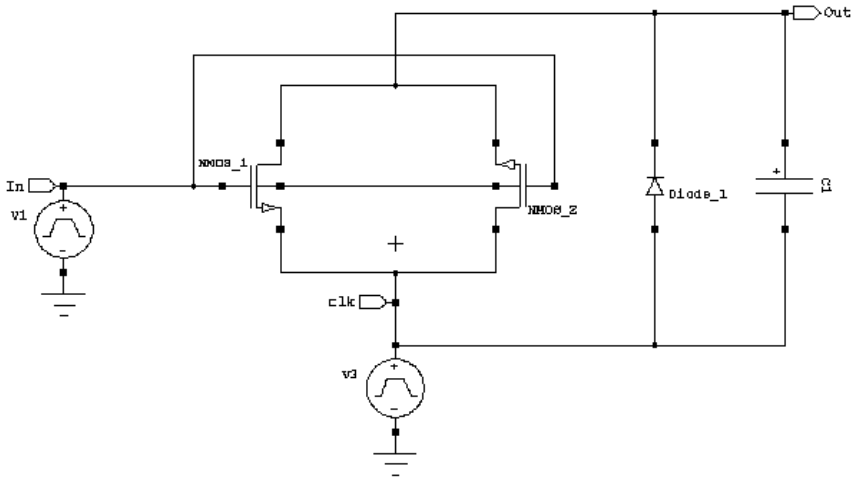


Fig. 4.9. CMOS inverter circuit using FinFET technology with adiabatic switching [57]

An inverter circuit utilising FinFET technology comprises a pull-down network, a diode, and a capacitor that are connected in parallel. It is called FinFET because both the gates are connected together.

4.4 RESULTS AND DISCUSSION

The interconnect circuit is fitted with various buffer types, and the power performance of each kind was assessed. Compared to the NMOS transistor, the PMOS transistor is thought to

have twice the width. An input pulse signal with a 500 ns duration and a 5 ns rise and fall time is applied for adiabatic switching logic. A ramp signal with a 200 ns period and a 100 ns rise and fall time is supplied with the clock signal. 1fF is the load capacitance [90].

4.4.1 INTERCONNECT CIRCUIT (H-MODEL) WITH SCHMITT TRIGGER AS A BUFFER USING ENERGY RECOVERY LOGIC

Evaluation and pre-charge are the two modes of operation. The clock in the pre-charge mode oscillates between 0 and VDD. The output is charged to logic high with a diode drop voltage when the diode is turned on [95]. In the evaluation mode, the clock oscillates between VDD and 0. The kind of input determines the diode's output since it is currently reverse-biased. The output is fully depleted if the supply voltage reaches logic 1. The load capacitance maintains the charge if the supply voltage drops to logic 0. Figure 4.10 shows the Schmitt trigger circuit with the energy recovery logic functioning as a buffer between global connections.

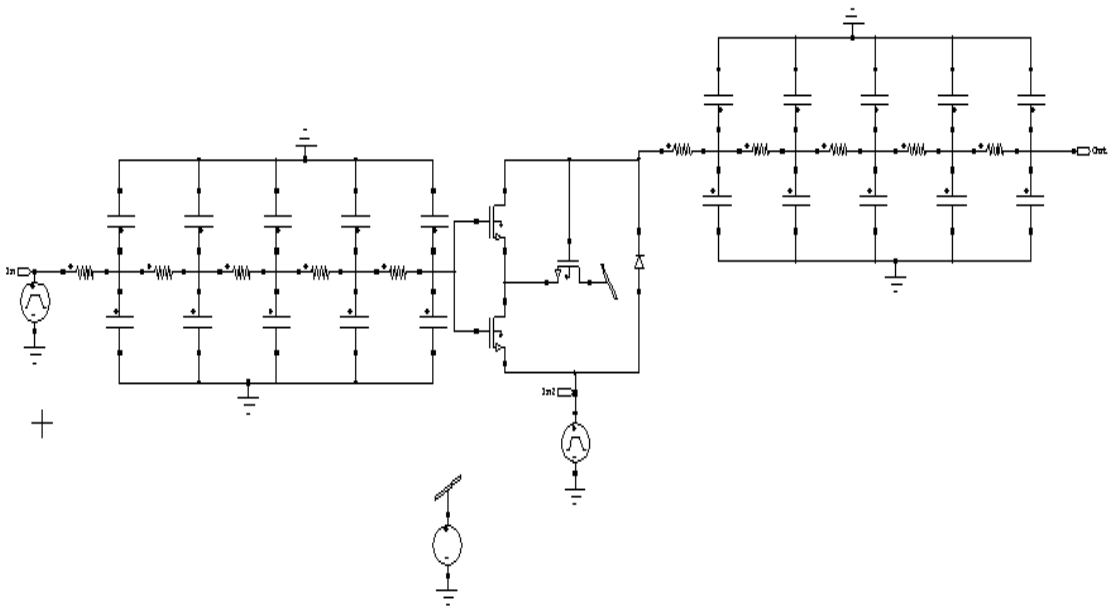


Fig. 4.10. The proposed interconnect circuit with Schmitt trigger as a buffer in between global interconnect

It was found that the simulated Schmitt trigger circuit, which included energy recovery logic, required 3.20 pW of power. The transient analysis of the charge storage situation in the simulated circuit is shown in Fig. 4.11.

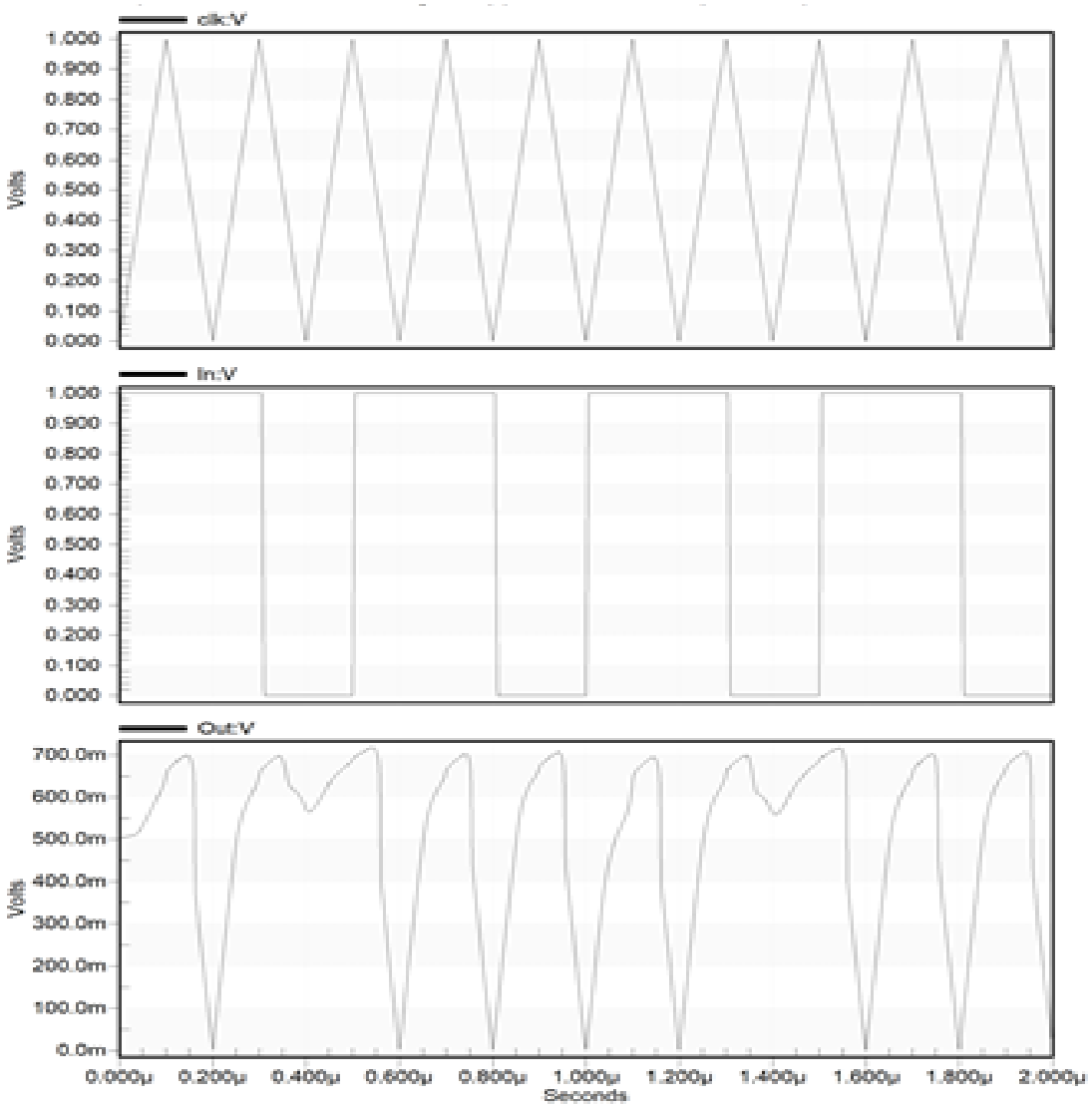


Fig. 4.11. Transient analysis

As illustrated in Fig. 4.11, the output flips to logic 1 with a diode drop voltage of 0.7V as the clock signal (ramp) rises to logic 1. The term "pre-charge phase" describes this working condition. The output when the clock signal changes from logic 1 to logic 0 depends on the type of input. The output fully drains when the input supply is logic 1 with a descending ramp. The output maintains its charge if the input supply is logic zero with a descending ramp. The evaluation phase is the name given to this operational plan. By using less power from the input source, the stored charge is further utilised during the evaluation process.

4.4.2 INTERCONNECT CIRCUIT (H-MODEL) WITH CMOS INVERTER USING FINFET TECHNOLOGY AS A BUFFER USING ENERGY RECOVERY LOGIC

In the suggested circuit, the pull-down network, diode, and load capacitor are connected in parallel using 45nm technology, which has twice the PMOS width compared to the NMOS width. An adiabatic switching process occurs in the circuit. Fig. 4.12 depicts the connection circuit with an inverter serving as a buffer.

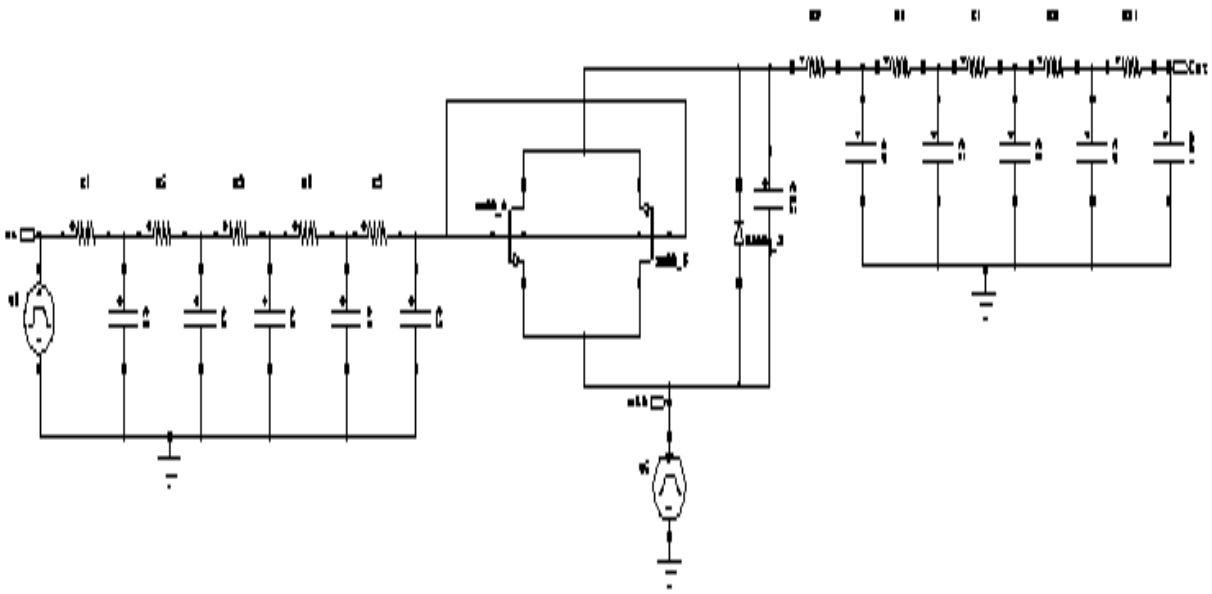


Fig. 4.12. Interconnect circuit with CMOS buffer using FinFET technology with energy recovery logic

It's an additional method of cutting down on power usage in an interconnect circuit. It can offer reduced latency or faster switching speeds. This circuit applies adiabatic switching for low power consumption and also makes use of dynamic CMOS logic. The reported power consumption of the connection circuit, which functions as a buffer circuit using FinFET technology and a CMOS inverter, is 15.37 pW.

4.4.3 COMPARISON OF RESULT

The power consumption of RC interconnect circuits with buffer insertion—using both kinds of buffers with energy recovery logic is compared in Table 4.1.

Table 4.1. The power consumption of RC interconnect circuits with buffer insertion is compared using both types of buffers and energy recovery logic.

Technique used	Power consumption (W)
Interconnect circuit with CMOS inverter	2.2nW
Interconnect circuit with CMOS inverter using FinFET technology	0.40nW
Interconnect circuit with Schmitt trigger as a buffer using energy recovery logic	40.6pW
Interconnect circuit with CMOS inverter using FinFET technology as a buffer and energy recovery logic	15.37pW

The recommended interconnect circuit with CMOS inverter employing FinFET technology as a buffer using an energy recovery logic circuit shows amazing results when compared to other interconnect circuits that are currently in use as buffers. The graph in Fig. 4.13 indicates the way the novel approaches lead to a decrease in power consumption.

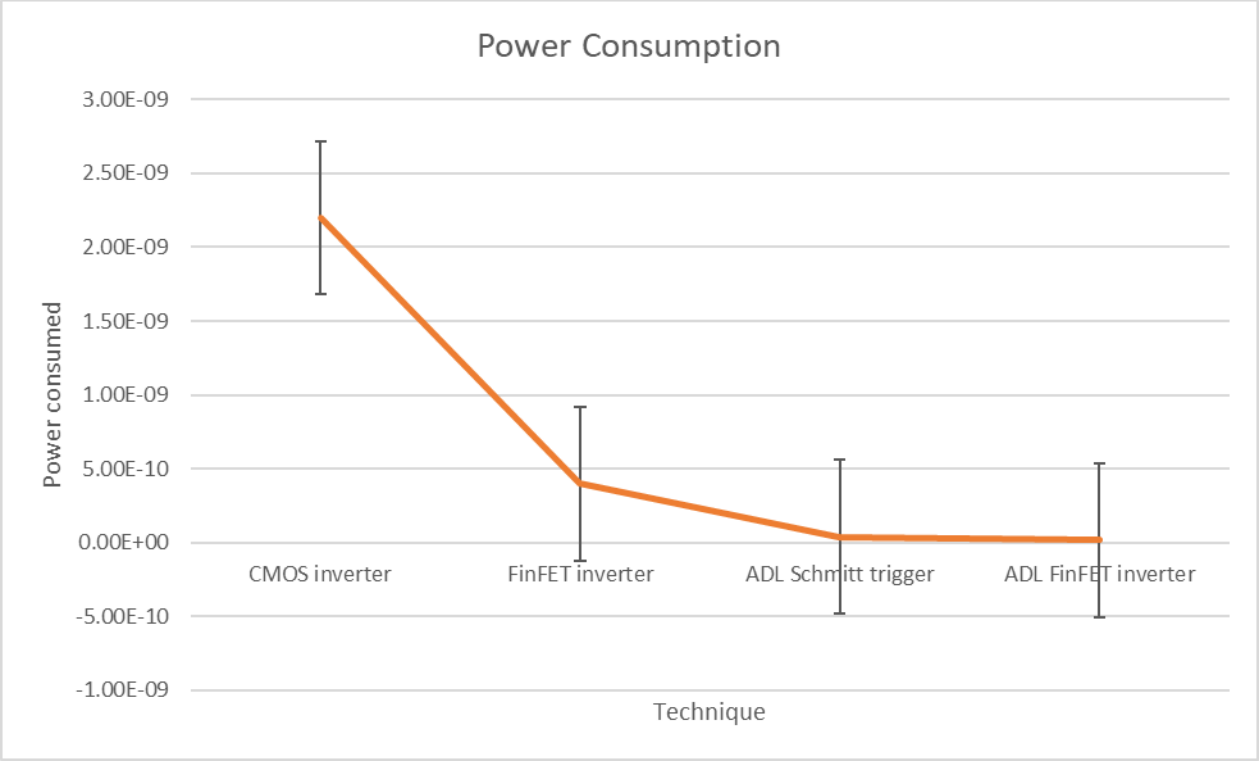


Fig. 4.13. Decrease in power consumption along with the technology used

Using FinFET technology and energy recovery logic, the CMOS inverter circuit produces outstanding results, as shown in Fig. 4.13. Furthermore, all of the main semiconductor companies currently use FinFETs as their production platform. But compared to the older planar devices, they are more challenging to manufacture and provide more complex

challenges (reliability, design, etc.). The FinFET platform is expected to be used in the construction of future devices.

The power consumption in interconnect circuits with and without buffer insertion (RC interconnect π-model) and varying connecting lengths is tabulated in Table 4.2. Table 4.3 provides an additional comparison with other innovative approaches.

Table 4.2. Comparison of power consumption of RC interconnect circuits with and without buffer insertion w.r.t interconnect length

Length (mm)	Power consumption of distributed RC interconnect (π-model) (µW)	Power consumption with ADL Schmitt trigger buffer insertion (pW)
1	0.113	17.4
2	0.113	13.9
3	0.114	14.9
4	0.115	15.9
5	0.115	16.9
6	0.115	17.8
7	0.115	13.8
8	0.115	11.7
9	0.116	9.93
10	0.117	8.40

As technology is scaled back and circuit efficiency is decreased, the issue of power consumption and dissipation in the form of heat in the circuits arises. Not all power consumption is desired, even when it is necessary to operate a circuit. With technology getting smaller, circuits must consume less power. It can be seen from Table 4.3 that after applying adiabatic switching to the buffer circuits, the power consumption is reduced considerably.

Table 4.3. Comparison of power consumption in RC interconnect circuits with state-of-art techniques for 10mm interconnect length

Technology (nm)	Supply voltage (V)	Power consumption (W)
45nm [37] CMOS	0.6	7.4µ
32nm [38] FinFET	0.225	0.116 µ
45nm (proposed interconnect buffered)	1	8.40p

It is clear from the comparison data that there has been a significant decrease in the circuits' overall power. The proposed interconnect structure shows 92.76% decrease in power consumption when compared with [38] and 99.89% decrease when compared with [37]. The suggested buffered connection circuit with energy recovery logic produces superior results even with a smaller technology node and FinFET technology [57], which is employed for low power consumption. The area appears to be longer since buffers have been built in between.

4.5 CONCLUSION

This chapter used an enhanced Elmore delay assessment model to show the RC interconnection structure with buffer insertion. The various buffer types were examined, as well as how they operate. In addition to latency, power consumption was also regarded as a primary concern, which was reduced by using an enhanced RC model. Buffers are incorporated using the adiabatic switching technique to reduce power consumption in the connecting circuits. It was observed that power consumption rapidly decreases with an increase in interconnection length following buffer insertion. The proposed interconnect structure showed 92.76% decrease in power consumption when compared with [38] and 99.89% decrease when compared with [37]. It was observed that the power utilisation of both kinds of RC interconnect networks followed a straight line. Even though there would be a slight increase in computation costs, the suggested structure with buffer insertion performs better in terms of reducing circuit power consumption. Furthermore, it is generally accepted that the buffer circuit serves to reduce the circuit's overall power consumption. Additionally, various buffer circuits can be implemented for future angles, which can reduce power consumption and delay. Correlations with copper material should be achievable, and other substances can also be used to evaluate the distinctive variables for the circuits.

Since, adding buffers in between long wires causes area constraints in the integrated circuits. It can increase the issues of delay, crosstalk, as well as heat generation as with the decrease in technology area components become closer to one another. Also, with technology reduction area automatically reduces with causes the issue of insertion of optimum numbers of buffers. To resolve these issues, different techniques can be studied like voltage swinging, optimised area and wire sizing, etc. one such technique will be studied in the following chapter which will target not only delay but power consumption as well.

CHAPTER 5

DESIGN AND IMPLEMENTATION OF RC GLOBAL INTERCONNECTS WITH CURRENT MODE SIGNALLING TECHNIQUE

CHAPTER 5: DESIGN AND IMPLEMENTATION OF RC GLOBAL INTERCONNECTS WITH CURRENT MODE SIGNALLING TECHNIQUE

This chapter examines the various signalling mechanisms and the problems that arise in long cables as a result of increased connection resistance and length. An overview of the current mode signalling approach for long wires is given in this chapter. A short introduction is provided in section 5.1. Various signalling techniques are covered in section 5.2. The proposed approach for interconnect designs is explained in Section 5.3. Results and debates are explained in Section 5.4, which is followed by the comparative and experimental evaluations. Finally, the chapter's conclusion is provided in section 5.5.

5.1 INTRODUCTION

Devices with the most features that are small, fast, and compact are necessary for modern technology. Over time, there has been a significant increase in the need for portable sizes, and engineers are facing more and more issues with the gadget. One such concern is the technical scalability of interconnections. Although numerous approaches to improve connection performance have already been put forth, achieving higher performance outcomes has proven challenging due to shrinking component sizes and spacing. Sometimes resolving these problems makes the design more complex. Although employing previously suggested techniques and tools could help drivers operating interconnects, doing so results in higher power usage. Even with less sophisticated technology, interconnects are acknowledged as the primary source of power consumption in SoC designs. Because many electronics systems are application-specific and battery-sensitive, it is essential to minimise energy usage in on-chip interconnects [96]. Since interconnects are more than just transmission connections to ensure signal integrity when signals are transmitted across the system, monitoring the system's power function becomes crucial [97]. Different system levels, such as the circuit, architecture, network, or system levels, can manage the power. Circuit noise modelling, buffer sizing, and voltage swing signalling are all included at the circuit level. Interface design and bus topology are included at the architecture level. At the network level, error detection, correction, and appropriate routing are executed; at the system level, adaptive voltage tuning and system-based power management are carried out. Each of these layers helps to build SoC communication systems that are dependable and energy-efficient.

This chapter's work is done at the circuit level, where the size of each buffer that needs to be placed has already been decided. Additionally, it was noted that after the buffer was inserted into lengthy cables, the delay increased but power consumption was reduced. But it was determined that adding buffers between lengthy wires increased the number of layers in an IC, which in turn increased the chip's overall area. And increase in area can affect the performance parameters of an interconnect circuit. This chapter will explore several signalling approaches to solve the area restrictions for an IC. We'll research and investigate voltage swing signalling and current mode signalling.

5.2 TYPES OF SIGNALLING

The primary bottleneck in high-performance VLSI systems is signalling under global strains since signal propagation delays are a common issue compared to circuit delays. For advanced mode signalling, therefore, precise and accurate delay estimate models are required [76]. There are two different kinds of signalling techniques: current mode signalling and voltage mode signalling. Many methods for simulating delay in voltage-mode interconnects have been devised, from distributed RLC versions to lumped RC models. The foundation of these methods is analytical closed-form formulations. Node voltages are used in voltage-mode signalling to describe networks, whereas branch currents are used in current-style signalling. Because current mode signalling keeps problems from arising from a fall in supply voltage and an increase in operation speed, researchers are currently particularly interested in it.

5.2.1 VOLTAGE MODE SIGNALLING

Low-power functionality is necessary for today's internet-connected gadgets. With so many gadgets connected to the online, the Internet has grown to be an indispensable aspect of modern life. The Internet of Things (IoT) is the name given to this technology. IoT is a collection of interconnected technologies rather than a single technology. Devices using this technology have transceivers, computers, actuators, and sensors incorporated in them [98]. Wires are used to connect all of these parts and facilitate signal transmission between devices. Although the IoT device's integrated components may be tailored to a particular application, the transmission lines that link them are the main source of worry. Typically, a voltage supply is applied to the connection to supply the circuit with an appropriate amount of current. To improve the circuit's efficiency, modifications to the voltage supply can be made, such as adjusting the power supply's voltage swing or switching activity. Sending low-voltage current signals to the network branches is an alternative option that could speed up the system and

use less energy. In any event, VLSI chips are where voltage mode signalling is most frequently used. When using voltage mode signalling, the receiver's input impedance termination is high ($R_L=\infty$). Information is transmitted using voltage. The output voltage, which depends on the input signal, is influenced by the supply voltage. The voltage value derived from the signal on the connection, which varies during a full voltage swing, is used by a sensing circuit at the destination. Fig. 5.1 [76] shows the theoretical model for the implementation of a conventional voltage mode connection. An open circuit terminates the output.

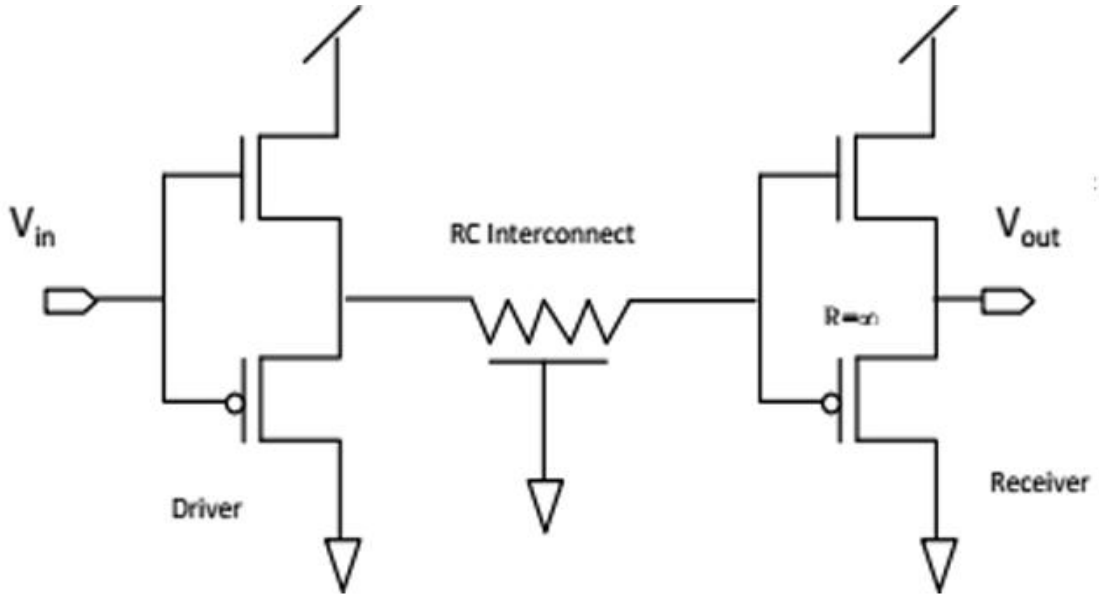


Fig. 5.1. CMOS depiction of voltage mode signalling [66]

The driver is made up of an inverter that powers a lengthy chain of RC interconnectors. The high input impedance of the receiver's inverter circuit ends this RC chain. The receiver's high input impedance causes a large input capacitance, which lengthens the RC connection chain's charging and discharging times. As a result, voltage mode signalling is very delayed. Electrostatically driven gate oxide breakdown may happen from the receiver's high input impedance, which prevents the charge buildup at the input from having an efficient discharge path to the ground.

It is easy to implement and examine the interconnect circuit using voltage mode signalling, however, the signalling itself has many drawbacks. Some of the issues can be low signal swing. The difference between the highest and lowest voltage levels in an electrical circuit or signal is referred to as a voltage swing. It shows the voltage values that the signal is capable

of reaching. While a smaller voltage swing could be more vulnerable to noise and interference, a larger voltage swing often provides higher noise protection and signal integrity. High switching noise injection is also one of the issues that can be sustained in a circuit with voltage mode signalling technique. Also, voltage fluctuations can also be seen and considered for creating delay issues in the circuits.

5.2.2 CURRENT MODE SIGNALLING

This type of signalling is considered better as compared to voltage mode signalling because of its various advantages over it since it can be more suitable for small portable devices. Since power is the primary concern, all current mode signalling schemes improve the performance of interconnect circuits that are appropriate for Internet of Things devices. It has emerged as one of the most intriguing advancements in the application of nanotechnology. The Internet of Nano-Things (IoNT), a brand-new IoT derivative, is expected to be created as a result, expanding the idea of the Internet of Things to its utmost potential through nanodevices [99]. Information is transmitted as a current signal in current mode signalling. At its input, the receiver has low impedance ($R_L = 0$). Shorting the wire ends the present mode signalling line. Fig. 5.2 [76] depicts the current mode signalling theoretical model.

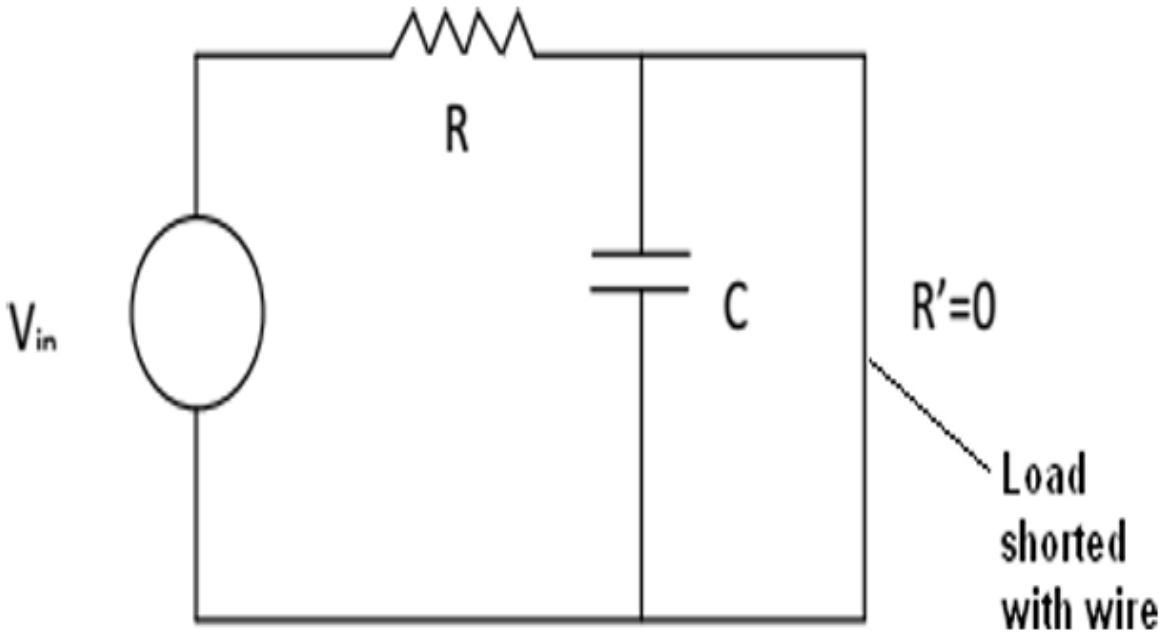


Fig. 5.2. Current mode signalling [76]

In Fig. 5.2, R' represent R_L in the circuit. The receiver provides low impedance and detects a current signal at its input. Fig. 5.3 [76] shows the CMOS representation of current mode signalling technique.

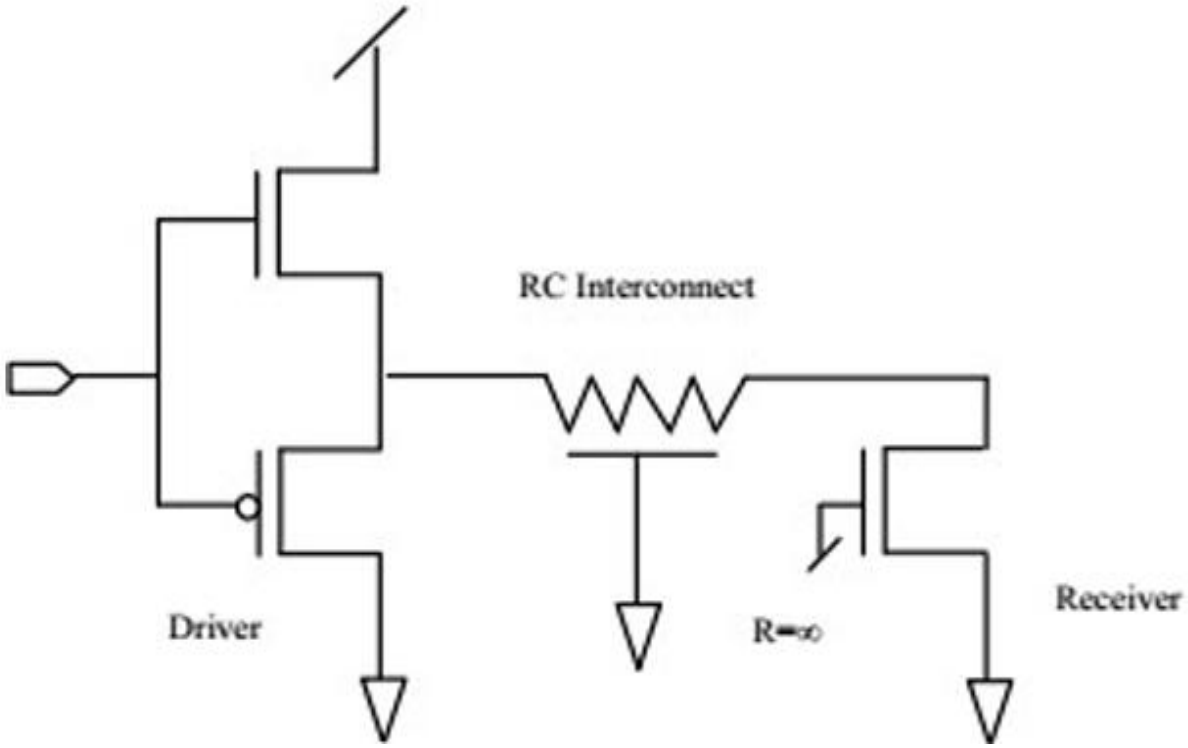


Fig. 5.3. CMOS representation of current mode signalling [76]

Considering that this technique depends on current to determine the logic values that are transmitted via a wire. The three primary factors for determining delay are termination impedance, driver output resistance, and voltage supply. By taking into account that the line will be terminated with a low impedance termination, power and time can be saved by preventing the charging of wire capacitance. However, this technique also consists of some advantages and disadvantages. By providing low voltage, small delay, signal integrity, low power, and low switching noise, the technique can be deemed to be advantageous for the circuits. However, the circuits' drawbacks could include the need for an additional receiver circuit and the potential for static power dissipation as a result of the low-impedance link to the ground.

5.3 PROPOSED METHODOLOGY

There are several kinds of interconnects, depending on what they are going to be used for. It could be a global interconnect that runs high up in the devices acting as a bus or clock, or it could be a local interconnect that connects two or more distinct transistors. The resistances and capacitances that make up an RC global interconnect determine the wire's overall performance. Since its geometry directly affects the system's performance parameters, it is also a problem when developing interconnects for nanotechnologies. Various techniques and algorithms can be developed to enhance the interconnect circuits' performance parameters, taking into account the geometry of the circuits as listed in Table 1.1 in Chapter 3. Chapter 3 already examines and provides a detailed description of one such technique. By using this strategy, the interconnect circuit's total resistance might be lowered by a factor of four while maintaining the circuit's capacitance. Without making the gadget any more complex, the resistance decrease enhanced the connection circuit's functionality. Both distributed networks and lumped networks model types underwent resistance reduction. In this chapter, using proposed H-model as mentioned in chapter 3 current mode signalling technique is applied to the interconnect circuits. Drivers are typically responsible for driving the interconnected lines. An interconnect line can be driven by a simple driver called a CMOS inverter for 45nm technology. A driver and a receiver are required in order to run the gearbox line in current mode. Low output impedance is a feature of one-bit current mode drivers. On the other hand, low capacitance and low impedance are provided by the current mode receiver side. Fig. 5.4 [97] shows the connecting circuit that uses the CMS approach.

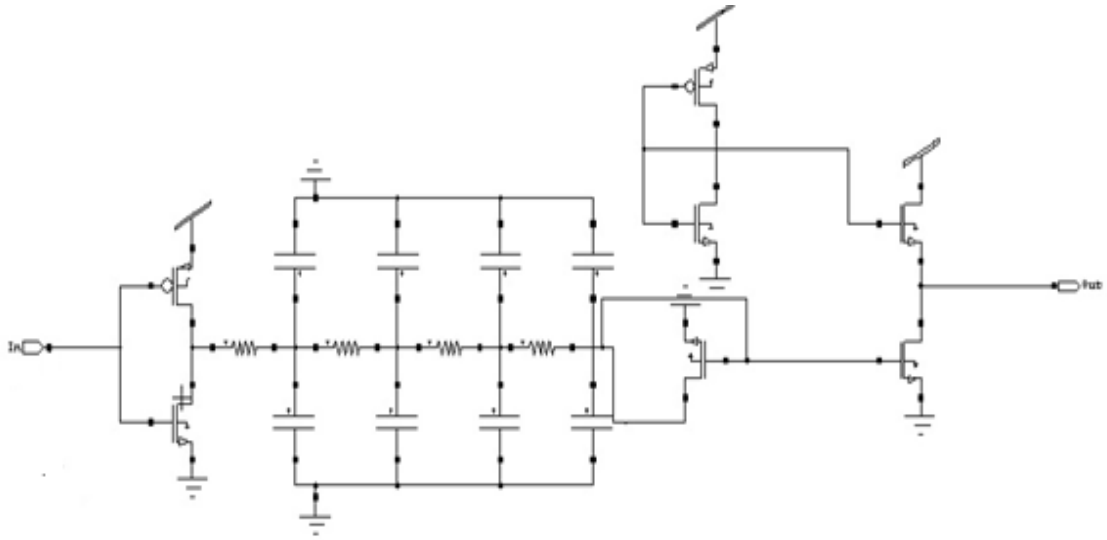


Fig. 5.4. Proposed interconnect circuit with CMS technique

The connecting line is powered by the basic inverter, which also serves as a current-mode driver. Using 45 nm CMOS technology, the aspect ratio of the receiver and current mode driver is W_p/W_n = 360/180. The dynamic power consumption, which is represented by Eq. (5.1) [100], is the power that is simulated.

$$P = \propto f C_L V_{dd}^2 \tag{5.1}$$

Where V_{dd} is the voltage delivered to transistors, C_L is the capacitive load including buffer and interconnect capacitance, f is the clock frequency and $\propto$ is the switching activity. The connecting circuit receives electricity from an inverter circuit for a delay. This inverter circuit is the current source for the connecting line. Thus, Eq. (5.2) [100] can be used to express the output current of the circuit:

$$i_o = A * i_i \tag{5.2}$$

Where A is the current attenuation and i_i is the input current. If $\frac{R_T}{4}$ and C_T stand for the wire's total resistance and capacitance, respectively, then Eq. (5.3) can be used to represent the output current delay roughly [100]:

$$\tau = \frac{R_T C_T}{8}\left[\frac{R_B + \frac{R_T}{12} + R_L\left(1 + \frac{8R_B}{R_T}\right)}{R_B + \frac{R_T}{4} + R_L}\right] \tag{5.3}$$

Where the load resistance is represented by R_L and the buffer resistance by R_B. The load for the source configuration is R_L= 0, which is the current mode type. As a result, the current mode delay can be expressed by Eq. (5.4) [100]:

$$\tau = \frac{R_T C_T}{8}\left[\frac{R_B + \frac{R_T}{12}}{R_B + \frac{R_T}{4}}\right] \tag{5.4}$$

$\frac{R_T}{4} >> R_B$ since global connection delay predominates over gate delay. Consequently, the connection circuit's overall latency when utilising the CMS approach can be expressed by Eq. (5.5) [100]:

$$\tau = \frac{R_T C_T}{24} \tag{5.5}$$

In theory, an interconnect circuit's delay can be determined by looking at the wire's total resistance and total capacitance without taking R_B into account. In reality, however, the total delay of the interconnect circuit is determined by the resistance of the wires, buffers, and capacitance. The delay for the wire with buffer resistance, and capacitance can be summarised using Eq. (5.6) [100].

$$\tau = R_B(C_T + C_B) + \frac{R_T}{4}\left(\frac{C_T}{2} + C_B\right) \tag{5.6}$$

In this case, R_T and C_T represent the wire resistance and capacitance, respectively, and R_B C_B represent the buffer resistance and capacitance.

5.4 RESULTS AND DISCUSSION

To find the ideal values for delay and power consumption, a simulation is performed using the proposed interconnection circuit and the current mode signalling (CMS) technique. The comparison of power usage and delay with and without the current mode signalling (CMS) technique is shown in Tables 5.1 and 5.2.

Table 5.1. Delay comparison for interconnect circuits for different lengths with CMS technique.

Interconnect length (mm)	Simulated delay π-model [28] (ps)	Theoretical delay for interconnect circuit with CMS technique (ps)	Simulated delay for interconnect circuit with CMS technique (ns)
1	2.82	0.21	0.04
2	10.75	0.87	0.35
3	23.68	1.97	0.65
4	42.14	3.51	0.91
5	65.91	5.49	1.16

6	94.87	7.90	1.38
7	129.15	10.76	1.60
8	168.70	14.06	1.81
9	213.55	17.79	2.01
10	263.72	21.97	2.21

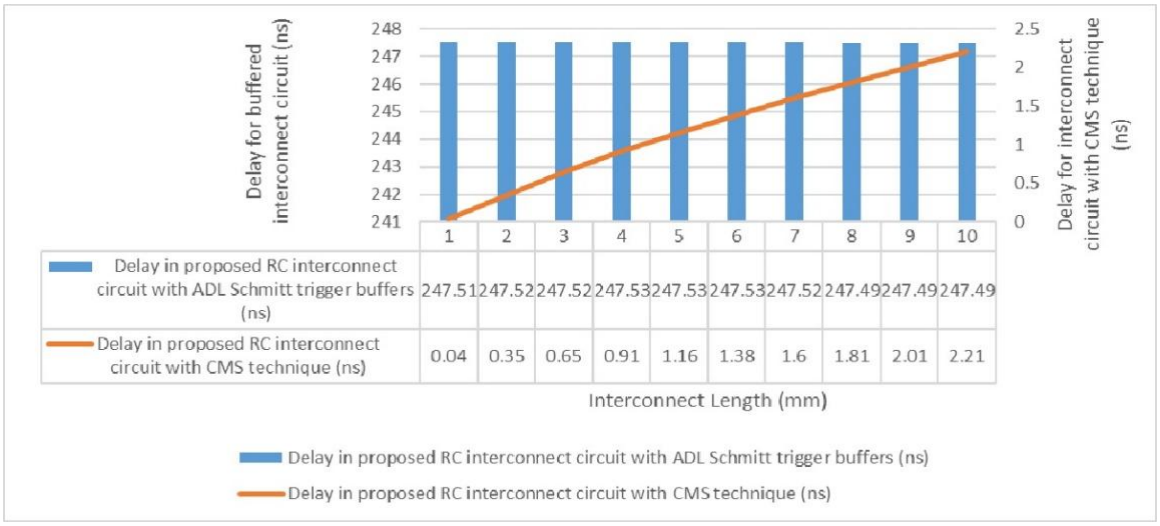
As demonstrated by Table 5.1, the π-model's delay is found to be superior to that of the interconnect circuit using the current mode signalling technique. This is a result of additional circuitry being added to the interconnect circuit to enhance the circuits' performance specifications.

Table 5.2. Power consumption comparison for interconnect circuits for different lengths with CMS technique.

Length (mm)	Power for interconnect circuit without CMS technique [24] (μW)	Power for interconnect circuit with CMS technique (nW)
1	11.3	18.7
2	11.3	20.8
3	11.4	23.6
4	11.5	26.5
5	11.5	29.4
6	11.5	32.3
7	11.5	35.1
8	11.5	37.9
9	11.6	40.7

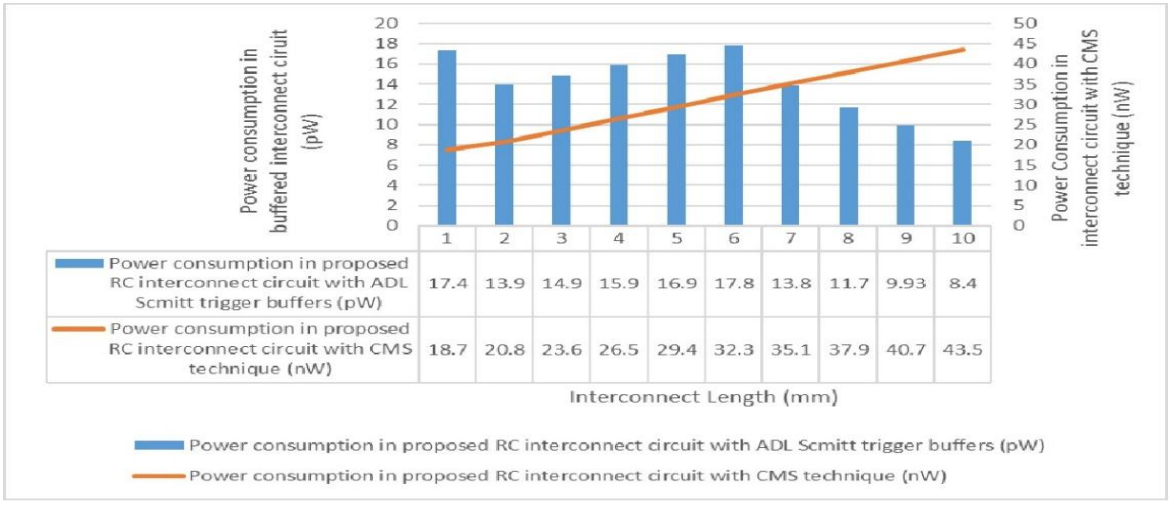
10	11.7	43.5

When compared to simple interconnect circuits, Table 5.2 shows that interconnect circuits that use the current mode signalling (CMS) technique consume less power. Using the current-mode technique makes it more energy-efficient even though basic interconnect circuits lower the parasitic component, which further reduces the power consumption in the circuits. Additionally, Fig. 5.5(a) and (b) show the comparison of power consumption and delay when compared to the interconnect circuits with buffer insertion approaches.



Interconnect Length (mm)	1	2	3	4	5	6	7	8	9	10
Delay in proposed RC interconnect circuit with ADL Schmitt trigger buffers (ns)	247.51	247.52	247.52	247.53	247.53	247.53	247.52	247.49	247.49	247.49
Delay in proposed RC interconnect circuit with CMS technique (ns)	0.04	0.35	0.65	0.91	1.16	1.38	1.6	1.81	2.01	2.21

(a)



Interconnect Length (mm)	1	2	3	4	5	6	7	8	9	10
Power consumption in proposed RC interconnect circuit with ADL Scmitt trigger buffers (pW)	17.4	13.9	14.9	15.9	16.9	17.8	13.8	11.7	9.93	8.4
Power consumption in proposed RC interconnect circuit with CMS technique (nW)	18.7	20.8	23.6	26.5	29.4	32.3	35.1	37.9	40.7	43.5

(b)

Fig. 5.5. The comparison results of the proposed interconnect circuit with Schmitt trigger buffer insertion technique using energy recovery logic and CMS technique (a) Delay (b) Power consumption

Lastly, the proposed interconnect structure with current mode signalling technique can be compared with the other state-of-art techniques and the results are tabulated in Table 5.3. It is observed that the proposed interconnect structure with CMS techniques shows better speed efficiency with 30.51% decrease in delay value when compared with [39] and 99.98% decrease in power consumption values when compared with [40].

Table 5.3. Comparison with other state-of-art techniques

Technology/Models	Delay (ns)	Power Consumption (W)
Proposed interconnect circuit with CMS technique (6mm, 1GHz)	1.38	32.3n
Interconnect circuit with CMS technique (6mm) [39]	1.986	-
Buffered interconnect circuit with CM technique (1GHz) [40]	-	0.15m

5.5 CONCLUSION

Small portable devices and IoT technology is being examined for various applications because to the rise in demand for smart gadgets. However, as technology advances, there is a growing demand for energy-efficient gadgets. Any nano device must have both high speed, low power consumption, and less area; all characteristics can be adjusted at the circuit level with a variety of instruments and methods. Reducing an interconnect line's resistance has been shown to significantly lower wire delays and power usage. Additionally, the resistance is dependent on whether the network is scattered or lumped in its structure. This chapter reviews a distributed interconnect topology with a wire parasitic component that uses a current-mode signalling mechanism with lower resistance. The interconnection power consumption has been increased, according to the simulation results. The comparison was done with interconnect circuits using buffers with adiabatic switching logic and interconnect circuits using current mode signalling technique. The simulation and theory's delay values differed noticeably from one another. The delay was lower than with state-of-the-art because the theoretical values only depended on the capacitance and resistance of the wire. When compared to the state-of-the-art, the simulated results with the additional buffer resistance and capacitance added showed a little higher delay, but still less. It is observed that the proposed interconnect structure with CMS techniques shows better speed efficiency with 30.51% decrease in delay

value when compared with [39] and 99.98% decrease in power consumption values when compared with [40].

This study aimed to reduce overall power consumption for Internet of Things applications by optimising power usage in the connectivity circuit. The SPICE program is used to calculate the power consumption for a range of connector lengths, from 1 mm to 10 mm. This chapter has demonstrated that as compared to circuits with lower resistance, interconnect circuits employing the CMS technique use a significant reduction in power consumption. The additional circuitry required to drive the connection lines is the interconnect design's drawback. This additional circuitry affects the device's latency and takes up space on the chip. If the buffers are not sized correctly, the delay will also get longer. Even a small amount of gate delay can increase the delay value for the entire interconnect design since the interconnect delay is bigger than the gate delay. The CMS approach, with its quick and energy-efficient processing, may be considered the future of VLSI interconnects, as technology and circuits are becoming rare every year. Despite enhancing all the performance parameters of the interconnects there still an issue persists. Inductance as a parasitic component starts to dominate in the circuit with the technology decrease. It introduces itself in the circuitry which becomes hard to neglect. That is why inductance as a parameter must be reduced for better performance and will be covered in more detail in the upcoming chapter.

CHAPTER 6

DESIGN AND IMPLEMENTATION OF RLC GLOBAL INTERCONNEC

CHAPTER 6: DESIGN AND IMPLEMENTATION OF RLC GLOBAL INTERCONNECTS

This chapter describes the VLSI interconnects as transmission lines and the problems which occurs in long wires due to the increase in interconnect length and resistance. In this chapter, an overview of the RLC interconnect circuits for long wires is provided. In section 6.1, basic introduction about RLC circuits is presented. In section 6.2, inductance as a parasitic component in long wires is discussed. Section 6.3 explains the proposed approach for RLC interconnect designs. Section 6.4 explains results and discussions followed by the experimental evaluations, and the comparison. Lastly, section 6.5 provides with the conclusion of the whole chapter.

6.1 INTRODUCTION

Although, today's technology is still working with RC interconnects but as the device size keeps on shrinking, inductance have started to play an important role. A difficult problem with inductance may arise when technology becomes smaller and the clock frequency rises. On the other hand, inductance is not always restricted to a certain area, which presents a challenge. When it comes to modelling, inductance is an electromagnetic phenomenon that can be more complicated than resistance or capacitance. If not for little pieces, it becomes nearly impossible to extract and analyse and is difficult to grasp [101]. The development of VLSI technology has led to the dominance of inductance in wire geometry. Consequently, interconnect latency and system performance have a major impact on the performance due to the transmission lines effect now [102]. Inductance results in overshoot and increased latency, which cannot be completely ignored. At gigahertz frequencies, long connecting wires function similarly to transmission lines [103]. Inductance as a parasitic may severely disrupt these chips performance at high operating frequencies. In the past, post-layout simulation was primarily concerned with resistance and capacitance parasitics, with inductance extraction restricted to custom inductor characterisation. That can't be true anymore as with the increase in interconnect length inductance as a parasitic component have started to become an important factor for a circuit's delay. In order to provide realistic post-layout simulations, inductance extraction for interconnect has become crucial due to the growing influence of inductance parasitics on modern designs. Hence, inductor becomes important to be included while modelling an interconnect circuit.

It is not optimal to have metal conductor interconnects separated by a dielectric. Material parasitics (resistance, capacitance, and inductance) will always create delays in signals passing across interconnects. Whereas capacitance parasitics are brought on by the electric field between two conductors, resistance parasitics are created by the resistance of electrons travelling through the metal. When current flows via a conductor, a magnetic field is produced, which leads to inductance parasitics. Any conductor that has current flowing through it produces a magnetic field. The same metal may then experience self-inductance from this magnetic field, or another metal may experience mutual inductance when it crosses the magnetic field [101]. Interconnect impedance can be expressed by Eq. (6.1) if we concentrate on resistance and inductance.

$$Z = R + j2\pi fL \tag{6.1}$$

Where impedance is represented by *Z*, resistance by *R* (measured in Ohms), operating frequency by *f*, and inductance by *L* (measured in Henrys). Resistance parasitics dominate connection impedance at low frequencies and direct current (DC). But as the frequency rises, inductive impedance takes centre stage and interferes with the transmission of the signal. Besides, increase in frequency give rise to skin effect in the interconnect parasitics. The current distribution is no longer uniform throughout the conductor cross-section as frequency rises. Between the outside surface and a depth known as the skin depth, the current has a tendency to flow closer to the conductor surface, or skin. This skin depth is determined by the conductor depth's electrical and magnetic characteristics as well as the current's frequency. At high frequencies, skin effects cause a conductor's resistance parasitics to grow [105]. They also result in a frequency-dependent value for the current's perceived resistance and effective inductance.

6.2 INDUCTANCE AS A PARASITIC COMPONENT

Certainly, the goal of parasitics extraction is to match physical silicon measurements as closely as feasible. Chip performance is impacted by inductance parasitics in several ways. Long wires (such as buses) can have a variety of impacts, including ringing (signal oscillation), overshooting (exceeding goal values), and delays. Impedance mismatch induces reflections in transmission lines, which is another effect [106]. Inductance parasitics can cause RF blocks to lose bandwidth and gain. Inductive parasitics can cause oscillation frequency drift in a voltage-controlled oscillator (VCO) architecture. It is crucial to run

inductance extraction during chip design and analysis to take these effects into account, particularly for high-frequency analogue and radio frequency circuits. The magnetic field produced by currents flowing through conductors causes inductance parasitics.

There are two primary obstacles to accurate inductance extraction [104]:

i. A phenomenon of loops is inductance. It is challenging to identify which current loops are important since inductance is a characteristic of current loops.
ii. The effect of inductance is long-lasting. Inductance is a long-range effect as opposed to capacitance extraction, where the conductors hide the electric field, hence limiting the couplings to the nearest neighbour. On nearby conductors, the magnetic field does not terminate.

Due to a rise in clock frequency and a fall in resistance, the inductive effect starts to take hold and affects global buses and clock routing. Deep submicron technology requires a modification of the interconnect model from the inadequate RC model to the RLC model, where L denotes inductance [107]. It becomes crucial to identify the near loop or return path in the circuit as inductance is by definition defined for loops rather than wires. Inductance extraction becomes challenging or unfeasible for the EDA tools [107]. There is a lot of resistance in small electronics, such as gate resistance and wire resistance. The majority of signals in the interconnect model are often dominated by RC delay when the gate ON resistance is on the order of a kilo-ohm, which is typically $R > > jwL$. However, the minuscule enough ON resistance of the huge driver allows the inductance to control the system's dynamic response. Generally speaking, the mutual inductance term is more noticeable and noisier in buses, whereas the self-inductance term is more prominent in clocks. Power supply rail inductance causes power loss in addition to IR drop [108]. Due to its ability to impose limitations on interconnect circuits, inductance behaviour is more noticeable over extended distances than capacitive behaviour. Global buses and clocks are frequently utilised as top-layer interconnects for data/information dissemination throughout the semiconductor. Because inductance behaviour is more noticeable in lengthy connecting cables, the top layers are thicker [74].

To study inductance from an electromagnetic point of view, consider a flux linearly related to the current as expressed by Eq. (6.2) [16]. An electromagnetic field is created around a conductor carrying current, and this flux stores energy.

$$\phi = L * i \tag{6.2}$$

Where ϕ is the flux, L is the proportionality constant known as inductance which is measured in Henrys (H), and i is the current associated with it. A voltage drop is caused by the magnetic flux acting on the wire itself when the current varies. To get at Eq. (6.3) for a linear inductor, a time derivative for Eq. (6.2) is considered and is represented by:

$$\Delta V = L * \frac{di}{dt} \tag{6.3}$$

For a DC, Eq. (6.3) suggests that there is zero voltage drop. This implies that for low-frequency operation, the inductor can be thought of as a short circuit. The voltage drop connected to the inductor in a chip increase as the current flowing through it does. Eq. (6.3) also illustrates how quickly the rate of change of current concerning time increases for a high-speed design. Thus, in the power distribution system and at the package pins, inductance effects are very significant [16].

6.3 PROPOSED METHODOLOGY

The on-chip interconnect's length grows as technology gets smaller. The resistance, capacitance, and inductance all rise in proportion to this increase in the connection length. Fig. 6.1 represents basic RLC circuit.

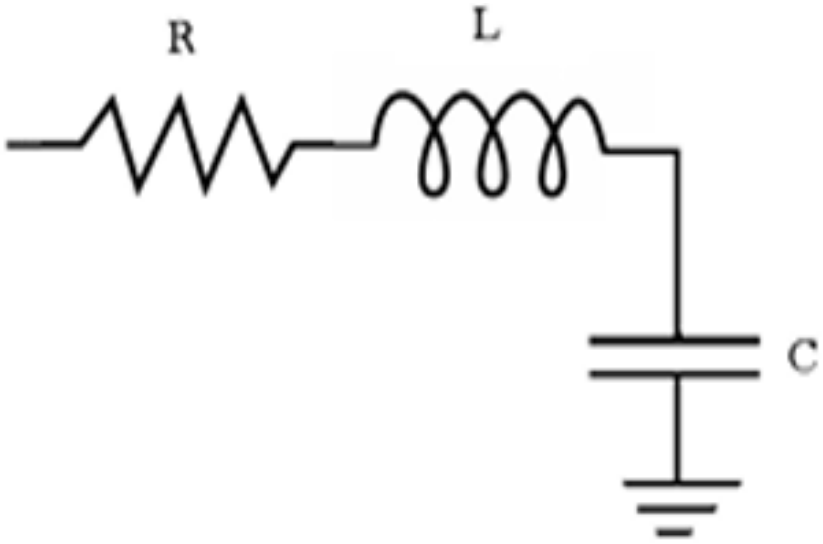


Fig. 6.1. Basic RLC circuit [106]

The inductance characteristic is only noticeable at higher frequencies. Frequency rises with decreasing connecting circuit area. Even basic wires within circuits begin to resemble transmission lines at higher frequencies. Because inductance is a function of circuit area, a smaller circuit will have a lower inductance. Additionally, the circuit's inductance directly affects impedance. As a result, when inductance decreases, so does impedance. As inductance decreases at high frequencies, the current's return route gets closer. As studied in chapter 3, the reduction in resistance value was seen with a change in interconnect structure (H-model). It was observed that the resistance has decreased by a factor of 4, substantially lowering the interconnect circuits' performance metrics. The resistance and capacitance of the structure in question are split into two sections, each having a half value that matches. It is simple to model and has an almost elementary structure. The resistance and capacitance values are divided when the circuits are connected in an inverted way, coupling one to the other. In this article, as the circuit's frequency is raised, inductance is also seen as a parasitic component alongside resistance and capacitance. When all of the parasitic elements are combined in an inverted orientation, resistance and inductance are decreased by a factor of 4. When the two circuits are connected, the resistance and inductance of the proposed structure is reduced by a factor of four. As technology becomes smaller, inductance becomes more important. As inductance increases, delay increases [98]. In the proposed layout, the inductance becomes parallel to each other when two circuits are connected in parallel. The inductance value is split between the two circuits when a single circuit is split into two. Moreover, the performance characteristics are improved when the inductance decreases. The total inductance of the proposed structure can be computed using Eq. (6.4).

$$\frac{1}{L} = \frac{1}{L_1} + \frac{1}{L_2} \tag{6.4}$$

To calculate the delay for the proposed RLC interconnect circuit consider Fig. 6.1 [98].

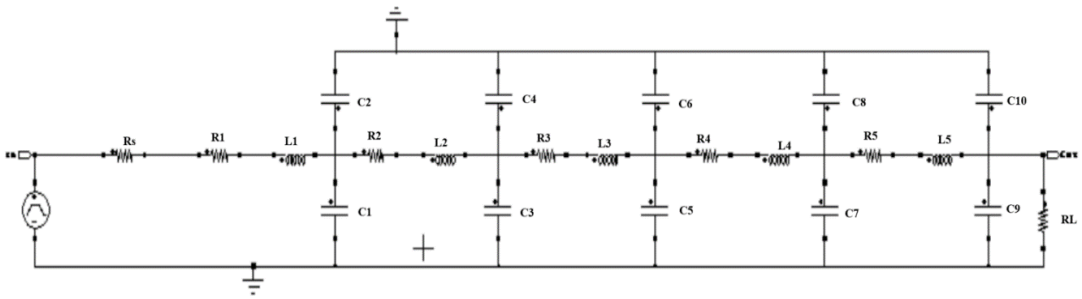


Fig. 6.2. Proposed RLC interconnect circuit [107]

The resistance and inductance of the suggested structure are lowered by a factor of four when the two circuits are joined. In the suggested arrangement, the inductance likewise becomes parallel when two circuits are connected in parallel. The inductance value was split across the two circuits that results from splitting the single circuit into two. Additionally, the performance parameters are optimised when the inductance decreases. To explain the entire transient model for each interconnect circuit, four normalised ratios (base variables) are required as expressed by Eq. (6.5), (6.6), (6.7), and (6.8), defined by [101, 109]:

$$R_{ratio} = \frac{line\ resistance}{characteristic\ impedance} = \frac{R}{Z_o} \tag{6.5}$$

$$C_{ratio} = \frac{load\ capacitance}{line\ capacitance} = \frac{C_L}{C} \tag{6.6}$$

$$T_{ratio} = \frac{time}{ToF} = \frac{t}{t_f} \tag{6.7}$$

$$R_T = \frac{source\ resistance}{characteristic\ impedance} = \frac{R_s}{Z_o} \tag{6.8}$$

Where R is the total wire resistance, R_S is the source resistance, Z_o is the wire impedance, C_L is the load capacitance, C is the total wire capacitance, and ToF (t_f) is the time of flight which can be expressed by Eq. (6.9):

$$t_f = L\sqrt{lc} \tag{6.9}$$

The amount of time it takes a signal going through a medium at the speed of light to travel a distance equal to the line's length is known as the time of flight. Similar basis variables may exist for interconnects with completely different line parameters, such as length, driver size, capacitance, load and resistance, and inductance per unit length. They will therefore likewise be same when their transient properties are represented by the normalised ratios. In this work, these dimensionless ratios are used to characterise connection properties such as time delay. The finite line is driven by a source driver that is always connected to the connection circuit and supplies some voltage. Eq. (6.10) was used to approximate the voltage at the end of a finite line with a capacitive termination.

$$V_{fin}(L,t) = V_{dd}\frac{2Z_o}{Z_o + R_s}e^{-\frac{rt}{2l}}\left[1 - e^{-\left(\frac{1}{C_L Z_o}\right)(t_d - t_f)}\right]\mu_o(t_d - t_f) \tag{6.10}$$

where characteristic impedance, source resistance, load capacitance, line resistance per unit length, inductance per unit length, time delay, and time of flight of the line are represented, respectively, by Z_o, R_s, CL, r, l, t_d, and t_f. To get the 50% delay for a transmission line with resistance and inductance that have been lowered by a factor of four, Eq. (6.11) can be used and is expressed as:

$$V_{fin}(L,t) = \frac{V_{dd}}{2} \tag{6.11}$$

$$V_{dd}\frac{2Z_o}{Z_o + R_s}e^{-\frac{rt}{2l}}\left[1 - e^{-\left(\frac{1}{C_L Z_o}\right)(t_d - t_f)}\right]\mu_o(t_d - t_f) = \frac{1}{2} \tag{6.12}$$

For a lossless transmission line, resistance becomes 0. So, for lossless transmission line the 50%-delay can be expressed by Eq. (6.13).

$$V_{dd}\frac{2Z_o}{Z_o + R_s}\left[1 - e^{-\left(\frac{1}{C_L Z_o}\right)(t_d - t_f)}\right]\mu_o(t_d - t_f) = \frac{1}{2} \tag{6.13}$$

$$t_d = t_f + C_L(0.45R_s + 0.25Z_o) \tag{6.14}$$

Expressing the time delay for a lossy RLC line of length L is possible using Eq. (6.15).

$$t_d = t_f + C_L\left(\frac{yrL}{4} + 0.45R_s + 0.25Z_o\right) \tag{6.15}$$

Consider the resistance-capacitance delay model Sakurai model, which was presented in [61], for estimating the value of y. Eq. (6.16) expresses the delay.

$$t_d = 0.377\left(\frac{r}{4}CL^2\right) + 0.693\left(R_s CL + C_L\frac{r}{4}L + R_s C_L\right) \tag{6.16}$$

The distributed RLC line offers the same time delay as the RC line concept for highly resistive lines with high resistance values. Presuming $\frac{r}{4}L \gg Z_o$, $C_L \gg CL$, and $\frac{r}{4}L \gg R_s$, the value of *y* can be evaluated by Eq. (6.17), (6.18) [98]:

$$t_d = 0.693\left(C_L\frac{r}{4}L\right) \tag{6.17}$$

$$y = 0.693 \tag{6.18}$$

An approximate model for the time delay of a distributed RLC line with load capacitance is obtained by substituting this value in Eq. (6.15) and simplifying the equation, as shown by Eq. (6.19).

$$t_d = t_f + 0.693C_L\left(\frac{r}{4}L + 0.65R_s + 0.36Z_o\right) \tag{6.19}$$

Neglecting source resistance, the lossless transmission line time delay can be expressed by Eq. (6.20).

$$t_d = t_f + 0.693C_L\left(\frac{r}{4}L + 0.36Z_o\right) \tag{6.20}$$

According to Eq. (6.20), if resistance predominates, the real-time delay for a line is equal to the RC delay; if inductance predominates, it is equal to the RLC delay [74]. Consequently, each capacitor is coupled to a distributed inductance. The phrases resistive and inductive dominate the line, and the terms RC and RLC just imply that since the response depends on the resistance and characteristic impedance values. The RC effect will be predominant if $R_T/4 >> Z_o$. On the other hand, an oscillating response will be seen if $R_T/4 << Z_o$ due to the inductive effects.

6.4 RESULTS AND DISCUSSIONS

Considering uniform distribution, Table I as mentioned in chapter 3 is considered as the wire geometry for 45nm technology. Table 6.1 tabulates the parasitic component values for interconnect circuit for different lengths ranging from 1mm to 10mm and Table 6.2 tabulates individual values of parasitic components [101].

Table 6.1. Different parasitic component values for different lengths of interconnect [98]

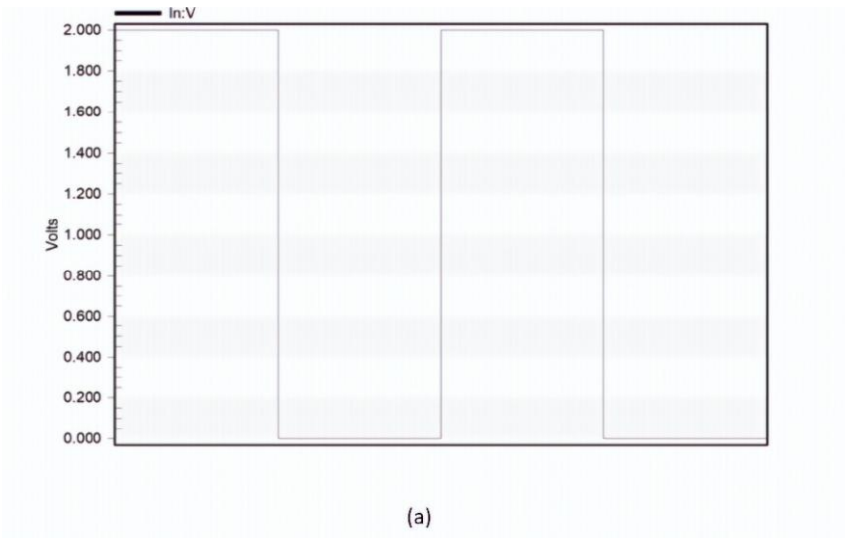
Length (mm)	Parameters		
	Resistance (Ω)	Capacitance (fF)	Inductance (nH)
1	110	191	1.58
2	220	383	3.44

3	330	575	5.41
4	440	767	7.44
5	550	959	9.52
6	660	1150	11.65
7	770	1342	13.81
8	880	1534	15.99
9	990	1726	18.20
10	1100	1918	20.44

Table 6.2. Individual parasitic component values for different lengths of interconnect [98]

Lengths (mm)	Individual Resistance (Ω)	Individual Capacitance (fF)	Individual Inductance (nH)
1	27.5	95.5	0.39
2	27.5	95.75	0.43
3	27.5	95.83	0.45
4	27.5	95.875	0.46
5	27.5	95.9	0.47
6	27.5	95.83	0.48
7	27.5	95.85	0.49
8	27.5	95.875	0.49
9	27.5	95.88	0.50
10	27.5	95.9	0.51

The inductive effects can be implemented and simulated using Table 6.2 and the effects can be seen in the form of waveform as shown in Fig. 6.2(a), (b), and (c).



(a)

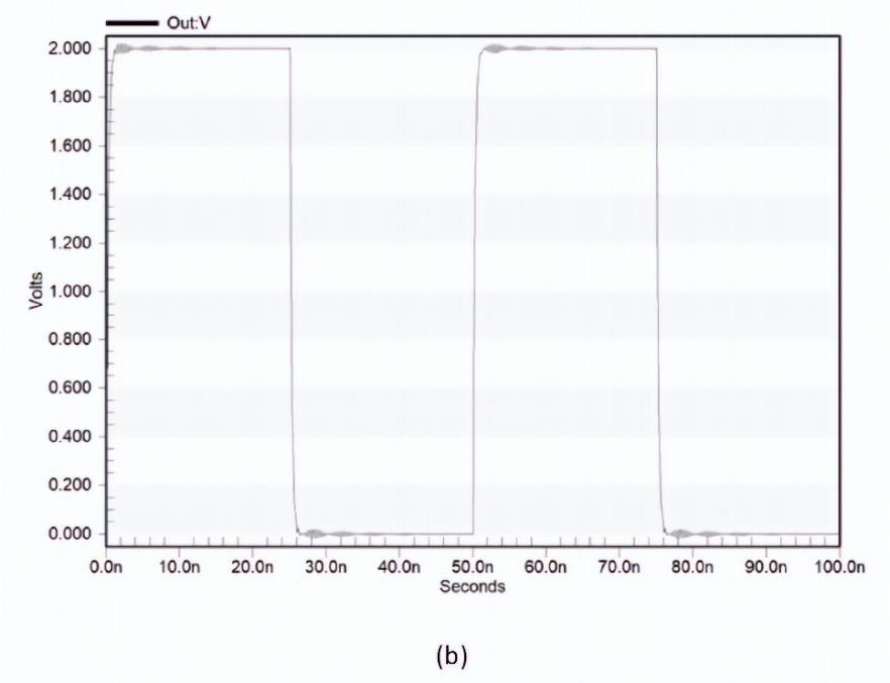


Fig. 6.3. Inductance effects (a) input signal (b) Interconnect length 2mm (c) Interconnect length 10mm

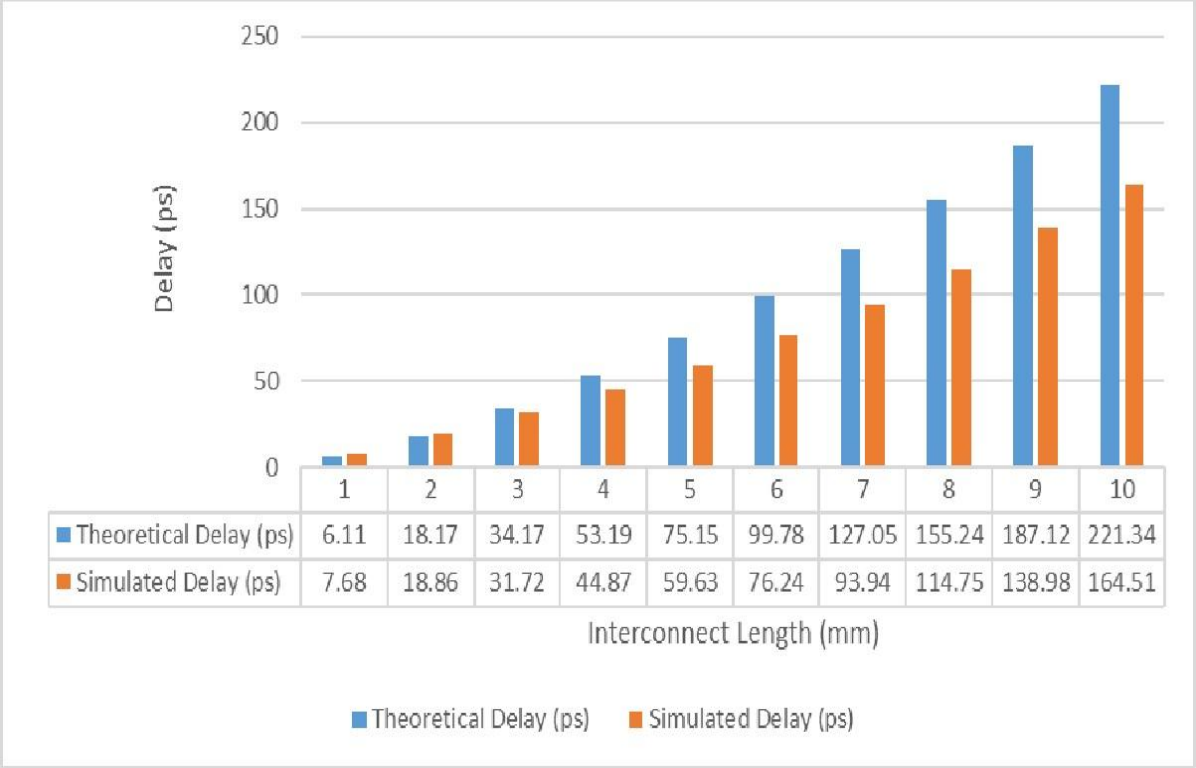
The performance parameters for the proposed distributed structures, which consider uniform distribution or the distribution of segments per unit length, are estimated using the values of resistance, capacitance, and inductance for each segment, which are displayed in Table 6.2 for a range of lengths. Total values of capacitance and resistance are derived using Predictive Technology Models (PTM) [23]. The waveform for the wired network with long (10 mm) and small (2 mm) wire lengths for the pulse input supply is shown in Fig. 6.2. Furthermore, estimated and tabulated performance values spanning from 1 mm to 10 mm, respectively, are

shown in Table 6.3. When modelling the structures, values calculated from Tables 6.1 and 6.2 are taken into consideration. When a pulse input is applied to the interconnected circuit, the RLC waveform is shown in Fig. 6.2. The waveforms demonstrate that the signal overshoots at each peak and that the signal strength declines. This overshoot in the output signal indicates that the circuit's delay increases when the transient value surpasses its ultimate value. It also implies the presence of inductive effects in the circuit. In comparison to circuits with longer wire lengths, the inductive effects are greater for circuits with shorter wire lengths. This is because smaller-length wires become extremely resistive whereas global-length lines become very resistive, overpowering the inductive effects in them.

Table 6.3. Performance evaluation for proposed RLC interconnect structure for Pulse input [70]

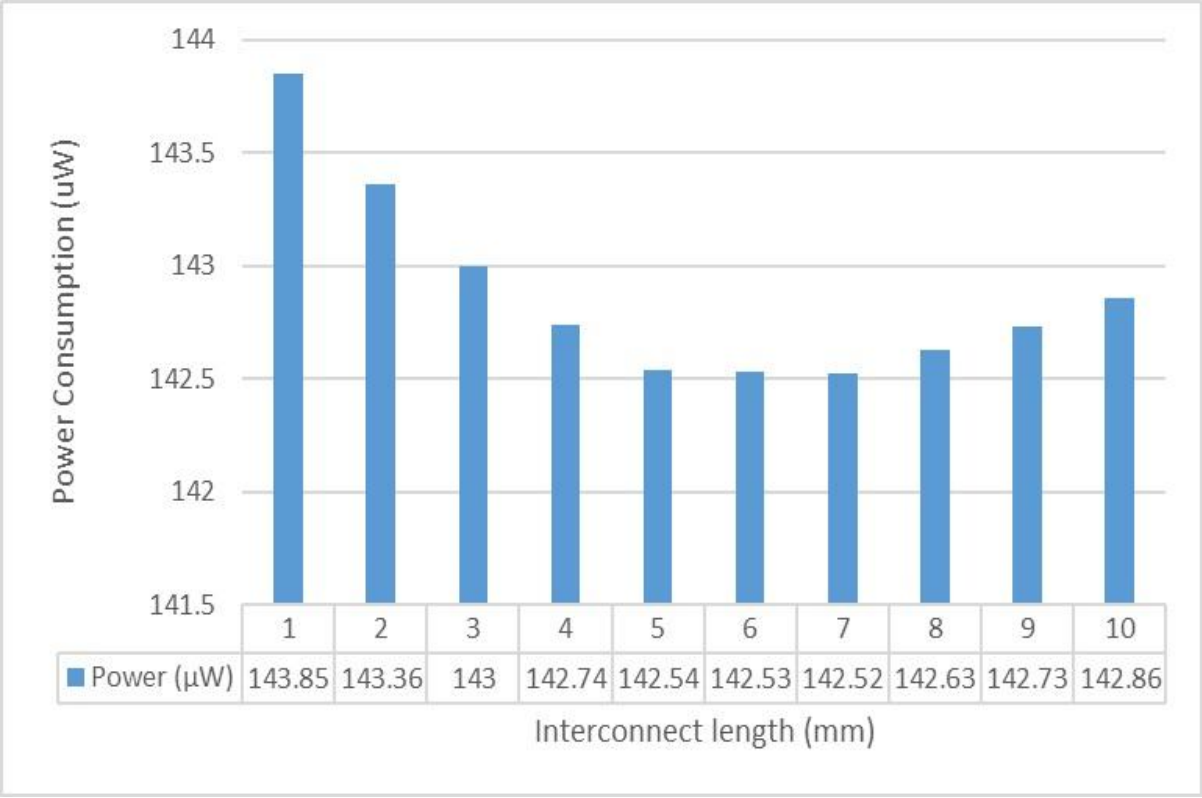
Length (mm)	Theoretical Delay (ps)	Simulated Delay (ps)	Power (µW)
1	6.11	7.68	143.85
2	18.17	18.86	143.36
3	34.17	31.72	143
4	53.19	44.87	142.74
5	75.15	59.63	142.54
6	99.78	76.24	142.53
7	127.05	93.94	142.52
8	155.24	114.75	142.63
9	187.12	138.98	142.73
10	221.34	164.51	142.86

Table 6.3 lists the power consumption as well as the theoretical and simulated delays for the RLC circuit at different lengths. It is clear that power consumption decreases and delay rises with wire length. Figs. 6.3(a) and (b) provide a graphical representation of Table 6.3 as well.



	1	2	3	4	5	6	7	8	9	10
Theoretical Delay (ps)	6.11	18.17	34.17	53.19	75.15	99.78	127.05	155.24	187.12	221.34
Simulated Delay (ps)	7.68	18.86	31.72	44.87	59.63	76.24	93.94	114.75	138.98	164.51

(a)



	1	2	3	4	5	6	7	8	9	10
Power (µW)	143.85	143.36	143	142.74	142.54	142.53	142.52	142.63	142.73	142.86

(b)

Fig. 6.4. The results for RLC interconnect circuits (a) Delay (b) Power consumption

The performance parameters for the proposed interconnect structure can be compared with the other state-of-art techniques and is tabulated in Table 6.4. The proposed interconnect circuit shows better efficiency and speed with 41.63% decrease on average when compared with [74].

Table 6.4. Comparison with other state-of-art technique.

Length (mm)	Proposed Delay (ps)	Delay (ps) [74]
2	18.86	29
4	44.87	74
6	-	-
8	114.75	213
10	164.51	305

The suggested circuits exhibit improved timing performance even when current mode signalling is used for the circuit in the research [71], which expands the bandwidth of the on-chip interconnects. This is due to the interconnect circuit's minor reorganisation.

6.5 CONCLUSION

An inventive RLC connection structure was simulated in this study. With delay calculations, the lossless RLC equivalent RC interconnect circuit was also built. It was shown that both resistance and inductance values are significantly declining, which eventually improves the interconnect circuits' overall performance. Every parasitic component's total and individual values were assessed with a uniform distribution in mind. Furthermore, it was found that the RLC network's pulse input signal delay increases linearly and noticeably with increasing connection length, while power consumption remaining almost constant. On the other hand, the RLC waveform with regard to time showed overshoots, which indicate whether inductive effects are present in the interconnect circuits. The recommended arrangement works better in terms of reducing circuit power consumption, despite a modest increase in processing expenses. Also, the proposed RLC interconnect structure shows 41.6% decrease in the performance parameters as compared to the state-of-art technique. Furthermore, in the future, the performance metrics of the circuits can be evaluated by comparing different materials to copper material. Additionally, by further dividing the length of each segment and adding buffers to the long wires, inductance effects can be minimised.

CHAPTER 7
CONCLUSION AND FUTURE WORK

CHAPTER 7: CONCLUSION AND FUTURE WORK

The latency of modern designs is mostly determined by interconnects, which are required to quickly and reliably generate estimates of interconnect delay at various levels of abstraction. Many connectivity strategies are utilised to improve performance in terms of noise reduction, power reduction, and speed. Technological advances have made size and speed an increasingly important feature of VLSI interconnects. Tens of nanometres is the maximum channel length for the device when technology descends to the deep submicron level. VLSI chips therefore need long interconnects. Considered the essential building component, interconnects are available in several sizes. They serve as a link between two or more blocks, hence while developing an IC, scalability issues must be taken into consideration. Interconnect became ever more important in VLSI circuits as scale increased. It regulates every significant electrical feature on the chip. Interconnects can now vary in size and speed thanks to downsizing technology, which has an instant impact on circuit characteristics. The connection circuit resistance is one such metric. Resistance increases when the connection geometry decreases. To minimise this resistance and enhance the connection circuit's performance, a novel interconnect structure with an enhanced Elmore delay estimation model was modelled. Additionally, lumped and distributed distribution segments for varying connection lengths have been shown to exhibit Elmore delay estimates for long wires with pulse and ramp inputs. The findings indicate that in RC networks with lumped pulse input signals, both power and delay rise linearly and significantly with increasing connection length. Conversely, in dispersed RC networks, power increases marginally while delay grows with increasing interconnect length. For both lumped and distributed networks, the ramp input delay is nearly the same as the pulse input supply. However, for lumped circuits, the power consumption increases linearly with the length of the interconnect; for distributed circuits, the power increases initially and then decrease with the length of the interconnect. As a result, the distributed network's performance metrics demonstrate greater efficiency as compared to the lumped network. A computation of optimised Elmore delay was carried out to lower the connection circuits' time constant. In addition to latency, power consumption was found to be optimal when utilising an improved RC model. However, reducing resistance may reduce some of the delay but as the wire length progresses the delay also increases. It is well known that the delay of lengthy wires varies quadratically with their length. Buffers are installed in between the lengthy cables to lessen the delay. Schmitt trigger inverter circuits and CMOS inverter circuits with FinFET technology are utilised as energy recovery logic

(ADL) buffers. These are used to simulate and implement the global interconnect circuits, and then they are compared for improved overall performance. After comparing, it is found that the connection circuit with the FinFET-equipped CMOS inverter and ADL logic produces superior power consumption results. Yet delay is observed to be increased due to an extra circuitry added to the circuit. To optimise overall performance of the circuit current mode signalling technique is used. In this technique, interconnect circuits are required with a driver circuit and a receiver circuit. After simulation, the results were observed and the delay calculations were done by reducing the resistance of the circuit. However, with the technology scale down, inductance effects start of dominate the interconnect wires. To reduce these effects inductance as a parasitic component is considered and reduced by the factor of four by introducing it into the proposed interconnect design. Further, for delay expression it was concluded that the nature of the transmission line will depend upon the resistance and impedance of the long wire. This means that if the wire's total resistance is greater than its impedance, the wire's RC delay will predominate; otherwise, the RLC delay will. Additionally, when comparing the two ladders—the RC ladder and the RLC ladder—power consumption in the RLC circuit is improved by 99.78% when compared to the π-RC lumped interconnect circuit, whereas power consumption in the π-RC distributed interconnect circuit is raised by 87.5%. RLC interconnected over RC lumped and distributed circuits showed delay improvements of 78.39% and 17.26%, respectively.

On achieving all the objective of this research work, finally the overall methodology of power-efficient VLSI interconnects with both the types of networks for L and π- model, Buffer Insertion with Energy Recovery logic, Current Mode Signalling Technique and RLC interconnect structure with reduced inductance value was shown in Fig 7.1. This research methodology works upon the performance parameters in terms of timing constant and power consumption as well as power dissipation of the VLSI interconnect circuits from length 1mm to 10mm.

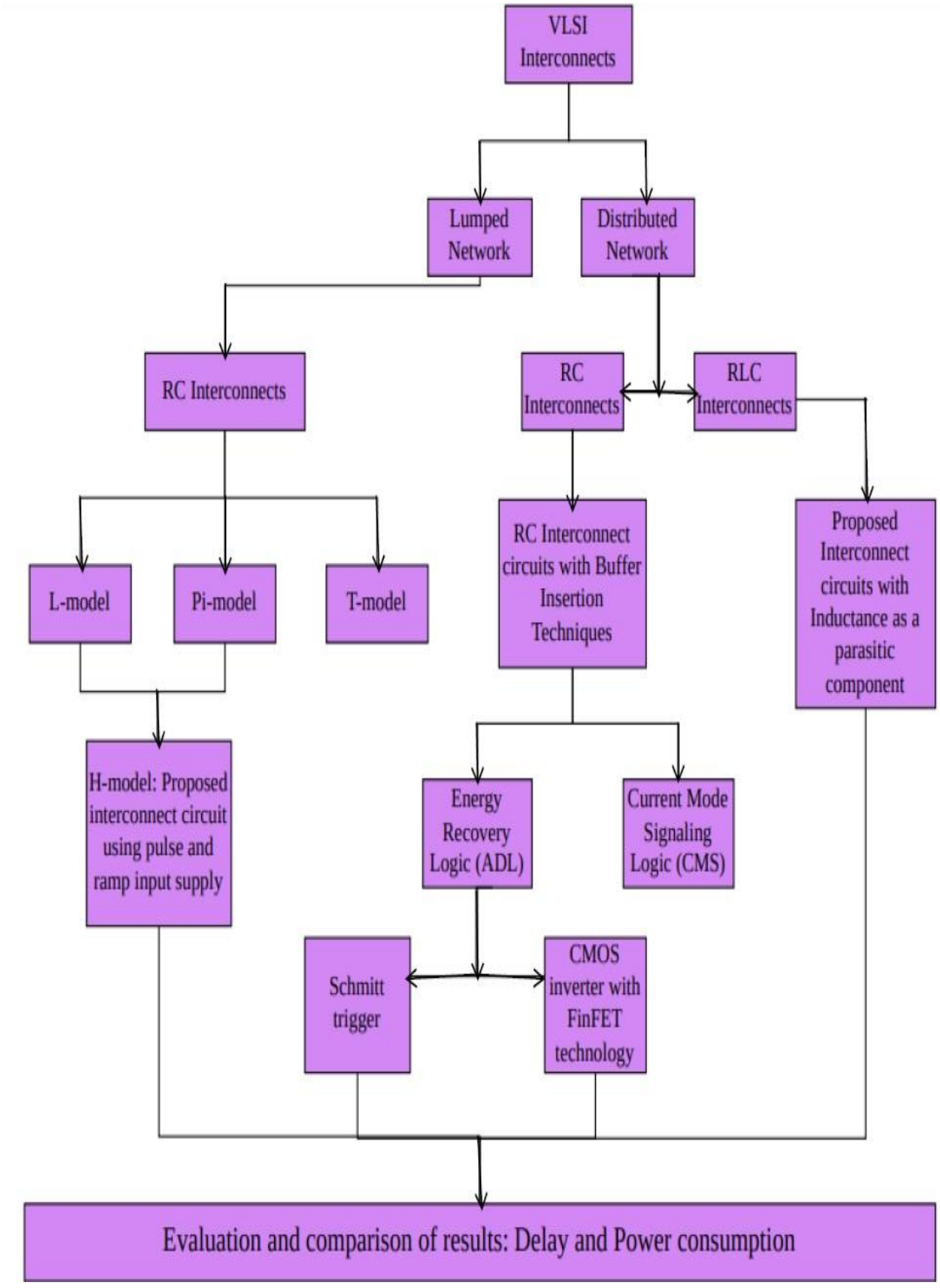
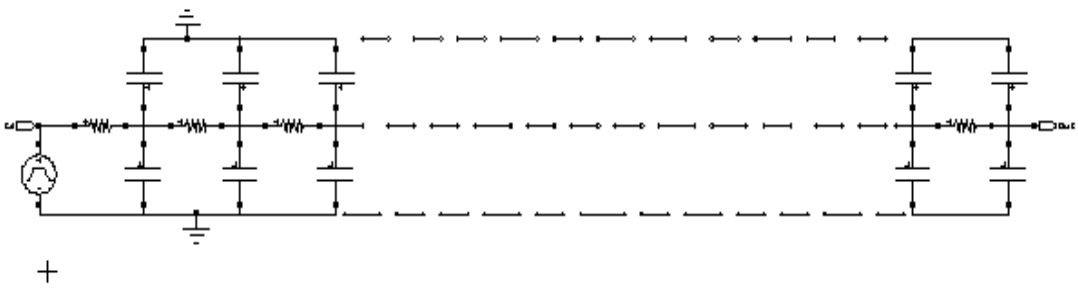


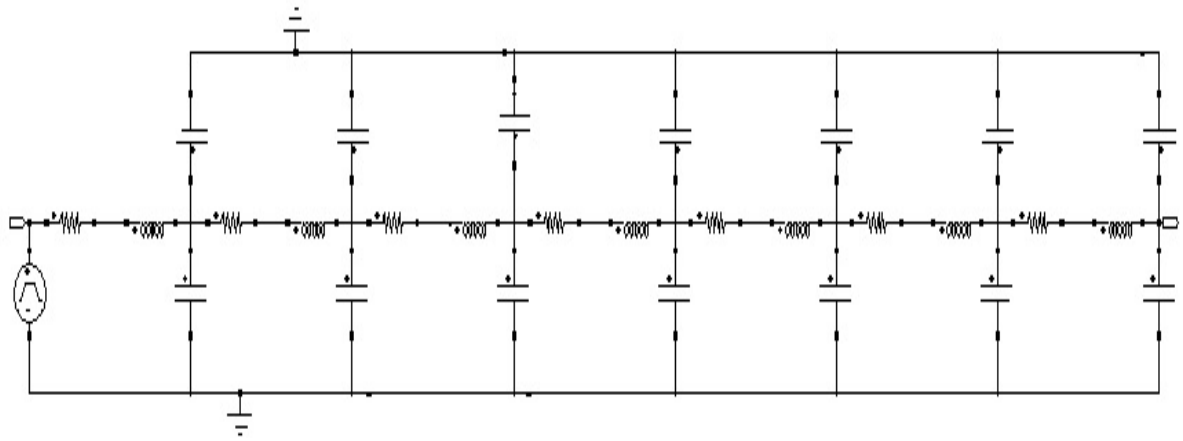
Fig. 7.1. Overview of the Methodology for Design of VLSI Interconnects for Power Optimisation

7.1 APPLICATION

The interconnect design for high frequency circuits and low resistance components is required to drive a device for proper functioning. Since, interconnect delay is dominating the gate delay in today's technology. It becomes a compulsion to look for low power devices with high throughput. Different applications require the concept of low-power interconnect design topologies be it healthcare, agriculture, house monitoring systems, etc. In [111], to facilitate the simultaneous monitoring of bio-potential signals (EEG/ECG), authors have introduced an active electrode design for electrical impedance tomography spectroscopy (EITS) that includes both current stimulation and sensing channels. The suggested design offers a wide bandwidth (20 MHz) at a low power consumption of 8 mW when operated at 5 V. In the proposed design as mentioned in [111], the input supply wires are decoupled against noise meaning the wires are set at such a way to minimize the noise injection in the device placed closed to a capacitor. In paper [112], author gives a thorough analysis of the solutions and trends that are now being offered in the context of smart mobility and supporting enabling technologies. By describing its primary characteristics and the fundamental advantages of utilising smart mobility in a smart city ecosystem, an overview of how smart mobility fits within smart cities is given. The study also discusses several other opportunities and difficulties with smart mobility. Finally, the key services and applications within smart mobility that are anticipated to emerge in the upcoming years are examined along with potential future trends and scope. The applications are focused on providing the customers with fast, low-powered, and energy efficient devices. And, since interconnects rule the timing constant and power consumption issues, it becomes necessary to address them for applications purposes too. To observe an energy efficient and fast interconnect design an H-model topology is proposed that can be used for the IoT applications of both RC and RLC interconnect circuits as shown in Fig. 7.2(a) and (b) [113].



(a)



(b)

Fig. 7.2. Proposed H-model (a) RC ladder (b) RLC ladder

Since, in the modern world a day would not be complete without the internet. Every job relies on technology, which is developing daily. The Internet of Things has a lot of potential in the future. The term "Internet of Things" (IoT) refers to a network of physical objects that have sensors, computers, networks, and software incorporated in them. Examples of these objects include autos and other products. This allows the objects to communicate with each other and gather data. The circuit efficiency has a significant impact on the system's overall performance. The device's interconnect performance suffers greatly with scale-down technology. The system may lag as a result of power consumption and dissipation problems brought on by the smaller computing module. These problems might also result in signal delays. Improving timing restrictions alone won't improve the circuit's performance. For improved circuit efficiency, power dissipation and consumption must also be taken into account. With the advancement of current technology, one of the essential components for establishing a link between multiple sensors or interfaces for wireless information transmission is now the Internet. In addition, low power consumption and high speed are necessary for IoT apps to work efficiently on devices. In the proposed H-model, the focus was to reduce not only resistance but inductance as well for overall improvement in the interconnect circuits. Upon reduction of the parasitic components of the long wires, their performance parameters were also improved as shown in Table 7.1.

Table 7.1. Comparison table in terms of performance parameters

Evaluation parameters	Power (μW)	Delay (ps)
Proposed RLC interconnect circuit	0.94	218.18
Proposed π-RC lumped interconnect circuit	427.61	1010
Proposed π-RC distributed interconnect circuit	0.117	263.72

Table 7.1 tabulates the performance of interconnect circuits using H-model for simple RC and RLC lines. Even though the suggested interconnected circuit achieves superior delay reduction results, the computation cost issue still exists. In addition, the suggested interconnect topology also reduces power consumption, however, distributed RC networks consume less power as compared to RLC interconnect circuit. This can be due to addition of another parasitic component into the wire. As a result, noise-related problems may arise in the device and cause additional errors. Wire routing and placement design must also be considered to study these challenges since the area becomes one of the critical variables for tiny device wireless transmission. Additionally, spacing can be taken into account for RLC circuits to lessen the issue of crosstalk noise, which will improve communication and minimise data distortion. When comparing the RLC circuit to the π-RC lumped interconnect circuit, power consumption is improved by 99.78%, and when comparing the RLC circuit to the π-RC distributed interconnect circuit, power consumption is increased by 87.5%. RLC interconnected over RC lumped and distributed circuits showed delay improvements of 78.39% and 17.26%, respectively.

7.2 FUTURE SCOPE

The calculation cost issue still exists even though the suggested interconnected circuit performs better in terms of time constant and power saving. In addition, the suggested interconnect topology makes use of ramp input, which is inexpensive to create and simple to integrate into Internet of Things applications for quick data transfer; yet, noise-related problems may arise in the device and cause additional errors. Since area becomes one of the key considerations for tiny device wireless transmission, wire routing and placement designs must also be taken into consideration in order to investigate these issues. Additionally, RLC

circuit spacing can be taken into account to lessen the issue of crosstalk noise for improved communication and reduced data distortion.

LIST OF PUBLICATIONS

LIST OF PUBLICATIONS

(JOURNAL)

[1] H. Bhardwaj, S. Jain, H. Sohal, "An innovative interconnect structure with improved Elmore delay estimation model for deep submicron technology," *Analog Integrated Circuits and Signal Processing*, Vol. 111(3), pp. 419–439, 2022. https://doi.org/10.1007/s10470-022-02012-3 **(SCI)**

[2] H. Bhardwaj, S. Jain, H. Sohal, "Power Optimization using Current-mode signalling technique for IoT Applications," *Measurement: Sensors, 24*, pp. 1-10, 2022, https://doi.org/10.1016/j.measen.2022.100494 **(Scopus, ESCI)**

[3] H. Bhardwaj, S. Jain, H. Sohal, "Global RC Interconnects with ADL Buffers for Low-power Applications," *Micro and Nano Systems*, 2024**.** DOI: 10.2174/0118764029298466240508091306 **(Scopus, ESCI)**

[4] H. Bhardwaj, S. Jain, H. Sohal, "Design of Global RLC interconnect circuit with analytical delay model," *Recent Advances in Electrical and Electronic Engineering*, 2024 DOI: 10.2174/0123520965298473240314065311 **(Scopus, ESCI)**

[5] H. Bhardwaj, S. Jain, H. Sohal, "Energy Optimization for RC and RLC Interconnect Design in Low Power VLSI," Micro and Nano systems, 2023 DOI: https://doi.org/10.2174/0118764029277963231127105304 **(Scopus, ESCI)**

(CONFERENCE)

[1] H. Bhardwaj, S. Jadav, H. Sohal and S. Jain, "Optimized Crosstalk Circuit for Long Wire Copper Interconnects using 45nm CMOS Inverter," *2020 IEEE International Women in Engineering (WIE) Conference on Electrical and Computer Engineering (WIECON-ECE)*, Bhubaneswar, India, 2020, pp. 392-395, Doi: 10.1109/WIECON-ECE52138.2020.9397927 **(IEEE SCOPUS-indexed)**

[2] H. Bhardwaj, S. Jain and H. Sohal, "A Novel Interconnect Structure for DSM Technologies," *2021 IEEE International Women in Engineering (WIE) Conference on Electrical and Computer Engineering (WIECON-ECE)*, Dhaka, Bangladesh, 2021, pp. 21-24, Doi: 10.1109/WIECON-ECE54711.2021.9829705 **(IEEE SCOPUS-indexed)**

[3] H. Bhardwaj, S. Jain and H. Sohal, "Design of Buffer Circuit for Global Interconnects Using Adiabatic Dynamic Logic," *2021 7th International Conference on Signal*

Processing and Communication (ICSC), Noida, India, 2021, pp. 311-315, Doi: 10.1109/ICSC53193.2021.9673404. **(IEEE SCOPUS-indexed)**

[4] H. Bhardwaj, S. Jain and H. Sohal, "Design of Global Interconnects using Adiabatic Dynamic Logic employing FinFET Technology," *2021 6th International Conference on Signal Processing, Computing and Control (ISPCC)*, Solan, India, 2021, pp. 450-455, Doi: 10.1109/ISPCC53510.2021.9609385. **(IEEE SCOPUS-indexed)**

REFERENCES

REFERENCES

[1] V. R. Kumbhare *et al*., "High-Speed Interconnects: History, Evolution, and the Road Ahead," in *IEEE Microwave Magazine*, vol. 23, no. 8, pp. 66-82, Aug. 2022, Doi: 10.1109/MMM.2021.3136268.

[2] J. A. Davis et al., "Interconnect limits on giga scale integration (GSI) in the 21st century," Proc. of the IEEE, vol. 89, no. 3, pp. 305-324, 2001.

[3] R. A. Johnson et al., "Advanced thin-film silicon-on-sapphire technology: microwave circuit applications," IEEE Trans. Electron Devices, vol. 45, no. 5, pp. 1047-1054, 1998.

[4] D. S. Gardner et al., "Layered and homogeneous films of aluminium and aluminium/silicon with titanium and tungsten for multilevel interconnects," IEEE J. Solid-State Circuits, vol. 20, no. 1, pp. 94-103, 1985.

[5] P. Kapur et al., "Technology and reliability constrained future copper interconnects: performance implications," IEEE Trans. Electron Devices, vol. 49, no. 4, pp. 598-604, 2002.

[6] D. Zhou, F. P. Preparata and S. M. Kang, "Interconnection delay in very high-speed VLSI," in *IEEE Transactions on Circuits and Systems*, vol. 38, no. 7, pp. 779-790, July 1991, Doi: 10.1109/31.135749.

[7] R. Chandel, S. Sarkar and R. P. Agarwal, "On mitigating power and delay in VLSI interconnects," *Canadian Conference on Electrical and Computer Engineering, 2005.*, Saskatoon, SK, Canada, 2005, pp. 1533-1536, Doi: 10.1109/CCECE.2005.1557270.

[8] L. Zhao, "All About Interconnects", Dec. 2017. [Online] Available: https://semiengineering.com/all-about-interconnects/

[9] *"Introduction to VLSI physical design,"* 2013 *SlideShare*. Available at: https://www.slideshare.net/slideshow/1-introduction-to-vlsi-physical design/18893277

[10] *Prof. Saraswat, "Interconnect scaling," pdf.*

[11] A. Sharma, and D. Duggal, "VLSI Interconnect delay and crosstalk models – A Review," *International Journal of innovations in Engineering and Technology (IJIET)*, Vol. 6 Issue 4, pp. 12-18, April 2016 (ISSN: 2319-1058).

[12] TV, "Exploring Interconnects in VLSI PD: Interconnect Series - 1." https://www.techsimplifiedtv.in/2023/10/exploring-interconnects-in-vlsi.html (accessed Jun. 25, 2024).

[13] "Interconnect Scaling trends – VLSI System Design." https://www.vlsisystemdesign.com/interconnect-scaling-trends/ (accessed Jun. 25, 2024).

[14] D.K. Sharma B.K. Kaushik R.K. Sharma, (2011),"VLSI interconnects and their testing: prospects and challenges ahead", Journal of Engineering, Design and Technology, Vol. 9 Iss 1 pp. 63 – 84. Permanent link to this document: http://dx.doi.org/10.1108/17260531111121477

[15] T. TV, "Exploring Interconnects in VLSI PD: Interconnect Series - 1." https://www.techsimplifiedtv.in/2023/10/exploring-interconnects-in-vlsi.html

[16] D. Hodges, H. Jackson, and R, Saleh, "Interconnect Design," in *Analysis and Design of Digital Integrated Circuits in Deep Sub-micron Circuits*, 3rd ed., New York, NY, USA: McGrraw-Hill (Inc.) Higher Educ, 2004, Ch. 10, pp. 441-477.

[17] "Today's analog/RF designs need interconnect inductance extraction - Tech Design Forum Techniques," www.techdesignforums.com. https://www.techdesignforums.com/practice/technique/todays-analog-rf-designs-need-interconnect-inductance-extraction/ (accessed Jul. 13, 2024).

[18] "VLSI Interconnects Credits: David Harris Instructed by Shmuel Wimer - ppt download," slideplayer.com. https://slideplayer.com/slide/17905384/ (accessed Jul. 13, 2024).

[19] "Distributed rc Model," SlideShare, Feb. 07, 2022. https://www.slideshare.net/slideshow/distributed-rc-model/251121445 (accessed Jul. 13, 2024).

[20] S. Saini, "A Novel Approach to Reduce Delay and Power in VLSI Interconnects," www.academia.edu, Jan. 2010, Accessed: Jul. 13, 2024. [Online]. Available: https://www.academia.edu/268923/A_Novel_Approach_to_Reduce_Delay_and_Power_In_VLSI_Interconnects

[21] T. Jemilehin, "The Elmore Delay Model in VLSI Design," All About Circuits, Nov. 11, 2020. Available: https://www.allaboutcircuits.com/technical-articles/elmore-delay-model-transistor-sizing-vlsi-design/ (accessed Jul. 13, 2024).

[22] K. Zhao, Y. Hu, G. Du, Y. Zhao, J. Dong, "Mechanisms of Scaling Effect for Emerging Nanoscale Interconnect Materials," Nanomaterials, 2022, 12, 1760 pp. 1-14. https://doi.org/10.3390/nano12101760.

[23] "Predictive Technology Model (PTM)", Ptm.asu.edu, (2020). http://ptm.asu.edu/

[24] H. Bhardwaj, S. Jain, and H. Sohal, "An innovative interconnect structure with improved Elmore delay estimation model for deep submicron technology," Analog

Integrated Circuits and Signal Processing, Vol. 111, pp. 1-21, 2022. 10.1007/s10470-022-02012-3.

[25] P. Saxena and N. Menezes and P. Cocchini and D.A. Kirkpatrick, Repeater scaling and its impact on CAD, IEEE Transactions on Computer-Aided Design, vol. 23, no. 4, pp. 451463, 2004.

[26] M. Mcdermott, "Interconnects in CMOS Technology," 2018 [Online]. https://cupdf.com/document/lecture-13-interconnects-in-cmos-mcdermotvlsi1mainlectureslecture13pdf.html

[27] R. Gupta *et al*., "The Elmore delay as a bound for RC trees with generalized input signals," in *32nd ACM/IEEE Design Automation Conference*, 1995.

[28] R. Fonseca *et al*., "Elmore based Interconnect delay models," 2005.

[29] E. Erdemli, and M. Aksoy, "A new approach for N-stage RC ladder networks based on Elmore Delay Model," (in Turkish), *Journal of Science and Engineering Sciences*, Vol 39-7, pp. 19-35, 2020.

[30] Tao Lin, E. Acar and L. Pileggi, "h-gamma: an RC delay metric based on a gamma distribution approximation of the homogeneous response," *1998 IEEE/ACM International Conference on Computer-Aided Design. Digest of Technical Papers (IEEE Cat. No.98CB36287)*, San Jose, CA, USA, 1998, pp. 19-25, Doi: 10.1109/ICCAD.1998.144239.

[31] C. J. Alpert, A. Devgan, and C. Kashyap, "A two moment RC delay metric for performance optimization," In Proceedings of the 2000 international symposium on Physical design (ISPD '00), Association for Computing Machinery, New York, NY, USA, pp. 69–74, 2000. https://doi.org/10.1145/332357.332377

[32] S. S. Sapatnekar, "RC Interconnect Optimization under the Elmore Delay Model," *31st Design Automation Conference*, San Diego, CA, USA, 1994, pp. 387-391, Doi: 10.1145/196244.196430.

[33] Soo-Young Oh, Won-Young Jung, Jeong-Taek Kong and Keun-Ho Lee, "Interconnect modelling in deep submicron design," *ICVC '99. 6th International Conference on VLSI and CAD (Cat. No.99EX361)*, Seoul, Korea (South), 1999, pp. 73-80, Doi: 10.1109/ICVC.1999.820828.

[34] Cong, Zhigang Pan, Lei He, Cheng-Kok Koh and Kei-Yong Khoo, "Interconnect design for deep submicron ICs," *1997 Proceedings of IEEE International Conference on Computer Aided Design (ICCAD)*, San Jose, CA, USA, 1997, pp. 478-485, Doi: 10.1109/ICCAD.1997.643579.

[35] U. Ramadass et al., "A Novel Interconnect Structure for Elmore Delay model with Resistance-Capacitance-Conductance Scheme," *American Journal of Applied sciences*, Vol. 10-8, pp. 881-892, 2013 (ISSN: 1546-9239), Doi: 10.3844/ajassp.2013.881.892.

[36] A. B. Kahng and S. Muddu, "Analysis of RC interconnections under ramp input," ACM Trans. Des. Autom. Electron. Syst, 2, April 1997, pp. 168–192. https://doi.org/10.1145/253052.253137

[37] R. Mita, G. Palumbo and M. Poli, "Propagation Delay of an RC-Chain with a Ramp Input," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 1, pp. 66-70, Jan. 2007, Doi: 10.1109/TCSII.2006.885397.

[38] M. Sathe, and N. Sarwade, "Performance comparison of CMOS and FinFET based circuits at 45nm technology using SPICE," *Mugdha Sathe Int. Journal of Engineering Research and Applications*, Vol. 4Issue 7, pp. 39-43, July 2014

[39] Xu Huang, Liu Kun, Huang Xiao-Zong, and He Zhengrong, "An Effective Method for Interconnect Delay Optimization of ASIC's," DEStech Transactions on Engineering and Technology Research, 2019. 10.12783/dtetr/ecae2018/27740.

[40] P.K. Rahi *et al.*, "Design and Simulation of CMOS Schmitt trigger," *IJISET – International Journal of Innovative Science, Engineering and Technology*, Vol. 3 Issue 8, pp. 305-309, August 2016.

[41] S. Shahana and A. Ahmed, "Design of a High-Speed Buffer using Schmitt Trigger Technique," vol. 03, no. 07, pp. 1153–1156, 2015, Accessed: Aug. 09, 2024. [Online]. Available: https://www.ijvdcs.org/uploads/451326IJVDCS6134-190.pdf

[42] "Using Schmitt Triggers for Low Slew-Rate Input," 2002. Accessed: Aug. 09, 2024. [Online]. Available: https://www.microsemi.com/document-portal/doc_view/130021-ac161-using-schmitt-triggers-for-low-slew-rate-input-app-note#:~:text=A%20Schmitt%20trigger%20is%20a

[43] M. Donato *et al.*, "A noise-immune sub-threshold circuit design based on selective use of Schmitt-trigger logic," May 2012, Doi: https://doi.org/10.1145/2206781.2206792.

[44] F. Arith, "Low voltage CMOS Schmitt Trigger in 0.18μm technology," *IOSR Journal of Engineering*, vol. 03, no. 03, pp. 08-15, Mar. 2013, Doi: https://doi.org/10.9790/3021-03320815.

[45] M. Kumar, P. Kaur, and S. Thapar, "Design of CMOS Schmitt Trigger," Jul. 2012.

[46] A. K. Biswas, "Wide Voltage Input Receiver with Hysteresis Characteristic to Reduce Input Signal Noise Effect," *ETRI Journal*, vol. 35, no. 5, pp. 797–807, Oct. 2013, Doi: https://doi.org/10.4218/etrij.13.0112.0632.

[47] H. Rashid, Md. Mamun, Md. S. Amin, and H. Husain, "Design of a Low Voltage Schmitt Trigger in 0.18 um CMOS Process with Tunable Hysteresis," *Modern Applied Science*, vol. 7, no. 4, Mar. 2013, Doi: https://doi.org/10.5539/mas.v7n4p47.

[48] S. Kundra and P. Soni, "Low Power Schmitt Trigger." Accessed: Aug. 09, 2024. [Online]. Available: https://core.ac.uk/download/pdf/234642998.pdf

[49] R. Bhavani and M. Manikumari, "Interconnect Delay and Power Optimization Using Schmitt Trigger as Alternate Approach to Buffer Insertion," IJSR, 2014. Accessed: Aug. 09, 2024. [Online]. Available: https://www.ijsr.net/archive/v3i10/T0NUMTQxMTE=.pdf

[50] P. Tejaswi and A. Srinivasulu, "A Schmitt Trigger by means of Complimentary Pass Transistor Logic." Accessed: Aug. 09, 2024. [Online]. Available: https://www.ijera.com/special_issue/ASPIC%202012/B005007.pdf

[51] Y.G. Goswami, and N. Saxena, "Determination of various performance parameters using CMOS and CNT via 4T Schmitt trigger," *International Journal of Innovative Science and Research Technology*, Vol. 3 Issue 6, pp. 287-291, June 2018.

[52] M.R. Elmezayen *et al.*, "Accurate analysis and design of Integrated single Input Schmitt trigger circuits," Journal of Low Power Electronics and Applications, pp. 1-20, 2020.

[53] M. Kaur, N. Gupta and A. K. Singh, "Impact of geometrical parameters on performance of MWCNT based chip interconnects," *2017 Progress in Electromagnetics Research Symposium - Spring (PIERS)*, St. Petersburg, Russia, 2017, pp. 988-993, Doi: 10.1109/PIERS.2017.8261888.

[54] S. Sharma, "Performance analysis of inverter gate using FinFET and Planar Bulk MOSFET Technologies," *International Journal of Electrical and Electronics Engineers (IJEEE)*, Vol. 7 Issue 1, pp. 439-506, 2015.

[55] R. Hajare *et al.*, "Performance analysis of FinFET based Inverter circuit, NAND and NOR gate at 22nm and 14nm node technologies," *International Journal on Recent and Innovation Trends in Computing and Communication*, Vol. 3 Issue 5, pp. 2527-2532, 2015.

[56] R Narang, M Saxena, and M Gupta, "Exploring the applicability of well optimized dielectric pocket tunnel transistor for future low power applications," Superlattices and Microstructures, 2019.

[57] B. Singh, A. Khosla, and S. B. Narang, "Low Power Bus Encoding Techniques for Memory Testing," *Microelectronics and Solid State Electronics*, vol. 2, no. 3, pp. 45–51, 2013, Available: http://article.sapub.org/10.5923.j.msse.20130203.02.html

[58] X. Huang *et al.*, "An Effective method for Interconnect delay optimization for ASIC's," in *2018 3rd International Conference on Electrical, Control and Automation Engineering (ECAE 2018)*, pp. 255-258.

[59] Z. Farjad, N. Masoumi, "Performance improvement of global interconnects using combined techniques of low swing transceiver and buffer insertion in nano technologies," IEEE, 978–1–4577–2209–7/11, 2011.

[60] R. A. Alunj, G. K. Kharate, "Design of DG FinFET based driver circuits for energy efficient sub threshold global interconnects," *Analog Integr Circ Sig Process*, Vol. 113, pp. 41–60, 2022, https://doi.org/10.1007/s10470-022-02051-w

[61] S. Kumar, A. Singh, S. Suresh, and Gawande, "Low Power Adiabatic Logic Design for VLSI Applications," *International Journal of Scientific Research & Engineering Trends*, vol. 7, pp. 2395–566, 2021, Accessed: Aug. 09, 2024. [Online]. Available: https://ijsret.com/wp-content/uploads/2021/07/IJSRET_V7_issue4_623.pdf

[62] Y. Takahashi, Y. Fukuta, T. Sekine and M. Yokoyama, "2PADCL: Two Phase drive Adiabatic Dynamic CMOS Logic," *APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems*, Singapore, 2006, pp. 1484-1487, Doi: 10.1109/APCCAS.2006.342503.

[63] A. Mishra and N. Singh, "Low Power Circuit Design Using Positive Feedback Adiabatic Logic (PFAL)," IJSR, 2014. Accessed: Aug. 09, 2024. [Online]. Available: https://www.ijsr.net/archive/v3i6/MDIwMTQxMTA=.pdf

[64] V. Bindal, "Adiabatic Logic Circuit Design," *IJISET -International Journal of Innovative Science, Engineering & Technology*, vol. 3, 2016, Accessed: Aug. 09, 2024. [Online]. Available: https://ijiset.com/vol3/v3s3/IJISET_V3_I3_84.pdf

[65] D. Shinghal, and A. Saxena. "Adiabatic Logic Circuits: A Retrospect," 2013.

[66] M. Shamian Bin Zainal, S. Anuar, A. Hamzah, S. Bin Ubin, A. Shis, and L. Chai, "IMPLEMENTATION OF ADIABATIC DYNAMIC LOGIC IN BIT FULL ADDER," 2006. Accessed: Aug. 09, 2024. [Online]. Available: https://core.ac.uk/download/pdf/12007682.pdf

[67] B.P. Bhuvana, V.S. Kanchana Bhaaskaran, "Performance Analysis of 2N-N-2P Adiabatic Logic Circuits for Low Power Applications using FinFET," Procedia Computer Science, Volume 115, 2017, Pages 166-173, ISSN 1877-0509, https://doi.org/10.1016/j.procs.2017.09.122.

[68] M. P. Frank, R. W. Brocato, B. D. Tierney, N. A. Missert, and A. H. Hsia, "Reversible Computing with Fast, Fully Static, Fully Adiabatic CMOS," *arXiv.org*, 2020. https://arxiv.org/abs/2009.00448 (accessed Aug. 09, 2024).

[69] N. Anuar, Y. Takahashi, and T. Sekine, "Adiabatic Logic versus CMOS for Low Power Applications." Accessed: Aug. 09, 2024. [Online]. Available: https://nazrulanuar.com/author/wp-content/uploads/2011/12/itc_paper2009.pdf

[70] M. Bhargavi & J. Suman, and B. Malakar, "A REVIEW PAPER ON ADIABATIC LOGIC BASED VARIOUS FULL ADDERS", 56. 2022.

[71] S. Jadav, G. Khanna, A. Kumar, and G. Saini, "Low power high throughput current mode signalling technique for global VLSI interconnect," *2010 International Conference on Computer and Communication Technology, ICCCT)*, pp. 290-295, 2010, 10.1109/ICCCT.2010.5640513

[72] R. Islam, "High-Speed On-Chip Signaling: Voltage or Current-Mode?" IETE Journal of Research, 2018, Vol. 67, pp. 1-10, 10.1080/03772063.2018.1534618.

[73] M. Jayamma and R. S. Boya, "Design of Different Interconnect Circuit Techniques for Future Interconnects," Nov. 2022, Doi: 10.5281/ZENODO.7375372.

[74] S. Jadav, M. Vashishath, and R. Chandel, "High speed RLC equivalent RC delay model for global VLSI Interconnects," Analog Integrated Circuits and Signal Processing, 2019.

[75] M. Susaritha, "A Comparative Study and Analysis of Various Interconnects for Very Large-Scale Integration." ECS Advances, Volume 2, Number 3, 2023, Doi: 10.1149/2754-2734/acfb21.

[76] B. Balaji and R. Naik, "DELAY ESTIMATION MODEL FOR HIGH-SPEED INTERCONNECTS IN VLSI," International Journal of Current Engineering and Scientific Research (ijcesr), vol. 12, no. 4, pp. 2394-0697, 2017, Doi: https://doi.org/10.21276/ijcesr.2017.4.12.48

[77] M. Kavicharan, N. S. Murthy and N. Bheema Rao, "A closed-form delay estimation model for current-mode high speed VLSI interconnects," *2013 The International Conference on Technological Advances in Electrical, Electronics and Computer Engineering (TAEECE)*, Konya, Turkey, 2013, pp. 502-506, Doi: 10.1109/TAEECE.2013.6557325.

[78] M. Dave, M. Baghini, and D. Sharma, "Current Mode Interconnect," 2010. Accessed: Aug. 09, 2024. [Online]. Available: https://www.ee.iitb.ac.in/~smdp/DKStutorials/interconnects-notes.pdf

[79] Y.I. Ismail *et al.*, “Equivalent Elmore Delay for RLC Circuits,” 1999.

[80] K.T. Tang and E.G. Friedman,” Lumped versus Distributed RC and RLC Interconnect Impedances,” in *Proc. 43rd IEEE Midwest Symp. On Circuits and Systems*, 2000.

[81] S. Selahattin, S. Lamichhane, and K. Sayil, “Crosstalk noise mitigation using a transmission gate with varied gate bias,” *Analog Integrated Circuits and Signal Processing*, Vol. 105:183–190, 2020, https://doi.org/10.1007/s10470-020-01706-w(0123456789().,-volV)(0123456789().,-volV)

[82] R. K. Pandey, E. F. Pribadi, and P. CP. Chao, “Technology scaling impact on VLSI interconnect and low swing signaling technique,” *Microsyst Technol, Vol.* **28**, pp. 2337–2351, 2022, https://doi.org/10.1007/s00542-022-05329-1

[83] K. Tang and E. G. Friedman, "Lumped versus distributed RC and RLC interconnect impedances," *Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems (Cat.No.CH37144)*, Lansing, MI, USA, 2000, pp. 136-139 vol.1, Doi: 10.1109/MWSCAS.2000.951604.

[84] Y. I. Ismail, E. G. Friedman and J. L. Neves, "Equivalent Elmore delay for RLC trees," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, no. 1, pp. 83-97, Jan. 2000, Doi: 10.1109/43.822622.

[85] R. Venkatesan, J. A. Davis and J. D. Meindl, "Compact distributed RLC interconnect models - part IV: unified models for time delay, crosstalk, and repeater insertion," in *IEEE Transactions on Electron Devices*, vol. 50, no. 4, pp. 1094-1102, April 2003, Doi: 10.1109/TED.2003.812509.

[86] M. S. Ullah and M. H. Chowdhury, "Analytical Models of High-Speed RLC Interconnect Delay for Complex and Real Poles," in *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol. 25, no. 6, pp. 1831-1841, June 2017, Doi: 10.1109/TVLSI.2017.2654921.

[87] D. Harris, “High Speed CMOS VLSI Design Lecture 4: Interconnect RC,” 1997. Available: chrome-extension://efaidnbmnnnibpcajpcglclefindmkaj/https://pages.hmc.edu/harris/class/hal/lect4.pdf

[88] Haley-frost, “PPT - EE4271 VLSI Design Interconnect Optimizations Buffer Insertion PowerPoint Presentation - ID:5905631,” Slide Serve, Mar. 16, 2019. https://www.slideserve.com/haley-frost/ee4271-vlsi-design-interconnect-optimizations-buffer-insertion-powerpoint-ppt-presentation (accessed Jul. 26, 2024).

[89] V. Wason and K. Banerjee, “A probabilistic framework for power-optimal repeater insertion in global interconnects under parameter variations,” In Proceedings of the 2005 international symposium on Low power electronics and design (ISLPED '05), Association for Computing Machinery, New York, NY, USA, pp. 131–136, 2005.

[90] H. Bhardwaj, S. Jain, and H. Sohal, “Design of Global Interconnects using Adiabatic Dynamic Logic employing FinFET Technology,” pp. 450-455, 2021. 10.1109/ISPCC53510.2021.9609385.

[91] M. Elmezayen, W. Hu, A. Maghraby, I. Aboughindia, and S. Ay, “Accurate Analysis and design of Integrated Single Input Schmitt Trigger Circuits,” Journal of Low Power Electronics and Applications, Vol. 10, No. 3, pp. 1-20, June 2020. DOI: 10.3390/jlpea10030021

[92] Dipali Patidar, Alok Kumar Mishra, Dhandapani Vaithiyanathan, Baljit Kaur. "An Energy-Efficient Conditional-Boosting Flip-Flop with Conditional Pulse for Low Power Application", 2022 IEEE 3rd Global Conference for Advancement in Technology (GCAT), 2022

[93] “Design of VLSI Systems,” *book.huihoo.com*. https://book.huihoo.com/design-of-vlsi-systems/ch07/ch07.html (accessed Jul. 26, 2024).

[94] H. Bhardwaj, S. Jain, and H. Sohal, “Design of Buffer Circuit for Global Interconnects Using Adiabatic Dynamic Logic,” pp. 311-315, 2021. 10.1109/ICSC53193.2021.9673404.

[95] R.S.G. Bhavani, and M. Manikumari, "Interconnect Delay and Power Optimization Using Schmitt Trigger as Alternate Approach to Buffer Insertion," International Journal of Science and Research (IJSR), Vol. 3, Issue 10, pp. 484-488, October 2014.

[96] V. Raghunathan, M.B. Srivastava, R.K. Gupta, “A survey of techniques for energy-efficient on-chip communication,” Proceedings of the 40thannual Design Automation Conference (DAC ’03), Association for Computing Machinery, New York, NY, USA (2003), pp. 900-905, 10.1145/775832.776059

[97] Cadence PCB Solutions, “Interconnect Design in Low Power VLSI”.

[98] P. Sethi, and S.R. Sarangi, “Internet of things: architecture, protocols, and application,” J. Electr. Computer Eng., 2017, 10.1155/2017/9324035, Article ID 9324035

[99] L. Podmore, “Integrating Nanotechnology into the Internet of Things,” AZoNano, 2022.

[100] H. Bhardwaj, S. Jain, and H. Sohal, "Power optimization using current-mode signalling technique for IoT applications," Measurement: Sensors, Volume 24, 2022, 100494, ISSN 2665-9174, https://doi.org/10.1016/j.measen.2022.100494.

[101] H. Bhardwaj, S. Jain, and H. Sohal, "Design of Global RLC Interconnect Circuit with Analytical Delay Model," Recent Advances in Electrical & Electronic Engineering (Formerly Recent Patents on Electrical & Electronic Engineering), 17, 2024. 10.2174/0123520965298473240314065311.

[102] A.B. Kahng, and S. Muddu, "An analytical delay model for RLC interconnects", *IEEE Trans. Comput. Aided Des. Integrated Circ. Syst.*, vol. 16, no. 12, pp. 1507-1514, 1997. http://dx.doi.org/10.1109/43.664231

[103] X. Qi, B. Kleveland, Z. Yu, S. Wong, R. Dutton, and T. Young, "On-chip inductance modelling of VLSI interconnects", *2000 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.00CH37056)* 09-09 February 2000, San Francisco, CA, USA, 2000.

[104] H. Sarhan, "Today's analog/RF designs need interconnect inductance extraction - Tech Design Forum Techniques," September 19, 2019, *www.techdesignforums.com*. https://www.techdesignforums.com/practice/technique/todays-analog-rf-designs-need-interconnect-inductance-extraction/

[105] Weeks, and L. Walter, "Transmission and Distribution of Electrical Energy," New York, NY: Harper & Row, 1981, ISBN 978-0060469825.

[106] K. Banerjee and A. Mehrotra, "Analysis of on-chip inductance effects for distributed RLC interconnects," in IEEE Transactions on computer-aided design of integrated circuits and systems, vol. 21, no. 8, pp 904-915, Aug. 2002. doi:10.1109/TCAD.2002.800459

[107] M. Kavicharan, N.S. Murthy, and N. Bheema Rao, "A closed-form delay estimation model for current-mode high speed VLSI interconnects," In: 2013 the international conference on technological advances in electrical, electronics and computer engineering (TAEECE), IEEE, pp 502–506, 2013.

[108] R.K. Pandey, E.F. Pribadi, and P.CP. Chao, "Technology scaling impact on VLSI interconnect and low swing signaling technique," Microsyst Technol, 28, 2337–2351, 2022. https://doi.org/10.1007/s00542-022-05329-1

[109] R. Venkatesan, J.A. Davis, and J.D. Meindl, Compact distributed rlc interconnect models—part IV: Unified models for time delay, crosstalk, and repeater insertion. *IEEE Trans. Elec. Dev.,* vol. 50, no. 4, pp. 1094-1102, 2003.

[110] M. Avcai and S. Yamacli, “An Improved Elmore Delay Model for VLSI Interconnects,” Mathematical and Computer Modelling, 51(7-8), 2010. 908-914. 0895-7177.

[111] G. Gargiulo, *et. al*., “Active electrode design suitable for simultaneous EIT and EEG,” Electronics Letters, 48, 2012. 1583-1584. 10.1049/el.2012.3212.

[112] S. Paiva, M. Ahad, G. Tripathi, N. Feroz, and G. Casalino, “Enabling Technologies for Urban Smart Mobility: Recent Trends, Opportunities and Challenges,” *Sensors,* vol. 21, no. 6, p. 2143, Mar. 2021, Doi: https://doi.org/10.3390/s21062143.

[113] H. Bhardwaj, S. Jain, and H. Sohal, “Energy Optimization for RC and RLC Interconnect Design in Low Power VLSI,” Micro and Nano systems, 16, 2023, 10.2174/0118764029277963231127105304.