## JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT TEST -1 EXAMINATION- 2025

B.Tech- IV Semester (ECE)

COURSE CODE (CREDITS): 18B11EC411 (3)

MAX. MARKS: 15

COURSE NAME: ANALOG INTEGRATED CIRCUITS

COURSE INSTRUCTORS: Dr. Shruti Jain

MAX. TIME 1 Hour

Note: (a) All questions are compulsory.

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

ON	Jor solving problems		
Q.No.		CO	Marks
Q1 Q2	<ul> <li>i. For a given op-amp PSRR = 70dB, CMRR = 10<sup>5</sup>, Ad = 10<sup>5</sup> Calculate the numerical value of PSRR.</li> <li>ii. If the output voltage changes by 20V in 40 μsec. Evaluate Slew rate.</li> <li>iii. Help Sita in drawing current mirror circuit using dual input and single output differential output.</li> <li>iv. Shyam wants to evaluate input impedance of level translator circuit? Help in evaluating the same and also explain each terminology used in the formula.</li> <li>v. Draw the different configurations of an open loop operational amplifier.</li> <li>i. Determine the output voltage of the content of the interval of the content of</li></ul>	[CO 2]	5
Q2	<ul> <li>=200μV, V<sub>2</sub>= 160μV. The amplifier has differential gain of 4000 and the value of CMRR is 150.</li> <li>ii. Explain block diagram representation, ideal conditions, and equivalent circuit of an operational amplifier.</li> </ul>	[CO 2]	2+3
	i. If $I_{E1} = I_{E2} = 144.87 \mu A$ , and voltage gains are 100 and 125 respectively. Calculate average bias current and the offset current. iii An emitter biased dual input balanced output differential amplifier has the following specifications: $V_{CC} = 10V$ , $-V_{EE} = -10V$ , $R_{C1} = R_{C2} = 2.7 \text{K}\Omega$ , $R_{inl} = R \text{in}_2 = 50\Omega$ , $R_E = 3.9 \text{K}\Omega$ , $R_E = 100\Omega$ , $I_E = 2.02 \text{mA}$ , $V_{BE} = 0.715 \text{V}$ , $\beta_{ac} = \beta_{dc} = 100$ . Calculate the voltage gain (with and without darlington pair).	[CO 1]	3+2