JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATIONS-FEBRUARY 2025

B.Tech-VI Semester (ECE)

COURSE CODE (CREDITS): 18B1WEC744 (3) MAX. MARKS: 15

COURSE NAME: FPGA based Instrumentation System Design

COURSE INSTRUCTOR: Dr. Pardeep Garg MAX. TIME: 1 Hour

Note: *(a) All questions are compulsory. (b) The candidate is allowed to make suitable numeric assumptions wherever required for solving problems.*

Q. No	Question	CO	Marks
Q1	What is the need and importance of field programmable gate array (FPGA)? Discuss along with the basic building blocks of an FPGA chip.	CO-1	2
Q2	a) Are there any restrictions on the size of the design which can be implemented in an FPGA? b) '*The placement of the design affects the maximum clock frequency of the design*' justify this statement.	CO-1	1.5+1.5=3
Q3	Compare and contrast FPGA with microcontroller, ASICs on the basis of common technical features. Also, considering an example (let's say: FIR filter design), compare FPGA with Programmable DSPs.	CO-1	1.5+1.5=3
Q4	When Pascal, FORTRAN, and C languages were being used, why did Hardware Description Languages (HDLs) emerge? Discuss in detail.	CO-2	2
Q5	A digital circuit for 4-bit Ripple Carry Counter has to be designed. Write a program (design block and stimulus block) in Verilog HDL to design it.	CO-2	3
Q6	a) Is Verilog HDL a case sensitive language? How are keywords written in this? What are identifiers? Give an example of keyword and identifier. b) For modeling of real digital circuits, symbols X, Z are very important. What do these signify in Verilog HDL?	CO-2	2