

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATION- 2025

B.Tech- VI Semester (ECE)

COURSE CODE (CREDITS): 18B11EC612 (4)

MAX. MARKS: 15

COURSE NAME: VLSI TECHNOLOGY

COURSE INSTRUCTORS: Dr. Shruti Jain

MAX. TIME: 1 Hour

*Note: (a) All questions are compulsory.*

*(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems*

Q.No.	Question	CO	Marks
Q1	<p>i. A MOSFET in saturation has a drain current of 1mA for <math>V_{DS} = 0.5</math> V. If the channel length modulation coefficient is <math>0.5V^{-1}</math>, the output resistance (in the <math>k\Omega</math>) of the MOSFET is _____.</p> <p>ii. Tell Sita when the gate to source voltages is negative.</p> <p>iii. The expression for threshold voltage for the enhancement mode <math>n</math>-MOS is _____.</p> <p>iv. Drain and gate terminal of <math>n</math>- channel MOSFET are connected together. Voltage <math>V_i</math> is applied on drain terminal. For this configuration, give the voltage current relationship.</p> <p>v. The Fermi potential for depletion mode <math>p</math>-substrate is _____.</p>	[CO 1]	5
Q2	<p>i. An nMOS transistor, operating in the linear resistance region with <math>V_{DS} = 0.1</math> V, is found to conduct <math>60\mu A</math> for <math>V_{GS} = 2</math> V and <math>160\mu A</math> for <math>V_{GS} = 4</math> V. What is the apparent value of threshold voltage <math>V_{th}</math>? If <math>k_n' = 50\mu A/V^2</math>, what is the device <math>W/L</math> ratio? If the device is operated at <math>V_{GS} = 3</math> V, at what value of <math>V_{DS}</math>, will the drain end of the MOSFET channel just reach pinch off.</p> <p>ii. Explain different regions (using energy band) when MOS system works under external bias for an <math>n</math>-channel MOS transistor.</p>	[CO 2]	3 + 2
Q3	<p>i. An <math>n</math>-MOS transistor is fabricated with the following physical parameters <math>N_D = 10^{20} \text{ cm}^{-3}</math>, <math>N_A(\text{substrate}) = 10^{16} \text{ cm}^{-3}</math>, <math>W = 10\mu m</math>, <math>Y = 5\mu m</math>, <math>L = 1.5\mu m</math>, <math>x_j = 0.4\mu m</math>, reverse bias voltage = 2.5V, <math>C_{jo} = 2.98 \times 10^{-8} \text{ F/cm}^2</math>, <math>\phi_0 = 0.94</math> V. Find source diffusion capacitance and drain diffusion capacitance for linearly graded junction. Assume that there is no channel implant.</p> <p>ii. In a technology for which the gate oxide thickness is 20nm, find the value of <math>N_A</math>, for which <math>\gamma = 0.5V^{1/2}</math>. (b) If the doping level is maintained but the gate oxide thickness is increased to 100nm, what does <math>\gamma</math> become?</p>	[CO 1]	2 + 3