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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- 2025

B.Tech-VI Semester (ECE)

COURSE CODE (CREDITS): 18B11EC612 (4) MAX. MARKS: 25

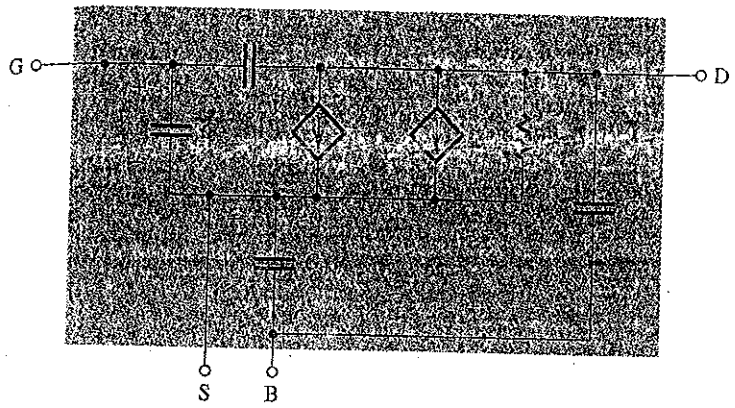
COURSE NAME: VLSI TECHNOLOGY

COURSE INSTRUCTORS: Dr. Shruti Jain MAX. TIME: 1 Hour 30 Minutes

Note: *(a) All questions are compulsory.*

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Q.No	Question	CO	Marks
Q1	i. Low noise margin is expressed as _____ ii. An *n*MOS is turned ON if its gate is connected to _____voltage. On the other hand, a *p*MOS is turned ON if its gate is connected to _____voltage. iii. For calculating V_{IH}, the driver current is in .....region. iv. For nMOS linear Enhancement load inverter *if* $v_0 = 3V$ and $v_i = 0.1V$, then driver current is in _____. v. The low output voltage is_____than low input voltage (less/ more).	2	5
Q2	i. Find the aspect ratio of driver for Resistive load inverter with the following parameters: R = 10 kΩ, V_{OL} = 0.6V, $\mu_n C_{ox} = 22.0\ \mu A/V^2$, V_{TO} = 1V, V_{DD} = 5.0V . ii. Explain the Voltage transfer characteristics of a resistive load *n*-MOS inverter. Give brief about transition width, logic swing and noise sensitivity.	4	3 + 2
Q3	Determine the *low output voltage* for Saturated E-MOS inverter when biased at V_{DD} = 4V, k'= 45μA/V², $V_{t0D} = V_{t0L}$ = 0.8V, $(W/L)_D$ =20/2, $(W/L)_L$= 2/2, V_{in} = 3.2V.	4	5
Q4	i. The *n*MOS depletion load inverter biased at V_{DD}= 5V. Assume transistor parameters of k_L = 10 μA/ V² , k_D = 100 μA/ V² , V_{TD} = 1V, V_{TL} = -2V. Calculate the power dissipated in the inverter circuit: a. when $v_i = 0.03V$ b. when $v_i = 5V$ ii. Design of a depletion load *n*MOS inverter such that the maximum power dissipation is 350μW, and the output voltage is 0.05V when v_i = 5V. The parameters are :	4	2.5 + 2.5

	$\mu_n C_{ox} = 35\mu A/V^2$, $V_{th} = 0.8V$ (enhancement-type), $V_{tL} = -2V$, $V_{DD} = 5.0V$. Assume aspect ratio for driver as 10.			
Q5	i. Sita has drawn a model (as shown in Fig 1) for her project. She is explaining the circuit to her project coordinator. You are required to help her in explaining all components and sources (as mentioned in Fig 1) with formulas. ii. Explain the effect of different scaling on voltages.  Fig 1		3	3 + 2