JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- 2025

M. Tech.-II Semester (CSE/IT/ECE/CE/BT/BI)

COURSE CODE (CREDITS): 21M1WEC239 (3) MAX. MARKS: 25

COURSE NAME: CMOS DIGITAL DESIGN TECHNIQUES

COURSE INSTRUCTORS: Dr. HARSH SOHAL MAX. TIME: 1 Hour 30 Min

Note: *(a) All questions are compulsory.*

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Q.No	Question	CO	Marks
Q1	What are the various design abstraction levels in CMOS VLSI Design? Explain in detail with the help of a block diagram highlighting the hierarchy.	CO 1	4
Q2	Explain and highlight their importance of the following terms w.r.t. CMOS IC industry: (a) NRE costs (b) RE costs (c)Scalability (d) Energy delay product (e) Reliability	CO 1	5
Q3	(a) What is the impact of interconnect parasitic on the VLSI interconnects? How can we classify different types of parasitic in IC interconnects? (b)For the wire schematic given in the Fig.1. below, draw its (a)all inclusive model (b) capacitive only model	CO2	3-4

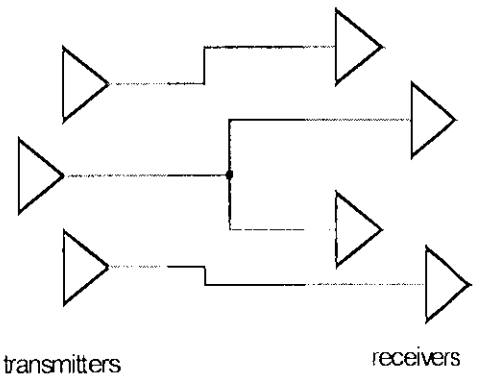

Fig.1.

Q4	Explain the concept of Ellmore Delay with the help of an RC network. What are the advantages and disadvantages of using this model for delay modeling?	CO2	3
Q5	Using complementary static CMOS Logic design technique, design and implement the following: (a) a two input NAND gate (b) $F = \overline{D + A.(B + C)}$. Also mention the Pull-up and Pull-down networks in the designed circuits.	CO3	3+3