## JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT TEST -3 EXAMINATION- 2025

## M.Tech-2<sup>nd</sup> Semester (CSE/IT)

COURSE CODE (CREDITS): 10M11CI212 (3)

MAX. MARKS: 35

COURSE NAME: ADVANCED OPERATING SYSTEMS

COURSE INSTRUCTORS: Dr. Pankaj Dhiman

MAX. TIME: 2 Hours

Note: (a) All questions are compulsory.

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Q.No			Question			CO	Marks
Q1	Assume FCFS scheduling and that the process resumes CPU only after I/O finishes.					2	6
	Process	Arrival Time	CPU Burst 1	I/O Time	CPU Burst 2		
	P1	0 ms	4 ms	3 ms	5 ms		
	P2	2 ms	3 ms	2 ms	2 ms		
	P3	3 ms	2 ms	4 ms	3 ms		
	Calculate the average waiting time and average turnaround time.						
Q2	Consider a single level paging scheme. The virtual address space is 4 MB and page size is 4 KB. What is the maximum page table entry size possible such that the entire page table fits well in one page?					6	
Q3	Discuss centralized, hierarchical, and distributed approaches to deadlock detection in a distributed system. Compare them based on: Communication overhead, Detection latency and Fault tolerance.					n.	4
Q4	Describe in detail how a process transitions through the states in a multitasking OS.					a 1	4
Q5	A system is having 3 user processes P1, P2 and P3 where P1 requires 2 units of resource R, P2 requires 3 units of resource R, P3 requires 4 units of resource R. The minimum number of units of R that ensures no deadlock is?					ts	6

Q6	Which page replacement algorithm (LRU, LFU, FIFO, and Random) is best suited for 1) Temporal locality. and 2) Frequency of access.	4	4
Q7	A certain computer system has the segmented paging architecture for	3	5
	virtual memory. The memory is byte addressable. Both virtual and		Section (A)
POST NEWS	physical address spaces contain 2 <sup>16</sup> bytes each. The virtual address space		
	is divided into 8 non-overlapping equal size segments. The memory		
	management unit (MMU) has a hardware segment table, each entry of		and make
	which contains the physical address of the page table for the segment.		
	Page tables are stored in the main memory and consists of 2 byte page		#
	table entries Assume that each page table entry contains (besides other	100	
	information) 1 valid bit, 3 bits for page protection and 1 dirty bit. How	1	
	many bits are available in page table entry for storing the aging		
	information for the page? Assume that page size is 512 bytes.		
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