JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- 2025

M. Tech.-II Semester (CSE/IT/**ECE**/CE/BT/BI)

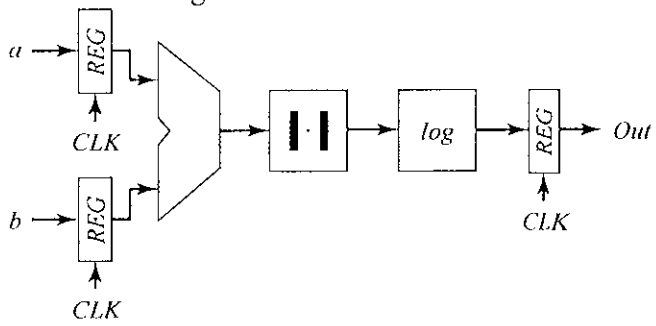
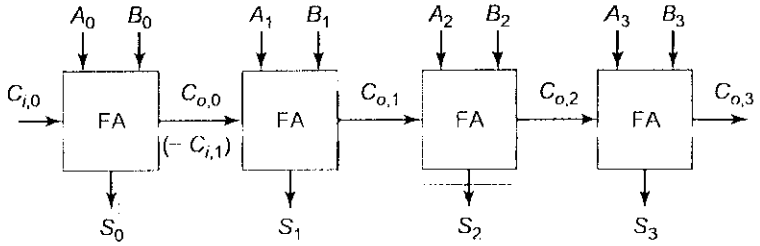
COURSE CODE (CREDITS): 21M1WEC239 (3) MAX. MARKS: 35

COURSE NAME: CMOS DIGITAL DESIGN TECHNIQUES

COURSE INSTRUCTORS: Dr. HARSH SOHAL MAX. TIME: 2 Hours

Note: *(a) All questions are compulsory.*

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Q.No	Question	CO	Marks
Q1	What are the various Building Blocks for Digital Architectures? Explain each one of them with suitable diagrams.	CO1	5
Q2	What are set up time and hold Time in digital circuits? How to calculate these? What is their role in finalizing the maximum operating frequency of Digital CMOS IC?	CO2	6
Q3	Explain the concept of pipelining in sequential circuits while giving the table for computations. Draw the pipelined design for the given reference circuit in the Fig.1. below.  Fig. 1.	CO2	6
Q4	The Fig.2. below gives a block diagram of a 4 bit Ripple Carry adder. Design the CMOS circuit implementing this block diagram functionality. Also mention the Boolean equations for all the output bits.  Fig. 2	CO3	6

Q5	For the circuit given below in Fig. 3, write the corresponding Boolean equations being implemented by the circuit.	CO3	6

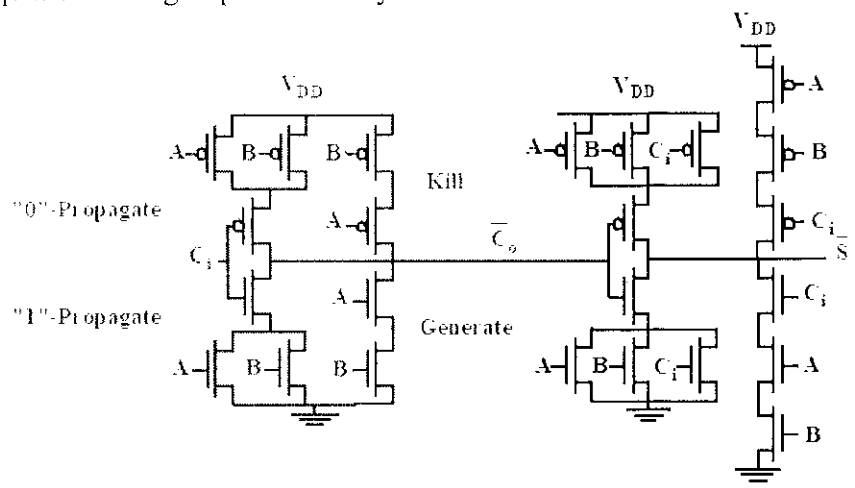


Fig.3.

Q6	(a) Do the following two circuits in Fig. 4 below implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits. b. Will these two circuits' output resistances always be equal to each other? Why or why not? c. Will these two circuits' rise and fall times always be equal to each other? Why or why not?	CO3	6

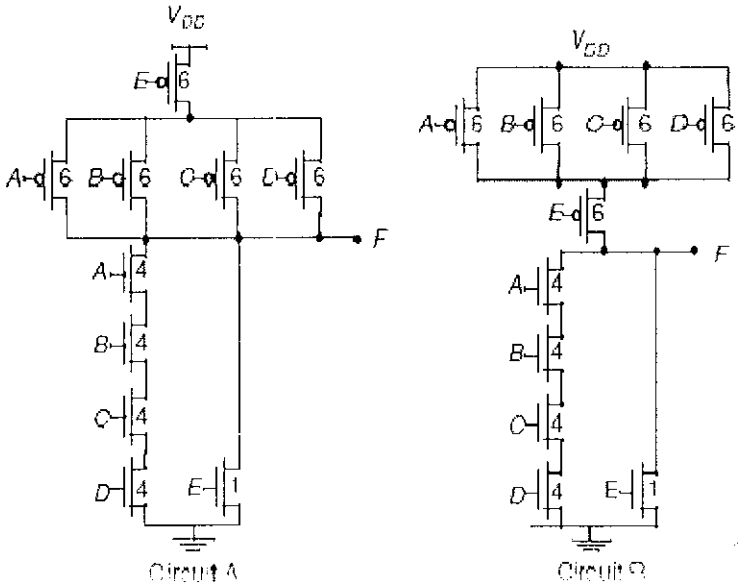


Fig. 4