JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-3 EXAMINATIONS-MAY 2025

B.Tech-VI Semester (ECE)

COURSE CODE (CREDITS): 18B1WEC744 (3) MAX. MARKS: 35

COURSE NAME: FPGA based Instrumentation System Design

COURSE INSTRUCTOR: Dr. Pardeep Garg MAX. TIME: 2 Hours

Note: (a) All questions are compulsory. (b) The candidate is allowed to make suitable numeric assumptions wherever required for solving problems.

Q. No	Question	CO	Marks

Q1	A Verilog design module code is written as follows:
	reg [8:0] flag;
	integer i;
	initial
	begin
	flag = 8'b 0001_0000;
	j=0;
	begin: block1
	while (j<8)
	begin
	if (flag[j])
	begin
	$display("Encountered a True bit at position %d", j);
	disable block1;
	end
	j=j+1;
	end
	end
	end
	i) Emphasizing on the special feature of block, discuss the functioning of the above Verilog code achieved w.r.t the special feature.
	ii) If similar kind of program has to be written in C language, the special feature of block highlighted here will be replaced by which feature option available in C language? Also, compare the functioning of Verilog language and C language w.r.t this feature.
		CO-3	3+3=6

Q2	C is a sequential language whereas Verilog HDL is a concurrent language. Justify the concurrent nature of Verilog HDL language	CO-3	4

	with the help of a programming example which uses multiple initial statements and show the output also.		
Q3	Clock is a recurring pattern pulse. A clock has to be generated of time period 20 time units which is initialized at time zero and the simulation should finish in 1500 time units. Write a Verilog design code module for the same.	CO-4	3
Q4	What is a hybrid DSP-microcontroller device? Explain any two applications where such devices are preferred over standard microcontrollers.	CO-4	2+2=4
Q5	The use of if-else loop is generally preferred in conditional statements. The if-else-if loop can be nested also. But, the nested if-else-if loop can become unwieldy if there are too many alternatives. What is the appropriate statement to be preferred in this situation? Discuss that statement employing a suitable example in Verilog HDL.	CO-4	4
Q6	Explain how an FPGA can be used as a custom microcontroller. Highlight at least two advantages of using FPGA over traditional microcontrollers.	CO-5	2+2=4
Q7	How is the sensitivity list/event OR control defined and used in Verilog HDL? Discuss with different test cases (with variable number of inputs).	CO-4	3
Q8	Explain the challenges involved in designing FPGA systems with multiple clock domains. What is metastability, and how can it be mitigated in clock domain crossing (CDC)?	CO-5	4
Q9	List any three key challenges faced in the design of multi-FPGA systems and briefly explain each.	CO-5	3