JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- 2025

B.Tech-VI Semester (ECE)

COURSE CODE (CREDITS): 18B11EC612 (4) MAX. MARKS: 35

COURSE NAME: VLSI TECHNOLOGY

COURSE INSTRUCTORS: Dr. Shruti Jain MAX. TIME: 2 Hour

Note: *(a) All questions are compulsory.*

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Q.No	Question	CO	Marks
Q1	i. _____MOS can pass logic 0 perfectly, but cannot pass logic 1 perfectly. ii. OR terms are realized by _____connections of nMOS in pull down network. iii. Three input NAND gate requires six transistors in CMOS logic _____(True / False) iv. Assuming depletion load, draw the logic diagram for $\overline{A(B+CD)}$. v. Specify the notation for *n*-diffusion, and *p*- substrate used for fabrication process. vi. For _____ (NAND/ NOR) gate the effective length of the driver transistors doubles. vii. State the conditions of Symmetric CMOS inverter to Ram.	CO-6	7
Q2	i. What are pass transistors? Explain all conditions considering example. ii. Derive *pull up to pull down* ratio if one of the inverter is fed to another inverter.	CO-6	2 + 4
Q3	Describe the stick diagram conventions used for CMOS circuits, color coding, and design rules. Consider NAND 2 CMOS logic gate and draw its transistor-level circuit. Translate this schematic into a	CO-5	5

	corresponding stick diagram, ensuring label to all layers, connections, and regions accurately.		
Q4	Describe each major fabrication step for nMOS. Use diagrams where necessary to illustrate the sequence and structure of layers formed during the process.	CO-5	5
Q5	Design a 2-input CMOS NOR gate using minimum-size transistors in a 65nm CMOS process. Assume the parameters as Minimum channel length = 65 nm, V_{DD} = 5V, V_{thn} = 0.7V, V_{thp} = -0.7V $k`$ = 60μA/V^2, minimum nMOS width = 120 nm, effective PMOS width = 2.5 × W_n. i. Draw the transistor-level circuit for a 2-input CMOS NOR gate. ii. Draw equivalent CMOS inverter stating the aspect ratios. iii. Effective resistance when output is high	CO-4	2 + 2 + 2
Q6	i. Ananya is designing CMOS inverter with the following parameters: V_{Tn} = 0.7V, V_{Tp} = -0.7V, $k_n`$ = 80μA/V$^2$, $k_p`$ = 40 μA/V^2 and V_{DD} = 3.7V, $(W/L)_n = (W/L)_p$ = 2. Help her in finding input voltage (v_i) when output voltage (v_0) is 3V. ii. State the high and low output voltages of CMOS inverter to Shyam. iii. Harsh wants to evaluate the midpoint voltage of CMOS inverter. State the conditions of pull up and pull down transistors. iv. State the typical values of threshold voltage and pass transistor threshold voltage in terms of V_{DD}.	CO-4	3 + 1 + 1 + 1