JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATION- 2025

B.Tech-V Semester (CSE/IT)

COURSE CODE (CREDITS): L-18B11CI514 (3) MAX. MARKS: 15

COURSE NAME: Computer Organization and Architecture

COURSE INSTRUCTORS: Dr. Nishant*, Dr. Praveen, Mr. Kuntal, Mr. Saurav. MAX. TIME: 1 Hour

Note: *(a) All questions are compulsory.*

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Q.No	Question	CO	Marks
Q1	An instruction is stored at location 4000 with its address field at location 4001. The address field has the value 5500. A processor register R1 contains the number 3000. Evaluate the effective address if the addressing mode of the instruction is: (i) Direct (ii) Immediate (iii) Relative (iv) Register (v) Register Indirect (vi) Indexed with R1 as index register.	CO-2	3
Q2	Using Booth's multiplication algorithm, multiply the 4-bit binary numbers +3 and −2. Show each step with updates in values.	CO-1,2	3
Q3.	A microprocessor has 32-line address bus. a) Calculate the total number of memory locations it can directly address. b) Express this amount in Megabytes (MB) and Gigabytes (GB), assuming 1 byte per location. c) If the data bus is 16 bits wide, what is the total bit capacity of this addressable memory?	[CO-1, 2]	3
Q4.	A hypothetical processor has: 16-bit instruction length, 4-bit opcode field and remaining bits are used by two address fields. (i) How many distinct instructions can be supported? (ii) How many address bits are available in each instruction? (iii) What is the maximum directly addressable memory size in bytes, assuming each address refers to 1 byte?	[CO-2]	2
Q5	(i) Show steps involved in instruction execution using instruction cycle state diagram. (ii) State difference b/w MBR and MAR.	[CO-2]	2
Q6	Based on details provided in below table, calculate CPI.	[CO-2]	2

Inst. type	Frequency	Cycle
ALU	45%	4
LOAD	35%	3
STORE	10%	2
BRNCH	10%	2