

(2.8)

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST - I EXAMINATION- 2025

B.Tech-V Semester (ECE/ECE Minor)

COURSE CODE (CREDITS):18B11EC512 (3)

MAX. MARKS: 15

COURSE NAME: Microprocessor and Interfacing

COURSE INSTRUCTORS: Dr. Shweta Pandit MAX. TIME: 1 Hour

Note:(a).All questions are compulsory.

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Q.No	Question	CO	Marks
Q1	a) Analyze the 8086 microprocessor addressing modes to identify scenarios where certain addressing methods become invalid. Justify why these modes are not permissible and illustrate your explanation with suitable examples of invalid instructions.	[1]	[1]
	b) What is the purpose of a segment register in the real mode operation of the microprocessor? Provide the default mapping of segment and offset registers addressing.		[1.5]
	c) Draw and explain the architecture of the 8086 microprocessor. Describe in detail how the instruction execution pipeline utilizes various buses for data transfer and control.		[2.5]
Q2	a) ASCII-coded data for numbers 0 to 9 is stored in a table located at a memory location starting from 1000:1000H. Write an assembly language program that uses the XLAT instruction to convert the unpacked BCD number 9 into ASCII-coded number. Store the ASCII-coded data at the memory location 2000:2000H. Write proper comments with each instruction used in the program.	[2]	[1.5+0.5]
	b) Use tables below to convert: (i) 8A3E3420H machine language instruction to assembly language (ii) MOV BX, [BP+4C00H] assembly language instruction to machine language instruction		[3]
(Note: Opcode for MOV is 100010;			
		RM Code	Addressing Mode

MOD		Function	RM Code		Addressing Mode
00	No displacement		000	DS:BX+SI	
01	8-bit sign-extended displacement		001	DS:BX+DI	
10	32-bit signed displacement		010	SS:BP+SI	
11	RM is a register		011	SS:BP+DI	
00			100	DS[SI]	
01			101	DS[DI]	
10			110	SS[BP]	
11			111	DS[BX]	

Code	W	0 (Byte)	W	1 (Word)	W	1 (Doubleword)
000		AL		AX		EAX
001		CL		CX		ECX
010		DL		DX		EDX
011		BL		BX		EBX
100		AX		AX		ESP
101		CH		BP		EBP
110		BP		BP		ESI
111		DI		DI		EDI

- Q3.**
- a) Given the Flag register structures of 8085 and 8086 microprocessors, analyze how the additional flags in 8086 enhance its functionality compared to 8085. Use labeled diagrams to justify your answer. [1]
 - b) Suppose that DS = 1300H, SS = 1400H, BP = 1500H, and SI = 0100H. Determine the address accessed by each of the following instructions, assuming real mode operation. [2] [1.5]
 - (i) MOV EAX, [BP+200H] (ii) MOV AL,[BP+SI-200H] (iii) MOV AL,[SI-0100H]
 - c) Write an assembly language program that adds AX, BX, CX, DX, and BP. Save the higher order word of the sum in SI and lower order word of the sum in DI register. Write proper comments with each instruction used in the program. [2+0.5]