JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST - 2 EXAMINATION (October 2025)
B.Tech. - III Semester (ECE-VLSI)

COURSE CODE (CREDITS): 25B11MA312 (2) MAX. MARKS: 25
COURSE NAME: NUMERICAL TECHNIQUES
COURSE INSTRUCTORS: RKB* MAX. TIME: 1 Hour 30 Mins.

Note: *All questions are compulsory. Use of scientific calculator is allowed. The candidate is allowed to make suitable numeric assumptions wherever required for solving problems.*

<table>
<tr><th>Q.No</th><th>Question</th><th>CO</th><th>Marks</th></tr>
<tr><td>Q1</td><td>Suppose that we are using a computer with a fixed word length of 5 digits. Evaluate the error due to rounding in representing the number 0.00345672. Also compute the relative error.</td><td>CO-1</td><td>2</td></tr>
<tr><td>Q2</td><td>Suppose we have the power consumption of a digital circuit measured at different supply voltages. The measured values are:
<table><tr><td>Supply Voltage (V)</td><td>1</td><td>1.2</td><td>1.5</td></tr><tr><td>Power (mW)</td><td>15</td><td>22</td><td>35</td></tr></table>Using Lagrange Interpolation, estimate the power consumption at V = 1.3.</td><td>CO-2</td><td>3</td></tr>
<tr><td>Q3</td><td>In VLSI design, propagation delay of a logic gate is often characterized at discrete load capacitance values. The following table shows the measured propagation delay (in nanoseconds) of a CMOS inverter for different load capacitances. Using Newton's Forward Interpolation, estimate the propagation delay at a load capacitance of 5 pF.
<table><tr><td>Load Capacitance (pF)</td><td>2</td><td>4</td><td>6</td><td>8</td></tr><tr><td>Propagation Delay (ns)</td><td>0.52</td><td>0.68</td><td>0.90</td><td>1.20</td></tr></table></td><td>CO-2</td><td>5</td></tr>
<tr><td>Q4</td><td>Using Stirling's interpolation technique, evaluate the value of $f(16)$ on the basis of the following observations recorded:
<table><tr><td>x</td><td>0</td><td>5</td><td>10</td><td>15</td><td>20</td><td>25</td><td>30</td></tr><tr><td>f(x)</td><td>0.0</td><td>0.0875</td><td>0.1763</td><td>0.2679</td><td>0.3640</td><td>0.4663</td><td>0.5774</td></tr></table></td><td>CO-2</td><td>5</td></tr>
<tr><td>Q5</td><td>In VLSI cell characterization, both the value of a function (delay) and its slope (sensitivity to input slew) are often required. Suppose the measured propagation delay $f(x)$ of a logic gate (in ns) at different input transition times (slew, in ns) and its slopes are given as:
<table><tr><th>x</th><th>f(x)</th><th>f '(x)</th></tr><tr><td>1</td><td>0.20</td><td>0.12</td></tr><tr><td>1.5</td><td>0.35</td><td>0.18</td></tr></table>Use Hermite interpolation to estimate the propagation delay at an input slew of $x = 1.2$.</td><td>CO-3</td><td>5</td></tr>
<tr><td>Q6</td><td>In an analog circuit, the instantaneous current through a transistor is given by the function $I(t) = 0.5 + 0.8t + 0.2t^2 \ \ (in\ mA) \ \ 0 \le t \le 6\,\mu s$. Using Simpson's 3/8 rule with $n = 6$ equal intervals, estimate the total charge $\int_0^6 I(t)dt$ (in μC) delivered during the interval [0, 6].</td><td>CO-3</td><td>5</td></tr>
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