

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
MAKE UP EXAMINATION (NOVEMBER 2025)

B.Tech. - III Semester (ECE-VLSI)

COURSE CODE (CREDITS): 25B11MA312 (2)

COURSE NAME: NUMERICAL TECHNIQUES

COURSE INSTRUCTORS: RKB*

MAX. MARKS: 25

MAX. TIME: 1 Hour 30 Mins.

Note: All questions are compulsory. Use of scientific calculator is allowed. The candidate is allowed to make suitable numeric assumptions wherever required for solving problems.

Q.No	Question	CO	Marks																
Q1	If for a transistor, the node-voltage equation reduces to a polynomial like $2x^3 - 3x - 4 = 0$ after non-dimensionalization. Solve the polynomial using Newton-Raphson method correct to 3 decimal places to find the node voltage (normalized) at the DC operating point needed before analyzing small-signal behavior or designing bias networks.	CO-2	5																
Q2	In VLSI design, propagation delay of a logic gate is often characterized at discrete load capacitance values. The following table shows the measured propagation delay (in nanoseconds) of a CMOS inverter for different load capacitances. Using Newton's Forward Interpolation, estimate the propagation delay at a load capacitance of 5 pF. <table border="1" style="margin: 10px auto;"> <tr> <td>Load Capacitance (pF)</td><td>2</td><td>4</td><td>6</td><td>8</td></tr> <tr> <td>Propagation Delay (ns)</td><td>0.52</td><td>0.68</td><td>0.90</td><td>1.20</td></tr> </table>	Load Capacitance (pF)	2	4	6	8	Propagation Delay (ns)	0.52	0.68	0.90	1.20	CO-3	5						
Load Capacitance (pF)	2	4	6	8															
Propagation Delay (ns)	0.52	0.68	0.90	1.20															
Q3	Suppose we have a gate delay measured at different input transition times. The measured gate delays at three input slews are given: <table border="1" style="margin: 10px auto;"> <tr> <td>Input Slew (ns)</td><td>0.1</td><td>0.3</td><td>0.5</td></tr> <tr> <td>Delay (ns)</td><td>0.25</td><td>0.40</td><td>0.65</td></tr> </table> Using Lagrange Interpolation, estimate the interpolated delay at input slew 0.20.	Input Slew (ns)	0.1	0.3	0.5	Delay (ns)	0.25	0.40	0.65	CO-2	5								
Input Slew (ns)	0.1	0.3	0.5																
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Q4	Suppose the following data represents the measured NMOS saturation current (I_d) versus gate voltage (V_{gs}) data: <table border="1" style="margin: 10px auto;"> <tr> <td>V_{gs}</td><td>0.8</td><td>1.0</td><td>1.2</td><td>1.4</td><td>1.6</td><td>1.8</td><td>2.0</td></tr> <tr> <td>I_d</td><td>0.05</td><td>0.40</td><td>1.10</td><td>2.10</td><td>3.45</td><td>5.10</td><td>7.05</td></tr> </table> Using the method of least square, fit a linear order equation to interpolate the value of saturation current at the gate voltage 1.5.	V_{gs}	0.8	1.0	1.2	1.4	1.6	1.8	2.0	I_d	0.05	0.40	1.10	2.10	3.45	5.10	7.05	CO-3	5
V_{gs}	0.8	1.0	1.2	1.4	1.6	1.8	2.0												
I_d	0.05	0.40	1.10	2.10	3.45	5.10	7.05												
Q5	In an analog circuit, the instantaneous current through a transistor is given by the function $I(t) = 0.3 + 0.5t + 0.4t^2$ (in mA) $0 \leq t \leq 12 \mu s$. Using Simpson's 3/8 rule with $n = 6$ equal intervals, estimate the total charge $\int_0^{12} I(t)dt$ (in μC) delivered during the interval $[0, 12]$.	CO-3	5																
