JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-3 EXAMINATION-DECEMBER-2025

B.Tech-III[rd] Semester (ECE/ECS/EE, Minor Degree)

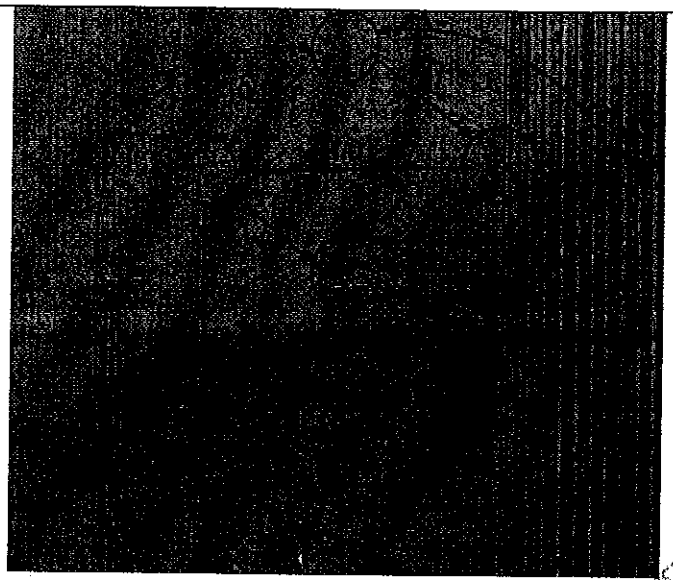
COURSE CODE (CREDITS): 25B11EC312/18B11EC312 (4) MAX. MARKS: 35

COURSE NAME: Digital Circuit Design/Digital Circuit & Logic Design

COURSE INSTRUCTOR: Dr. Pardeep Garg MAX. TIME: 2 Hours

Note: (a) All questions are compulsory. (b)The candidate is allowed to make suitable numeric assumptions wherever required for solving problems. (c) Try to attempt all parts of a question at one place.

Q. No	Question	CO	Marks
Q1	(a) Why does race-around condition occur? How can it be solved using Master-Slave flip-flop design? Discuss both in detail.	CO-4	1.5+2.5 = 4
	(b) Discuss the significance of asynchronous inputs in flip-flops along with the truth-table.	CO-4	1.5
	(c) Design a logic circuit that converts D flip-flop to J-K flip-flop.	CO-4	2.5
Q2	(a) Design a mod-160 ripple counter using cascading.	CO-4	4
	(b) A binary ripple counter is required to count up to 4095. How many flip flops are required? If the clock frequency is 9.6 MHZ, what is the frequency at the output of the most significant bit?	CO-4	1+1=2
	(c) Design a synchronous Mod-6 counter using T flip-flops.	CO-4	3
	(d) Design a 4-bit Johnson counter and discuss its functioning.	CO-4	2
Q3	A 4-bits serial-in-serial-out shift register has to be designed using D flip-flops in such a way that the data can be shifted in both (left and right) directions simultaneously on command using the same designed circuit (one circuit only). Draw the logic diagram of such design and explain its working.	CO-4	4
Q4	(a) Design a sequence detector to detect the binary sequence **1001** using Mealy type finite state machine (FSM) with the help of D flip-flops.	CO-5	5.5
	(b) Differentiate between Moore and Mealy type finite state machines (FSM).	CO-5	1.5
Q5	Obtain the state table, reduced state table, reduced state diagram for the state machine whose state diagram is shown in figure.	CO-5	1+1+1=3

			
Q6	Design the circuit for a 3-input (A, B, and C) and single output (Y) AND gate using CMOS logic family (all in one circuit only).	CO-5	2