JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

MOOC End Term Examination- 2025

B.Tech-VII Semester (CSE/IT/CE/BT/BI)

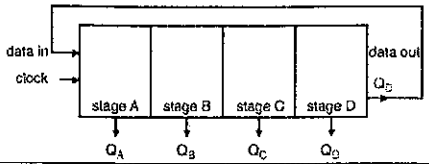
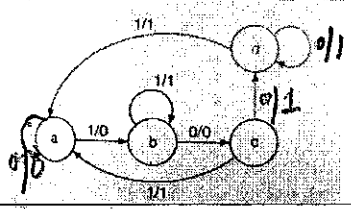
COURSE CODE (CREDITS): 25B2WEC606 (3) MAX. MARKS: 70

COURSE NAME: Digital Circuits

COURSE INSTRUCTORS: Dr. Pardeep Garg MAX. TIME: 3 Hours

Note: (a) All questions are compulsory. (b) The candidate is allowed to make suitable numeric assumptions wherever required for solving problems. (c) A Non-Programmable Scientific Calculator is allowed.

Q. No	Question	Marks
Q1	**i)** Convert Hexadecimal number (B9F.AE) to Octal. **ii)** Find out the Gray code for octal number 52. **iii)** Find the max-terms of AB + A'C. **iv)** State Redundant Literal rule.	2 2 2 1
Q2	**i)** Solve for the values of two-valued variables A, B, C, and D by solving the set of simultaneous equations: A'+AB = 0 AB = AC AB+ AC'+CD = C'D **ii)** An air-conditioning unit is controlled by four variables: temperature T, humidity H, the time of the delay D, and the day of the week W. The unit is turned on under any of the following circumstances: a) The temperature exceeds 78°F, and the time of the day is between 8 a.m. and 5 p.m. b) The humidity exceeds 85%, the temperature exceeds 78°F, and the time of day is between 8 a.m. and 5 p.m. c) The humidity exceeds 85%, the temperature exceeds 78°F, and it is a weekend. d) It is Saturday or Sunday and humidity exceeds 85%. Write a logic expression for controlling the air-conditioning unit. Simplify the expression obtained as far as possible.	3 4
Q3	Design a 32:1 multiplexer using 8:1 multiplexers (all having active-high enable input) & 2:4 decoder (all in one-circuit only).	7
Q4	Nitin just learned how a three-bit synchronous counter works in upward direction, and he is excited about building his own. He does so, and the circuit works perfectly. Draw the circuit which Nitin has designed assuming T flip flops.	7
Q5	**i)** Design how a 4-bits shift register circuit could be built from D-type flip-flops with the ability to shift data either to the right or to the left, on command. **ii)** Name the sequential circuit as shown in Figure:	6

		1
Q6	**i)** Design a circuit for conversion of D to JK flip flop. **ii)** Differentiate between combinational and sequential circuits. **iii)** Discuss the significance of asynchronous inputs in flip-flops along with the truth-table.	3 2 2
Q7	**i)** Design a sequence detector to detect the binary sequence **1001** using Mealy type finite state machine (FSM) with the help of D flip-flops. **ii)** Differentiate between Moore and Mealy type finite state machines (FSM).	5 2
Q8	**i)** A long sequence of pulses enters a 2-input 2-output synchronous sequential circuit which is required to produce an output z=1, whenever the sequence 1111 occurs. Overlapping sequences are accepted. For example, if the input is 01011111, the required output is 00000011. Draw the state diagram. **ii)** Obtain the state table, reduced state table, reduced state diagram for the state machine whose state diagram is shown in Figure: 	3.5 3.5
Q9	**i)** Compare Static RAM (SRAM) and Dynamic RAM (DRAM) in terms of their internal cell structure, data-retention mechanism, and relative advantages/disadvantages (speed, cost, density). Also mention briefly what distinguishes Read Only Memory (ROM) from these types of RAM. **ii)** A 10-bit ADC has an input voltage range of 0–5 V. **(a)** What is the resolution of this ADC in volts? **(b)** If the input analog voltage is 2.35 V, what is the corresponding digital output code (in decimal)? **(c)** A DAC with the same resolution receives a digital input of 512. What output voltage will it produce?	4 1+1+1=3
Q10	**i)** Explain the function of the accumulator, flag register, and program counter in the 8085 microprocessor. Why are these registers essential for instruction execution? **ii)** Write an 8085 assembly program to add two 8-bit numbers stored in memory locations 8000H and 8001H, and store the result at 8002H. **iii)** Differentiate between IN and OUT instructions of 8085 with an example of each. Mention how the address of the I/O device is provided.	3 2 2