JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3EXAMINATION- 2025

B.Tech- V Semester (ECE/Minor ECE)

COURSE CODE (CREDITS):18B11EC512(03) MAX. MARKS: 35

COURSE NAME: Microprocessor and Interfacing

COURSE INSTRUCTOR: Dr. Shweta Pandit MAX. TIME: 2 Hours

Note:*(a)All questions are compulsory.*

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Q.No	Question	CO	Marks
Q1	a. Which conditional jump instructions follow the comparison of signed numbers? b. What are different unconditional jump instructions? Compare them with the help of examples.	2	0.5 4
Q2	a. How IRET instruction is different from RET instruction? b. The interrupt vector for an INT 40H instruction is stored at which memory locations? c. Define procedure. Write a procedure that sums AX, BX, CX, and DX. If a carry occurs, place a logic 1 in SI. If no carry occurs, place a 0 in SI. The sum should be found in AX after the execution of your procedure.	4	1 1 1+2.5
Q3	a. What actions does the processor perform when a software interrupt instruction is executed? b. With the help of INT 21H, write an assembly language program to input a single digit number. How does the program differ if we have to input and display this single digit number through same INT 21H.	4	2 3
Q4	a. Interpret the information given by the 8AH content of CWR of 8255 PPI. b. Explain the functional block diagram of 8255 PPI along with its command word register structure.	3	1 4
Q5	Provide neat and clean diagram with proper explanation of interfacing connections of a hexadecimal keyboard to 8086 microprocessor. Mention how does the lookup table is formed to encode a key pressed by the hexadecimal keyboard.	3	7
Q6	a. Give the mapping table of different processors with its corresponding coprocessors. b. What is Direct Memory Access Mode? What is its advantage? c. Define MMX and SIMD w.r.t. processors. d. Compare and contrast among 8086, Intel Pentium and Core 2 processors.	5	1 2 2 3