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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATIONS- 2026

B.Tech.-VI Semester (ECE)

COURSE CODE (CREDITS): 18B1WEC744 (3)

MAX MARKS: 25

COURSE NAME: FPGA based Instrumentation System Design

COURSE INSTRUCTOR: Dr. Harsh Sohal

MAX. TIME: 1 Hour 30 Min

Note: (a) All questions are compulsory.

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

(c) Use of calculator is not allowed

Q.No	Question	CO	Marks
Q1	Some programmable logic devices (and PROM memory devices as well) use tiny fuses which are intentionally "blown" in specific patterns to represent the desired program. Programming a device by blowing tiny fuses inside of it carries certain advantages and disadvantages - describe what some of these are.	1	3
Q2	(a) What is instantiation? How is it useful in Verilog HDL programming? Give an example of 1bit full-adder. (b) What are the two stimulus styles provided in verilog HDL? Describe all the components with the block diagrams.	1	3+3
Q3	(a) Read the code below and decipher the block diagram of the circuit being implemented. <pre> module ripple_carry_counter(q, clk, reset); output [3:0] q; input clk, reset; //4 instances of the module T_FF are created. T_FF tff0(q[0],clk, reset); T_FF tff1(q[1],q[0], reset); T_FF tff2(q[2],q[1], reset); T_FF tff3(q[3],q[2], reset); endmodule </pre> (b) What will be required to obtain the RTL of the above code when run in a verilog HDL tool like Xilinx Vivado? Discuss	2	3+2
Q4	Explain the following basic operators. Also write a Verilog statement exemplifying the use of each one of them while using the correct symbols and syntax. 1) Concatenation 2) bitwise negation 3) logical or 4) reduction and 5) greater than	2	5

Q5	<p>(a) For the following testbench code Draw the waveforms to be obtained when we simulate module D using the stimulus code provided above.</p> <pre data-bbox="288 421 1145 952"> // Stimulus (top-level module) module stimulus; reg A, B, C; wire OUT; D d1(OUT, A, B, C); // Stimulate the inputs. Finish the simulation at 40 time units. Initial begin A= 1'b0; B= 1'b0; C= 1'b0; #10 A= 1'b1; B= 1'b1; C= 1'b1; #10 A= 1'b1; B= 1'b0; C= 1'b0; #20 \$finish; end endmodule </pre> <p>(b) Declare the following variables in Verilog:</p> <ol data-bbox="395 1059 1193 1417" style="list-style-type: none"> 1) An 8-bit vector net called a_in. 2) A 32-bit storage register called address. Bit 31 must be the most significant bit. Set the value of the register to a 32-bit decimal number equal to 3. 3) An integer called count. 4) A time variable called snap_shot. 5) An array called delays. Array contains 20 elements of the type integer. 6) A memory MEM containing 256 words of 64 bits each. 	2	3+3
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