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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- October 2018

B.Tech III Semester (CSE, IT)

COURSE CODE: 10B11EC401 MAX. MARKS: 25

COURSE NAME: DIGITAL ELECTRONICS

COURSE CREDITS: 04 MAX. TIME: 1Hr 30 min

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

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1. a) Implement the Odd Parity Generator and realize the expression using NOR-Universal Gates.

b) An LED should glow when the following conditions apply:

i. Switches A, B, C are ON.

ii. Switches A and B are ON but switch C is OFF.

iii. Switches A and C are ON but switch B is OFF.

iv. Switches C and B are ON but switch A is OFF.

Draw a truth table for this situation. Implement the function using 4:1 multiplexer.

[3 + 3 = 6] [CO3, CO4]

2. For given function $f(A, B, C, D) =$

$$\left(A+B+\overline{C}+\overline{D}\right).\left(\overline{A}+C+\overline{D}\right).\left(\overline{A}+B+\overline{C}+\overline{D}\right).\left(\overline{B}+C\right).\left(\overline{B}+\overline{C}\right).\left(A+\overline{B}\right).\left(\overline{B}+\overline{D}\right)$$

find the following

a) Write the maxterms.

b) Find the reduced expression in POS form using K-Map.

c) Realize the expression using NAND gate. **[2 + 1.5 + 3 = 6.5] [CO3]**

3. a) Draw Full Subtractor circuit using Demultiplexer with active high inputs and outputs.

b) Design three bit Binary Parallel Adder - Subtractor circuit.

c) Design a two bit comparator using AOI logic.

[2 + 1.5 + 3 = 6.5] [CO4]

4. a) Design 4 line to 16 line decoder using 2 line to 4 line decoder.

b) Design a logic circuit to produce a high output only if the input, represented by a 4 bit binary number, is greater than eleven or less than two. Implement a minimized circuit using only NAND gates.

[3 + 3 = 6] [CO1, CO4]