

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- 2026

B.Tech-VI Semester (ECE)

COURSE CODE (CREDITS): 18B11EC612 (4)

MAX. MARKS: 25

COURSE NAME: VLSI TECHNOLOGY

COURSE INSTRUCTORS: Dr. Shruti Jain

MAX. TIME: 1 Hour 30 Minutes

Note: (a) All questions are compulsory. Use of calculator is allowed.

(b) The candidate is allowed to make suitable numeric assumptions wherever required for solving problems.

| Q.No | Question | CO | Marks |
|------|--|----|-------|
| Q1 | i. Draw the VTC curve for resistive load <i>n</i> -MOS inverter. ii. Transition width is expressed as _____ iii. For calculating V_{IL} , the driver current is in _____ region. iv. For <i>n</i> MOS saturated Enhancement load inverter if $v_i = 3V$ and $v_o = 0.1V$, then driver current is in _____. v. A fast circuit dissipates more power. Justify. | 2 | 5 |
| Q2 | Evaluate source capacitance (C_s considering both oxide and junction capacitance) for <i>n</i> -channel MOS transistor with abrupt junction having parameters: substrate doping density = $10^{16}/\text{cm}^3$, polysilicon gate doping density = $2 \times 10^{20}/\text{cm}^3$, $C_{j0} = 2.942 \times 10^{-4} \text{F/m}^2$, gate oxide thickness = 50nm, length of drain = $9\mu\text{m}$, width = $4\mu\text{m}$, length of channel = $1.5\mu\text{m}$, drain to bulk voltage = 1.5V, gate to source voltage = 2V, drain to source voltage = 2V, threshold voltage = 0.8V, electron mobility = $650 \text{cm}^2/\text{V-s}$. | 3 | 5 |
| Q3 | i. A resistive load <i>n</i> MOS inverter has the following parameters: $R = 1 \text{k}\Omega$, $\mu_n C_{ox} = 22 \mu\text{A}/\text{V}^2$, $V_{TO} = 1V$, $V_{DD} = 4.0V$. Determine W/L ratio such that $V_{OL} = 1V$. ii. For resistive load <i>n</i> MOS inverter determine the V_{OH} when biased at $V_{DD} = 2.5V$, $k' = 1\mu\text{A}/\text{V}^2$, $V_{i0D} = 0.5V$, $(W/L)_D = 10$, $R = 2\text{k}\Omega$. | 4 | 3 + 2 |
| Q4 | Sita wants to work on linear E-MOS inverter. Determine the <i>high input voltage</i> when inverter is biased at $V_{DD} = 4V$, $V_{GG} = 5V$, $k' = 45\mu\text{A}/\text{V}^2$, $V_{i0D} = V_{i0L} = 0.8V$, $(W/L)_D = 10$, $(W/L)_L = 2$, $V_{out} = 0.2V$. | 4 | 5 |
| Q5 | Design the depletion load inverter such that maximum power dissipation is $350\mu\text{W}$. The inverter is biased at 5V with output voltage 0.192V, threshold voltages $V_{TOD} = 1V$, $V_{TOL} = -3V$, $K_n' = 25\mu\text{A}/\text{V}^2$. | 4 | 5 |