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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST-3 EXAMINATION - December 2018
B.Tech VIIth Semester

COURSE CODE: 12B1WEC732 MAX. MARKS: 35
COURSE NAME: Digital System Design
COURSE CREDITS: 03 MAX. TIME: 2 HRS

Note: All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means. Marks are indicated against each question in square brackets.

Q1. Answer the following questions briefly: **[2 x 5=10Marks]**

(a) Define Race. Explain the different types of races in asynchronous sequential circuits.

(b) Differentiate between flow table and transition table.

(c) Draw the model of asynchronous sequential circuit and explain.

(d) What is state equivalency theorem?

(e) What is stable state and total state?

Q2. An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the circuit are

$$Y_1 = x_1x_2 + x_1y_2' + x_2'y_1; \quad Y_2 = x_2 + x_1y_1'y_2 + x_1'y_1 \quad ; \quad z = x_2 + y_1$$

(a) Draw the logic diagram of the circuit **(b)** Derive the transition table and output map

(c) Obtain a flow table for the circuit **[2+2+4=7 Marks]**

Q3. Design a synchronous circuit that has a single-input variable and single output variable. The input data are received serially. Cause the first output bit to be same value as the first input bit in the serial string. Output z is to change thereafter only when three consecutive input bits have the same value.

(a) Construct the initial ASM diagram describing the system.

(b) Create a state table, and reduce the state table if possible.

(c) Determine the number of state variables needed, and create the state assignment to minimize the logic.

(d) Construct a new ASM diagram reflecting the minimized state machine and the state assignment.

[2 x 4 = 8 Marks]

Q4. (a) Construct the state diagram for a Mealy sequential circuit that will detect the serial input sequence $x = 010110$. When the complete sequence has been detected, then cause z to go high. **[3 Marks]**

(b) Using D flip-flop, design a synchronous modulo-8 binary counter. Use binary state assignment. **[3 Marks]**

(c) Realize SR latch using NOR gate in context to its usage in asynchronous sequential circuit. Also draw the transition diagram for the same. **[4 Marks]**

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