JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATIONS- 2026

B.Tech-V Semester (CSE/IT)

COURSE CODE (CREDITS): 18B11CI514 (3) MAX MARKS: 35

COURSE NAME: Computer Organization and Architecture

COURSE INSTRUCTOR: EMP MAX. TIME: 2 Hours

Note: *(a) All questions are compulsory.*

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

(c) Use of nonprogrammable scientific calculator is allowed

Q.No	Question	CO	Marks
Q1	A computer has a cache memory access time of 20 ns and main memory access time of 100 ns. If the cache hit ratio is 0.9, calculate the average memory access time.	CO4	2
Q2	Differentiate between Static RAM (SRAM) and Dynamic RAM (DRAM). Compare them based on structure, working principle, speed, power consumption, cost, storage capacity, refreshing requirement, and typical applications in computer systems.	CO4	3
Q3	A computer has 64 registers and 4096 memory locations. An instruction consists of: (a) Register field, (b) Opcode field (c) Memory address field. Determine the number of bits required for: A. Register field B. Address field C. Opcode field if 128 instructions are supported D. Total instruction length	CO2	4
Q4	Explain the organization of CPU registers in a basic computer system. Discuss the role of: (i) Program Counter (PC) (ii) Instruction Register (IR) (iii) Memory Address Register (MAR) (iv) Accumulator (AC) (v) Data Register (DR)	CO2	4
Q5	Describe the hardware implementation for Signed Magnitude Addition and Subtraction with a neat block diagram. Explain how arithmetic operations are performed on signed magnitude numbers, including the role of sign bits, magnitude comparison, addition/subtraction logic, and overflow handling. Illustrate the working of the circuit with suitable examples.	CO3	5

Q6	(a) Explain the working of a BCD Adder with a neat diagram. (b) Add the following BCD numbers and show correction steps clearly: $0101 + 1001$	CO3	5
Q7	Draw the flowchart and hardware implementation of Booth's Multiplication Algorithm. Using Booth's Multiplication Algorithm, multiply the following signed binary numbers and obtain the product: $M = (+13)_{10} = (01101)_2$ $Q = (-6)_{10} = (11010)_2$ After each step of the algorithm. show the contents of: A. Accumulator A B. Multiplier Q C. Extra Bit (Q_{-1}) D. Sequence Counter (*SC*)	CO3	6
Q8	A computer employs RAM chips of 512 x 8 and ROM chips of 2048 x 8. The computer system needs 2K bytes of RAM and 4K bytes of ROM. Each of the chips have an active high chip select signal *CS1* and an active low chip select signal $\overline{CS2}$. (a) How many RAM and ROM chips are needed? (b) Draw a memory address map for the system and give address range in hexadecimal for each RAM and ROM chips. (c) If the CPU has a 16 bit address bus, draw the memory connection to the CPU with suitable memory mapping circuits. Show clearly address bus, data bus and control bus connections from CPU to all the memory chips.	CO4	6