JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-3 EXAMINATION-MAY 2026

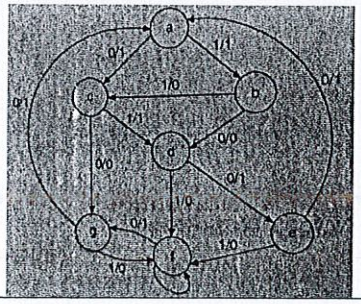
B.Tech-VII Semester (CSE/IT/BT/BI/CE)

COURSE CODE (CREDITS): 20B1WEC734 (3) MAX. MARKS: 35

COURSE NAME: Digital Systems

COURSE INSTRUCTOR: Dr. Pardeep Garg MAX. TIME: 2 Hours

*Note: (a) All questions are compulsory. (b) The candidate is allowed to make suitable numeric assumptions wherever required for solving problems. (c) A non-programmable calculator is allowed.*

| Q. No | Question | CO | Marks |
|---|---|---|---|
| Q1 | A binary ripple counter is required to count up to $16,383_{10}$. How many flip flops are required? If the clock frequency is 8.192 MHZ, what is the frequency at the output of the most significant bit? | 3 | 3 |
| Q2 | Design a mod-80 ripple counter using cascading. | 3 | 5 |
| Q3 | Design a synchronous Mod-14 counter using T flip-flops. | 3 | 6 |
| Q4 | **a)** Differentiate between Moore and Mealy type finite state machines (FSM).<br>**b)** Design a sequence detector to detect the binary sequence **1010** using Moore type finite state machine (FSM) with the help of D flip-flops. | 3<br>3 | 2<br>8 |
| Q5 | A synchronous sequential machine has a single control input x and the clock, and two outputs A and B. On consecutive rising edges of the clock, the code on A and B changes from 00 to 01 to 10 to 11and repeats itself if x=1; if at any time, x=0, it holds to present state. Draw the state diagram. | 3 | 2.5 |
| Q6 | Draw the algorithmic state machine (ASM) chart for mod-5 synchronous counter. | 3 | 2.5 |
| Q7 | Obtain the state table, reduced state table, reduced state diagram for the state machine whose state diagram is shown in figure.<br>  | 3 | 2+2+2=6 |