JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-3 EXAMINATION-MAY-2026

B.Tech- IVth Semester (CSE/IT)

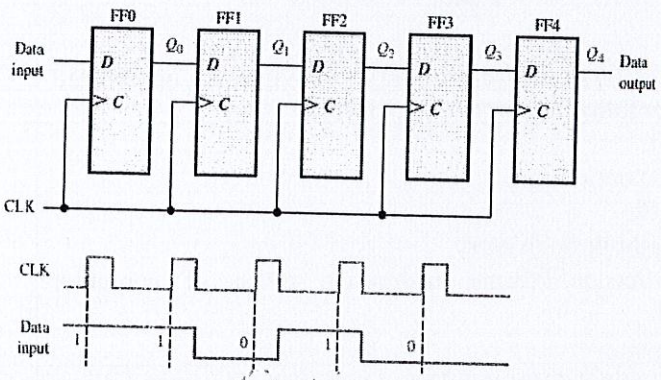
COURSE CODE (CREDITS): 25B11CI411 (3) MAX. MARKS: 35

COURSE NAME: Digital Systems and Computer Organization

COURSE INSTRUCTOR: SWT (Coordinator), EMJ, PDG, ALK, NTJ, MNS

MAX. TIME: 2 Hours

Note: *(a) All questions are compulsory. (b) The candidate is allowed to make suitable numeric assumptions wherever required for solving problems. (c) Calculator is allowed. d) Attempt all parts of a question at one place.*

Q. No	Question	CO	Marks
Q1	Show the states of the 5-bit register shown in Figure 1 for the specified data input and clock waveforms. Assume that the register is initially cleared (all 0s).  **Figure 1**	CO-3	5
Q2	Design a Synchronous Modulo-11 counter using D-Flip-Flop.	CO-3	5
Q3	**a)** Compare and contrast between RISC and CISC architectures with respect to: Instruction format, Addressing modes, Execution cycle, Pipeline efficiency etc. **b)** A machine has 24-bit instruction format. It has 16 registers and each of which is 32-bit long. It needs to support 58 instructions. Each instruction has two register operands and one immediate operand. If the immediate operand is signed integer, what will be the minimum value of immediate operand?	CO-4	3 2
Q4	Provide a step-by-step solution using Booth's Algorithm along with the flowchart to multiply 6 and 4 using register size of 4, and verify the correctness of final result.	CO-4	5
Q5	Consider a system with 3-level memory organization. Access time of L1, L2 and main memory are 1 ns, 10 ns, and 100 ns, respectively. Hit ratios of L1 and L2 are 0.7 and 0.8. Using independent or parallel memory organization for L1, L2 and Main memory, calculate the average access time of this system?	CO-3	3

<table>
<tr>
<td>Q6</td>
<td>Illustrate Immediate Addressing, Register Addressing, Direct Addressing, Indirect Addressing, Register Indirect Addressing, and Index Addressing modes in computer organization.

For the given status of memory, registers, and PC, find the effective address and operand for above mentioned addressing modes.

<table>
<tr><td>PC</td><td>300</td></tr>
<tr><td>R1</td><td>600</td></tr>
<tr><td>XR (index register)</td><td>100</td></tr>
</table>

<table>
<tr><th>Address</th><th colspan="2">Memory</th></tr>
<tr><td>300</td><td>Load to AC</td><td>Mode</td></tr>
<tr><td>301</td><td colspan="2">Address = 500</td></tr>
<tr><td>302</td><td colspan="2">Next Instruction</td></tr>
<tr><td>:</td><td colspan="2"></td></tr>
<tr><td>499</td><td colspan="2">450</td></tr>
<tr><td>500</td><td colspan="2">700</td></tr>
<tr><td>:</td><td colspan="2"></td></tr>
<tr><td>600</td><td colspan="2">800</td></tr>
<tr><td>:</td><td colspan="2"></td></tr>
<tr><td>:</td><td colspan="2"></td></tr>
<tr><td>700</td><td colspan="2">900</td></tr>
<tr><td>:</td><td colspan="2"></td></tr>
<tr><td>799</td><td colspan="2">250</td></tr>
<tr><td>:</td><td colspan="2"></td></tr>
<tr><td>802</td><td colspan="2">325</td></tr>
<tr><td>:</td><td colspan="2"></td></tr>
<tr><td>900</td><td colspan="2">300</td></tr>
</table>
</td>
<td>CO-3</td>
<td>5</td>
</tr>
<tr>
<td>Q7</td>
<td>a) Let R1 (8-bit reg.) = 11010010, CF (carry flag) = 0. What will be updated value of R1 and CF after following operations on R1?
(i) Shift Left
(ii) Shift Arithmetic Right
(iii) Rotate Left
(iii) Rotate Right through carry
b) Explain the Fetch-Decode-Execute instruction cycle of computer organization in detail.</td>
<td>CO-4</td>
<td>2

2</td>
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<tr>
<td>Q8</td>
<td>What is Cache Memory Mapping? Compare Direct mapping, Fully associative, and K- way set associative Cache Mapping techniques.</td>
<td>CO-3</td>
<td>3</td>
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