JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- 2026

B.Tech-VI Semester (ECE)

COURSE CODE (CREDITS): 18B11EC612 (4) MAX. MARKS: 35

COURSE NAME: VLSI TECHNOLOGY

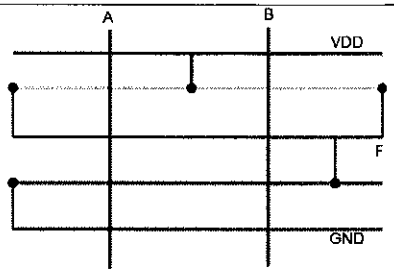
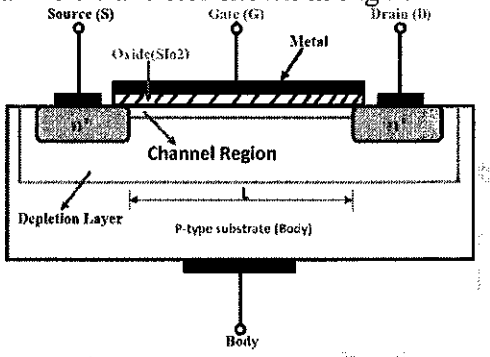
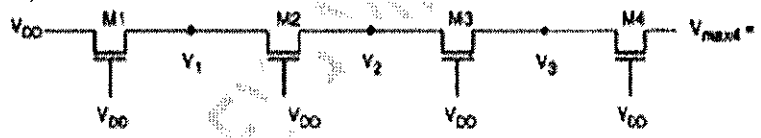
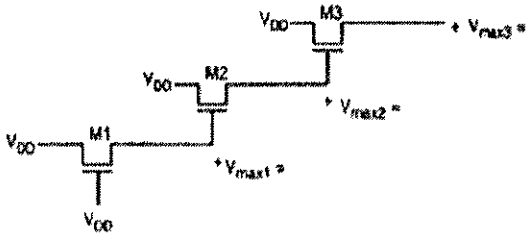
COURSE INSTRUCTORS: Dr. Shruti Jain MAX. TIME: 2 Hour

Note: (a) All questions are compulsory.

(b) The candidate is allowed to make suitable numeric assumptions wherever required for solving problems

(c) Use of calculator is allowed

Q.No	Question	CO	Marks
Q1	i. Drain terminal and gate terminal of a *n*- channel MOSFET are connected together. Voltage V_x is applied on gate terminal. For this configuration, write the current and voltage. ii. State different pull up networks for an inverter. iii. If one inverter drives another inverter, what is the Z_{PU}/Z_{PD} ratio? iv. Draw the equivalent inverter diagram for a 2-input CMOS NOR gate. v. A threshold voltage of −1.0 V corresponds to which type of MOS transistor?	CO1	5
Q2	i. For a digital logic inverter fabricated in a 0.8μm CMOS technology for which $(W/L)_n = 6$ and $(W/L)_p = 8$, $k'_n = 150\mu A/V^2$, $V_{tn} = 0.7V$, $k'_p = 62\ \mu\ A/V^2$, $V_{tp} = -0.85V$, $V_{DD} = 3.3V$, $C = 0.05pF$. Find the output resistance for $v_O = V_{OL}$. ii. Explain the four different voltages and indicate them on the characteristic curve. Also arrange and label them in ascending order according to their voltage values. iii. Consider a CMOS inverter with the following parameters V_{OH}=5V, V_{OL}= 0V, V_{IH}=3.5 V, V_{IL}=1.5 V. Calculate Noise margin.	CO3	2 + 2 + 1
Q3	Design the logic diagram using CMOS logic for logic expression $f(A,B,C) = \overline{A + B(C)}$. Find the equivalent CMOS inverter, assuming $(W/L)_n = (W/L)_p = 10$.	CO4	5
Q4	i. What condition ensures symmetry in a CMOS inverter? ii. Calculate the W/L ratio of PMOS and NMOS for symmetry given μ_n/μ_p. If $\mu_n/\mu_p = 3$, $L_n = L_p = 1$ μm. Find W_n and W_p. iii. Sita is plotting VTC curve of CMOS inverter. She wants to calculate the switching threshold V_M voltage. Help her in finding the midpoint voltage. V_{DD} =3 V, $V_{tn} = \lvert V_{tp} \rvert = 0.5$ V, $\mu_n/\mu_p = 2$, $W_p = W_n$.	CO4	1 + 2 + 2
Q5	i. Describe the process of converting a circuit diagram into a stick diagram. ii. Draw the circuit diagram corresponding to the stick diagram shown in Fig. 1 and clearly label the source and drain terminals.	CO5	3 + 2

	 Fig 1 : Stick diagram		
Q6	Explain the fabrication process, including all relevant notations used involved in building a MOS transistor shown in Fig 2.  Fig 2	CO5	5
Q7	i. The chain of pass-transistor logic is given with logic '1' transfer. Discuss and derive the voltages at every node (V_1, V_2, V_3, and V_{max4}) as shown in Fig 3. Assume V_{th1} is the threshold voltage of transistor $M1$, V_{th2} for $M2$ and so on.  Fig 3 ii. In Fig. 4, during logic '1' transfer, each pass transistor drives another pass transistor. Discuss and derive the voltages at each node, namely V_{max1}, V_{max2}, and V_{max3}. Assume V_{th1} is the threshold voltage of transistor $M1$, V_{th2} for $M2$ and so on.  Fig 4 iii. State the typical values of V_{th} , V_{thpass}	CO6	2 + 2 + 1