

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATION- 2026

B.Tech-V Semester (CSE/IT)

COURSE CODE (CREDITS): 18B11CI514 (3)

MAX. MARKS: 15

COURSE NAME: COMPUTER ORGANIZATION AND ARCHITECTURE

COURSE INSTRUCTOR: EMP

MAX. TIME: 1 Hour

Note: (a) All questions are compulsory.

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

(c) Use of calculator is not allowed

Q.No	Question	CO	Marks
Q1	Analyze the evolution of computers from the second to the fifth generation with respect to major hardware technologies.	CO-1	2
Q2	Identify and explain the different types of bus structures used in a computer system. Discuss the roles of the address bus and control bus in transferring information between the CPU registers and memory.	CO-1	2
Q3	Explain the organization of CPU registers in a basic computer system. Discuss the role of: (i) Program Counter (PC) (ii) Instruction Register (IR) (iii) Memory Address Register (MAR) (iv) Accumulator (AC) (v) Data Register (DR)	CO-2	3
Q4	Draw a neat block diagram of the Von Neumann architecture and critically analyze its organization and the Von Neumann bottleneck. Compare the Von Neumann and Harvard architectures with respect to memory organization, memory access, instruction execution speed, and their suitability for modern embedded systems.	CO-1	4
Q5	A computer has 32 registers and 1024 memory locations. An instruction consists of: (a) Register field, (b) Opcode field (c) Memory address field. Determine the number of bits required for: A. Register field B. Address field C. Opcode field if 64 instructions are supported D. Total instruction length	CO-2	4