

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -I EXAMINATION- 2026

B.Tech-III Semester (ECE/ECS/EE VLSI/ Minor ECE)

COURSE CODE (CREDITS): 25B11EC312 (4)

MAX. MARKS: 15

COURSE NAME: DIGITAL CIRCUIT DESIGN

COURSE INSTRUCTOR: Dr. Shruti Jain

MAX. TIME: 1 Hour

Note: (a) All questions are compulsory.

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

(c) Use of calculator is not allowed

Q.No	Question	CO	Marks
Q1	i. Convert $(1001011000001110)_2$ into octal, hexadecimal, Gray code. Also determine the final output for an odd-parity generator ii. Determine the 7's complement of the decimal number 57.05 iii. Using the principle of duality, find the dual of the Boolean expression: $A' B + B' C$ iv. Convert the excess three code 01000111 into Gray code.	CO1	2 + 1 + 1 + 1
Q2	Using 8-bit signed binary representation, evaluate $(-45) - (-78)$ by: i. 2's complement method ii. 1's complement method Verify that both methods give the same decimal result.	CO1	2.5 + 2.5
Q3	i. Using Karnaugh-map minimization, obtain the simplified Boolean expression for each of the following functions and realize the resulting expression using universal gates $F(A, B, C, D) = \sum m(0, 1, 2, 3, 8, 9, 10, 11, 14, 15)$ ii. A digital circuit has the following function: $F(A, B, C, D) = \sum m(0, 1, 4, 5, 6, 7, 10, 11, 12, 14, 15) + d(2, 3, 8, 9)$. Using K-map: (a) Find the minimum SOP expression. (b) Find the minimum POS expression. (c) Determine which implementation requires fewer gates.	CO2	2.5 + 2.5