

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATION- 2026

B.Tech-V Semester (CSE/IT)

COURSE CODE (CREDITS): 25B1WCI543 (2)

MAX. MARKS: 15

COURSE NAME: Embedded Software Development

COURSE INSTRUCTOR: EMP

MAX. TIME: 1 Hour

Note: (a) All questions are compulsory.

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

(c) Use of calculator is allowed

Q.No	Question	CO	Marks
Q1	Using the simplified triangular revenue model, calculate the percentage of total addressable revenue lost for an embedded product with an expected lifetime of $2W = 72$ weeks if its launch is delayed by $D = 6$ weeks. Show your formulas and step-by-step calculations.	CO-1	2
Q2	Why does a single-purpose processor typically achieve higher throughput (performance) and consume less power than a general-purpose processor? Identify two key architectural overheads present in a general-purpose processor that are eliminated in a custom, single-purpose design.	CO-1	2
Q3	In embedded pipeline design, concurrency is said to "decouple" a system's throughput from its latency. Using the example of a digital camera, explain how two systems can have identical processing latencies of 0.25 seconds per task yet deliver a 2 times speedup in task completion rate.	CO-1	3
Q4	Describe how "Conditional Execution" operates in the ARM instruction set. Why does this architectural feature provide a significant performance advantage over traditional branch instructions, and what is its performance trade-off?	CO-1	4
Q5	Under standard operating conditions, the Program Counter (PC) in a 3-stage ARM7 pipeline experiences a constant offset because the Fetch stage is always two instructions ahead of the Execute stage. a) Explain why the PC offset is exactly 8 bytes when the processor is operating in ARM state. b) Deduce how this PC offset changes (in bytes) if the processor dynamically switches to Thumb state, and justify your answer based on Thumb instruction width.	CO-1	4