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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- October 2018

B.Tech CSE/IT/ECE VII Semester

COURSE CODE: 13B1WCI731

MAX. MARKS: 25

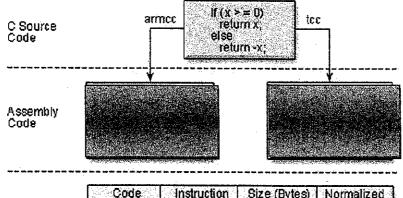
COURSE NAME: ARM BASED EMBEDDED SYSTEM DESIGN

COURSE CREDITS: 03

MAX. TIME 1.5Hr

Note: All questions are compulsory. Each question carries equal marks. Carrying of mobile phone during examinations will be treated as case of unfair means.

1. (a) Write and compare the assembly code for ARM and Thumb architecture. What are the advantages of Thumb over ARM architecture?



Comparison

Code	Instruction	Size (Bytes)	Normalized
ARM			
Thumb			

- (b) Explain the following:
 - i. Enter Debugging State
 - ii. Action In Debug State
 - iii. Debug Extensions
- 2. (a) Write all ARM Condition Codes fields.

Op co de	Mnemonic	Interpretation	Status flag state for
[31:28]	extension		execution

(b) Let's assume that label1 and label2 correspond to addresses 0x1C30 and 0x2C30, respectively. Further, assume that the address of the "BEQ" instruction is 0x0100 and of the "BL" instruction is 0x0120

BEQ label1

BL label2

label1

175

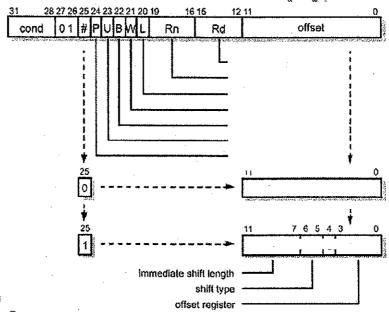
label2 .

What is the Byte offset for BEQ and BL? What is the Word offset for BEQ and BL? Write the machine code representation for BEQ label1 and BL label2

3. (a) Explain the following format for Data Processing Instruction Binary Encoding

31 2	8 27 26	25	24 21	20	19 16	15	12	11		0
cond	00	#	opcode				Rd		operand 2	

- (b) Write and explain all Data Processing Instructions
- 4. (a) Explain the following format for Data Transfer Instructions (LDR/STR)



- (b) Calculate the offset for STR r2, label
 - say this instruction is at address 0xF8
 - say "label" corresponds to address 0x1FF
- List all the Multiply Instructions with opcode, mnemonics, meanings and effects.
- (b) WAP to calculates a scalar product of two vectors, 20 long.
 - r8 and r9 points to the two vectors
 - r11 is the loop counter
 - r10 stores the result