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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- Oct 2017

B.Tech 3rd Semester

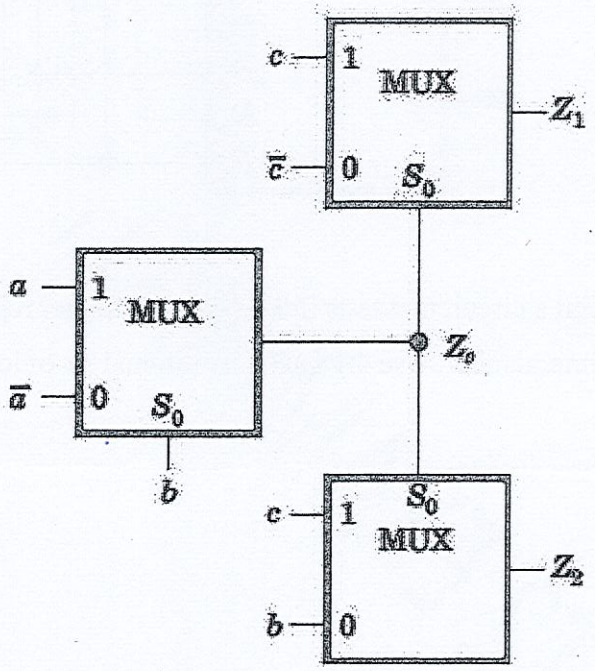
COURSE CODE: 10B11EC401 MAX. MARKS: 25

COURSE NAME: Digital Electronics

COURSE CREDITS: 4 MAX. TIME: One Hour Thirty Minutes

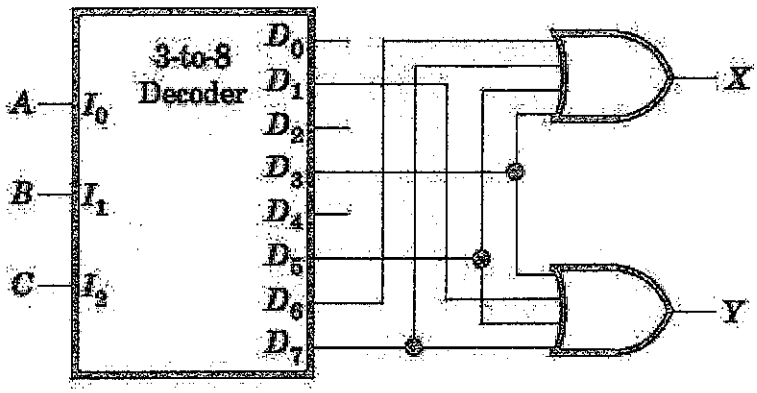
Note: All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.

1. Find Z_1 for the mux network shown in figure below: 2



2. Realize a 4-Bit magnitude comparator using logic gates. 3
3. Implement X-NOR, X-OR and NOR logic gates using 2:1 mux. 3
4. Realize 4-bit look ahead carry adder. Compare it with 4-bit parrallel adder in terms of carry propagation delay. 3
5. Realize Decimal to BCD priority encoder using logic gates. 2
6. Implement the following boolean expression using 8:1 multiplexer: 2
   $F(A,B,C,D) = \sum m\,(1,3,5,10,11,13,14) + \text{don't care}\,(0,2)$

7. What are the disdavantages of S-R flip flop. How are these disadvantages overcomed in J-K flip flop. Explain using characterstics table. 3
8. Implement a 1:16 line demux using only 2:4 decoders with enable input and no other logic gate. 2
9. The building block shown in figure is a active high o/p decoder. Find simplified outputs X and Y in terms of A,B and C. 2



10. Design a circuit that tests if the decimal number represented by 4-bit binary number is a prime number. Use 4:1 mux and minimal no of logic gates. 3