Dr Naveen

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST -III EXAMINATION- Dec 2017
B.Tech III Semester

COURSE CODE: 10B11EC401 MAX. MARKS:35
COURSE NAME: Digital Electronics
COURSE CREDITS: 4 MAX. TIME: Two Hr

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

Q1) Design a 4 bit bidirectional serial in serial out shift register using D flip flop. **(3)**

Q2) Design a 3 bit synchronous UP / DOWN counter using JK flip flop. **(3)**

Q3) Convert the decimal number 3.248 X 10^4 to a single – precision floating point binary Number. **(3)**

Q4) Add the following numbers **(3)**

(i) $DF_{16} + AC_{16}$ (ii) $13_8 + 25_8$ (iii) BCD numbers 01100111 + 01010011

Q5) Minimize the following expression F (ABCDE) using K map, where A is the MSB

$F = \sum_m(0, 1, 4, 8, 12, 13, 15, 16, 17, 23, 29, 31)$ **(3)**

Q6) Design a 3 bit synchronous counter which counts the following sequence. **(5)**

0 → 3 → 1 → 4 → 7 → 5 → 2 → 6

Q7) Design SR flip flop from JK flip flop using K map. **(5)**

Q8)

a) Why do we prefer synchronous counters over asynchronous counters. **(5)**

b) What is the difference between a latch and a flip flop.

c) List any three applications of shift registers.

d) What is race around condition in J K flip flop.

e) Implement NAND gate using 2 X 1 MUX.

Q9) Implement the following Boolean expression F (A, B, C, D) where A is MSB and D is LSB bit, using 4 X 1 MUX by considering MSB bits as select lines.

(5)

$F=\sum_m(0, 1 3 4, 7, 9, 11, 12)$