Vivek Sehgal

Roll No:.....

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-1 – September 2017

B.Tech (CSE & IT) 7th Semester

COURSE CODE: 13B1WCI731 MAX. MARKS: 15

COURSE NAME: Arm Based Embedded System Design

COURSE CREDITS: 03 MAX. TIME: 1 Hrs

Note: *All questions are compulsory. The carrying of mobile phone during examinations will be treated as a case of unfair means.*

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1. (a) Draw and explain the classical distribution of ARM CORTEX Series for 8 bit, 16 bit and 32 bit [3]

   (b) What is the difference between RISC and CISC? Explain using tabular format [2]

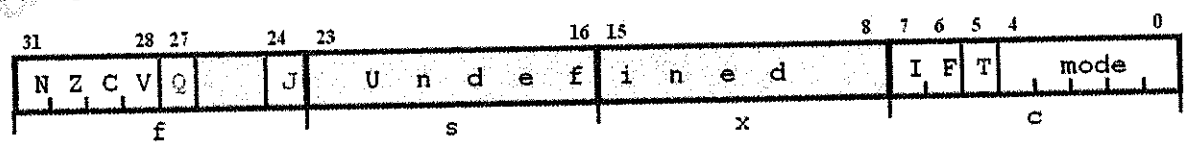
2. (a) Tell about the Exception Handling in ARM processor. What does the ARM Core do automatically for every exception? [2]

   (b) Why should you design the DSP algorithm in general ARM architecture so that saturation is not required? [1]

   (c) Explain the structure of ARM ADS (ARM Developer Suite) Tools [2]

3. (a) Draw and explain the registers bank of ARM architecture for following operating modes:
   i. User
   ii. FIQ
   iii. IRQ
   iv. Supervisor
   v. Abort
   vi. Undef
   vii. System [3]

   (b) Expain the bit distribution of following ARM Program Status Registers



[2]

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