Dr Sruti

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION - 2022

B.Tech. VIII Semester (ECE)

COURSE CODE: 19B1WEC831 MAX. MARKS: 25

COURSE NAME: DIGITAL CMOS ICs

COURSE CREDITS: 03 MAX. TIME: 1 Hour 30 Min

Note: *All questions are compulsory. Marks are indicated against each question in square brackets.*

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1. In logic design, complex gates such as AOI and OAI are often used to combine the functions of several gates into a single gate, thus reducing the chip area and parasitic of the circuit. Consider OAI32 whose logic function is $Z=\overline{(A+B+C)(D+E)}$.
   a. Draw the full CMOS circuit diagram
   b. Draw the domino CMOS circuit diagram which implements *Z*. **[5]**

2. Evaluate the optimum stage effort for the logic cascade as shown in Fig 1. Assume symmetric gates with $r = 2.5$. **[5]**

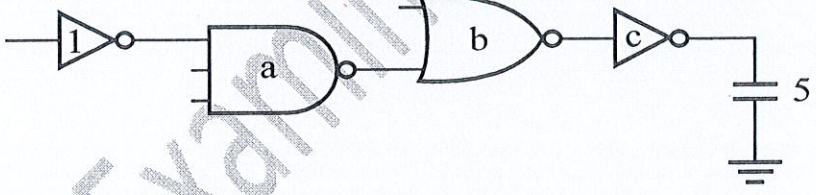

Fig 1

S	R	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
1	1	Q	$\overline{Q}$

Fig .2

3. Design the circuit using CMOS logic for Fig 2. **[5]**
4. Geeta wants to draw *CMOS D latch* using transmission gates. Help her in drawing the circuit. Also, explain the circuit. **[5]**
5. a) Draw and explain the Sense amplifier-based cross-coupled latch.
   b) Shyam wants to remove the erroneous evaluation problem from the circuit. Which circuit he will use to remove this problem? **[2.5 + 2.5]**