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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

MAKEUP EXAMINATION- 2016

B.Tech 6th Semester

COURSE CODE: 10B11CI613 MAX. MARKS: 25

COURSE NAME: Computer Organization & Architecture

COURSE CREDITS: 4 MAX. TIME: 1Hr 30 Min

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

Q1. Justify the following statements with suitable reasons, examples, and diagrams wherever required **[5 marks]**

a) One of the consequences of Moore's law is the reduction in overall speed

b) K- Way set associative mapping is a combination of direct mapping and associative mapping.

c) MIPS is not a general metric to measure performance of processors.

d) Multiple bus system is better than single bus system.

e) Interrupt priority approach is better than disabled interrupt approach to handle multiple interrupts.

Q2. Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 80 MHz and M2 has a clock rate of 100 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows: **[5 marks]**

Instruction Class	Machine M1 – Cycles/Instruction Class	Machine M2 – Cycles/Instruction Class	Frequency
A	1	2	60%
B	2	3	30%
C	4	4	10%

(a) Calculate the average CPI for each machine, M1, and M2.

(b) Calculate the average MIPS ratings for each machine, M1 and M2.

(c) Which machine has a smaller MIPS rating?

Q3. a) Derive the mathematical expression for speed up that can be achieved using n processor system instead of a uniprocessor system. What is a law of diminishing returns in multi core systems? **[2.5 marks]**

b) Suppose that we can improve the floating point instruction performance of machine by a factor of 15 (the same floating point instructions run 15 times faster on this new machine). What percent of the instructions must be floating point to achieve a Speedup of at least 4? **[2.5 marks]**

Q4. Explain the following with suitable diagrams and examples: **[5 marks]**

a) Unified versus split cache

b) Cache coherence problem and its solutions

c) Moore's law and its importance

d) Mapping functions

e) Write through and write back policy

Q5. Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size. **[5 marks]**

a) Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

b) Assume an associative cache. Show the address format and determine the following Parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

c) Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in set, number of sets in cache, number of lines in cache, size of tag.