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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- 2016

B.Tech IV Semester

COURSE CODE: 10B22CI421

MAX. MARKS: 25

COURSE NAME: Computer Organization

COURSE CREDITS: 04

MAX. TIME: 1Hr 30 Min

Note: All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means. Each question carries equal marks.

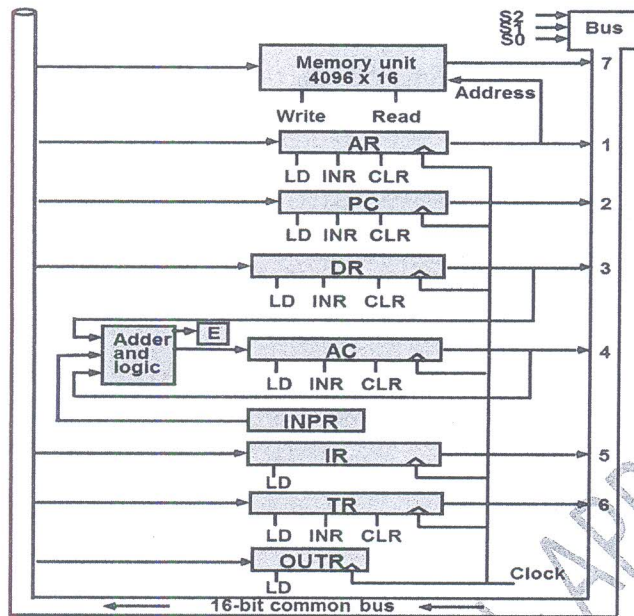
1. (a) The following control inputs are active in common bus system shown in Figure below. For each case, specify the register transfer that will execute during the next clock transition.

	S ₂	S ₁	S ₀	LD of register	Memory	Adder and Logic Circuit
a.	1	1	1	IR	Read	_____
b.	1	1	0	PC	_____	_____
c.	1	0	0	DR	Write	_____
d.	0	0	0	AC	_____	Add

- (b) Fill-up the following control inputs are active in common bus system shown in Figure below. For each case of register transfer that will execute during the next clock transition.

	S ₂	S ₁	S ₀	LD of register	Memory	Adder and Logic Circuit
a.						
b.						
c.						
d.						

- a. $AR \leftarrow PC$
b. $IR \leftarrow M[AR]$
c. $M[AR] \leftarrow TR$
d. $AC \leftarrow DR, DR \leftarrow AC$ (done simultaneously)



2. Draw and explain the Hardwired Control Organization of basic computer with instruction register.
3. Draw and explain the common bus architecture for fetch and decode phase.

T0: AR ← PC (S0S1S2=010, T0=1)

T1: IR ← M [AR], PC ← PC + 1 (S0S1S2=111, T1=1)

T2: D0, ..., D7 ← Decode IR(12-14), AR ← IR(0-11), I ← IR(15)

4. What are the various phases of instruction cycle? Explain the instruction cycle with a flow chart to determine the type of instruction.
5. Explain the following register and memory reference instructions with symbolic description of RTL

	r:
CLA	rB ₁₁ :
CLE	rB ₁₀ :
CMA	rB ₉ :
CME	rB ₈ :
CIR	rB ₇ :
CIL	rB ₆ :
INC	rB ₅ :
SPA	rB ₄ :
SNA	rB ₃ :
SZA	rB ₂ :
SZE	rB ₁ :
HLT	rB ₀ :

Symbol	Operation Decoder	Symbolic Description
AND	D ₀	
ADD	D ₁	
LDA	D ₂	
STA	D ₃	
BUN	D ₄	
BSA	D ₅	
ISZ	D ₆	