JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- 2016

B.Tech IV Semester

COURSE CODE: 10B22CI421   MAX. MARKS: 35

COURSE NAME: Computer Organization

COURSE CREDITS: 04   MAX. TIME: 2HRS

Note: All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means. Each question carries equal marks.

1. (a) How will you implement the shift operations through hardware? Draw and explain 4-bit Combinational Circuit Shifter.

    (b) Interface one stage of arithmetic circuit and one stage of logical circuit with Shift operations to give complete Arithmetic Logic Shift Unit.

2. (a) Drive the Boolean logic expression for x_2. Show that x_2 can be generated with one AND gate and with one OR gate.

x1	x2	x3	x4	x5	x6	x7	S2	S1	S0	selected register
0	0	0	0	0	0	0	0	0	0	none
1	0	0	0	0	0	0	0	0	1	AR
0	1	0	0	0	0	0	0	1	0	PC
0	0	1	0	0	0	0	0	1	1	DR
0	0	0	1	0	0	0	1	0	0	AC
0	0	0	0	1	0	0	1	0	1	IR
0	0	0	0	0	1	0	1	1	0	TR
0	0	0	0	0	0	1	1	1	1	Memory

    (b) Write all the control functions with microinstructions for the basic computer in tabular form.

3. Draw the flow chart for first pass and second pass assembler.

4. Write the assembly code with flowchart to multiply two numbers

5. Write the assembly code for:

    i.   EX-OR operation with two operands.

    ii.   Double precision subtraction

    iii. Write a program to unpack two characters from location WRD and store them in bit 0 through 7 of locations CH1 and CH2. Bit 8 through 15 should contain zero.

6. (a) Explain the following Control Unit Implementation using block diagram:

    i.   Hardwired

ii.   Microprogrammed

(b) The Microinstruction Format for micro operations is shown below.

Microinstruction Format

3	3	3	2	2	7
F1	F2	F3	CD	BR	AD
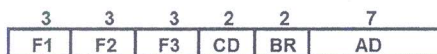
F1, F2, F3: Microoperation fields
CD: Condition for branching
BR: Branch field
AD: Address field

Write all the micro operations for all fields (F1, F2, F3, CD, BR).

7. For given control word and Encoding of register selection fields:

Control Word

3	3	3	5
SELA	SELB	SELD	OPR
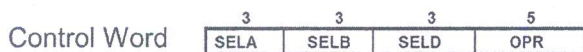
Encoding of register selection fields

Binary Code	SELA	SELB	SELD
000	Input	Input	None
001	R1	R1	R1
010	R2	R2	R2
011	R3	R3	R3
100	R4	R4	R4
101	R5	R5	R5
110	R6	R6	R6
111	R7	R7	R7

cpe 252: Computer Organization

i.   List the encoded ALU operations

OPR Select	Operation	Symbol
00000		
00001		
00010		
00101		
00110		
01000		
01010		
01100		
01110		
10000		
11000		

ii   Explain the following micro operations

Microoperation	Symbolic Designation				Control Word
	SELA	SELB	SELD	OPR	
R1 ← R2 - R3					
R4 ← R4 ∨ R5					
R6 ← R6 + 1					
R7 ← R1					
Output ← R2					
Output ← Input					
R4 ← shl R4					
R5 ← 0					