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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-3 EXAMINATION- JUNE -2016

B.Tech VI Semester

COURSE CODE: 10B11CI613 MAX. MARKS: 35

COURSE NAME: Computer Organization & Architecture

COURSE CREDITS: 04 MAX. TIME: 2 HRS

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

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1. An instruction is stored at location 3000 with its address field at location 3001. The address field has the value 4500. A processor register R1 contains the number 2000. Evaluate the effective address if the addressing mode of the instruction is (i) Direct (ii) Immediate (iii) Relative (iv) Register (v) Register Indirect (vi) Index with R1 as the index register
(b) The content of the top of a memory stack is 5320. The content of the stack pointer SP is 3560. A two word call subroutine instruction is located in memory at an address 1120 followed by the address field of 6720 at location 1121. What are the content of PC, SP and the top of the stack:
(i) Before the call instruction is fetched from memory? (ii) After the call instruction is executed? (iii) After the return from subroutine? [3.5+3.5]

2. Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instructions I1, I2, I3,… , I12 is executed in this pipelined processor. Instruction I4 is the only branch instruction and its branch target is I9. If the branch is taken during the execution of this program, calculate the time (in ns) needed to complete the program. [7]

3. State and explain Booth's algorithm in detail with suitable flow chart. Dry run it using multiply 7 by -5. [7]

4. (a) Explain the working of Intel 8237A DMA Controller with suitable block diagram. Justify with suitable example how DMA based I/O operation is faster than programmed or interrupt based I/O operation.
(b) Consider a disk with an advertised average seek time of 8 ms, rotation speed of 20000 rpm, and 512 byte sectors with 600 sectors per track. Suppose that we wish to read a file consisting of 3000 sectors. How much data will be transferred from 3000 sectors? Estimate the total transfer time using (a) Sequential access (b) Random access [3.5+3.5]

5. Write detailed notes on the following with suitable diagrams
(a) Static Ram and DRAM (b) RAID Levels [3.5+3.5]