Dr Pradeep Kr

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST -2 EXAMINATION- 2016
B.Tech VI Semester

COURSE CODE: 10B11CI613 MAX. MARKS: 25
COURSE NAME: Computer Organization & Architecture
COURSE CREDITS: 04 MAX. TIME: 1Hr 30 Min

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means. Vague answer will credit to zero marks*

1. **Justify the following statements with suitable reasoning, diagrams and examples** [5x2=10]
   (i) Cache coherence problem leads to inconsistent results in contemporary computers.
   (ii) Principle of locality of reference plays an important role in the design of efficient memory systems in computers.
   (iii) Fully associative mapping overcome the problem of thrashing.
   (iv) Instruction register plays an important role in instruction execution cycle.
   (v) Asynchronous timing of bus design is more efficient than synchronous timing of bus design.
2. Consider a computer with the following characteristics: total of 1Mbyte of main memory; word size of 1 byte; block size of 16 bytes; and cache size of 64 Kbytes. (a) For the main memory addresses of F0010, 01234, and CABBE, give the corresponding tag, cache line address, and word offsets for a direct-mapped cache. (b) Give any two main memory addresses with different tags that map to the same cache slot for a direct-mapped cache. (c) For the main memory addresses of F0010 and CABBE, give the corresponding tag and offset values for a fully-associative cache.
   d. For the main memory addresses of F0010 and CABBE, give the corresponding tag, cache set, and offset values for a two-way set-associative cache. [5]
3. A computer system has an L1 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size in L2 cache is 16 words. The memory access times are 2 nanoseconds. 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and main memory unit respectively.

   When there is a miss in L1 cache and a hit in L2 cache, a block is transferred from L2 cache to L1 cache. What is the time taken for this transfer? [3]
4. Let us assume that the processor is going to execute ADD B,A instruction of 16 bit which stores the sum of the contents of memory locations B and A into memory location A. Partial list of opcodes is 0001: Load AC from memory, 0010:Store AC to memory, 0101: Add to AC from memory. PC content is initialized to 300. Memory snapshot is shown as

Memory Locations	Instructions (Integer Format)
300	1 9 4 0
301	5 9 4 1
302	2 9 4 1
.....	.....
940	0 0 0 3
941	0 0 0 2

   Show step by step execution of the above said instructions using IR, PC, AC and memory locations. [3]
5. Design traditional bus architecture for your computer. Show all components that you can connect within your bus design. What problems you observe in your design as far as contemporary computers are concerned? Modify your design so as it can fulfill the needs of contemporary computers. [4]