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TEST-2 EXAMINATION (April 2016)

B.Tech 4th Sem (ECE)

COURESE CODE :- 10B11EC401 MAX. MARKS :25

COURSE NAME :- Digital Electronics

COURSE CREDITS: 4 MAX. TIME :1Hr 30Min

Note: All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means. Attempt all parts of a question at one place.

Q1(a). Use K-map to convert the following POS expression into a minimized POS expression, a minimized SOP expression. **(1+1=2)**

$F = (\bar{A}+\bar{B}+C+D)\,(A+\bar{B}+C+D)\,(A+B+C+\bar{D})\,(A+B+\bar{C}+\bar{D})\,(\bar{A}+B+C+\bar{D})\,(A+B+\bar{C}+D)$

Q1(b). Using Boolean algebra, show that $A\bar{B}C + B + B\bar{D} + AB\bar{D} + \bar{A}C = B + C$ **(2)**

Q1(c). $\bar{W}X+YZ$ is a simplified Boolean expression of the expression $WXYZ+\bar{W}\bar{X}YZ+\bar{W}X$. Determine if there are any don't care entries. If yes, determine those. **(1)**

Q2 (a). Design a 4-input priority encoder and explain its working. **(3)**

Q2(b). Draw the circuit of 4-bit binary parallel adder subtractor and explain its working. **(2)**

Q3(a). Design a 2 bit magnitude comparator using 1:16 demultiplexer. **(3)**

Q3(b). Design a 40:1 Multiplexer using 8:1 multiplexers only. **(2)**

Q4(a). What is race around condition? Draw and explain the circuit to overcome this problem. **(1+2 =3)**

Q4(b). Differentiate between combinational and sequential circuit. Draw the circuit of T latch using NAND gates only. **(1+1 =2)**

Q5(a). Convert D flip flop to S-R flip flop. **(2)**

Q5(b). Draw and explain the excitation table of J-K flip flop. **(1.5)**

Q5(c). Derive the characteristic equation of S-R flip flop. **(1.5)**